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# PREFACE TO THE PROCEEDINGS OF THERMINIC 2016

This 22<sup>nd</sup> edition of THERMINIC is again the main European event for academics and industry to share recent advancements in thermal issues of electronics and micro-electronics, including problems of nano-scale heat-transfer, thermal modeling and simulation issues in solid-state lighting as well as cooling issues of power electronics.

Following the workshops held in Grenoble (1995), Budapest (1996), Cannes (1997 and 1998), Rome (1999), Budapest (2000), Paris (2001), Madrid (2002), Aix-en-Provence (2003), Sophia Antipolis (2004), Belgirate (2005), Nice (2006), Budapest (2007), Rome (2008), Leuven (2009), Barcelona (2010), Paris (2011), Budapest (2012), Berlin (2013), Greenwhich (2014), and Paris (2015) the workshop is back again to the Hungarian capital, 20 years after THERMINIC was held in Budapest for the first time.

The 22nd THERMINIC Workshop once more proposed a strong technical program. This year's event had a special focus on advanced thermal management, thermo-mechanical reliability, solid-state lighting and power electronics components – both form design and testing aspects. The Components, Packaging and Manufacturing Technology Society co-sponsored this year's workshop, which gathered over 100 attendees from around the world.

PREFACE

The workshop featured 3 keynote talks, 12 sessions with oral presentation of contributed papers and with sessions introducing the 19 posers accepted for the workshop. A small vendors' exhibition and presentation has also been organized. This volume forms the proceedings (collection of papers) of the 22nd Therminic Workshop, containing the full text of all of the 44 contributed papers and it also contains the text version of 18 contributions that have been presented on posters. The workshop program featured two sessions partially dedicated to European research projects: to the QUANTIHEAT project and to the Delphi4LED project.

We would like to express our sincere appreciation to the authors for their valuable contributions to the Workshop. We are also grateful to the members of the Program Committee who have given of their time and expertise to review and help select the papers contained herein. We hope that you will find the contents of these Proceedings beneficial to your own work.



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SESSION OVERVIEW

## **Table of Contents**

## Session 1: Advanced Thermal Management

Fabrication Of A Micro-Thermoelectric Cooler (µ-TEC) For Room Temperature Applications By Template Assisted Electrodeposition Javier García Fernández, Nicolás Pérez Rodriguez, Melanie Mohn, Tom Sieger, Heike Schlörb, Heiko Reith, Gabi Schierning, Kornelius Nielsch	14
<b>Thermo-Mechanical Assessment of Copper and Graphite Heat</b> <b>Spreaders for Compact Packages</b> Rafael Prieto, Jean-Philippe Colonna, Perceval Coudrain, Norbert Chevrier, Severine Cheramy, Alexis Farcy	19
<b>Optimal Thermal Design of CMOS for Direct Integration of Carbon</b> <b>Nanotubes</b> Avisek Roy, Ferenc Ender, Mehdi Azadmehr, Knut E. Aasmundtveit	23
Session 2: Thermo-mechanical Reliability	
Location Resolved Transient Thermal Analysis to Investigate Crack Growth in Solder Joints E Liu, Thomas Zahner, Sebastian Besold, Gordon Elger	28
<b>Collapse of a Liquid Solder Bump under Load</b> Wendy Luiten, Co van Veen	34
<b>Determination of Bond Wire Failure Probabilities in</b> <b>Microelectronic Packages</b> Thorben Casper, Ulrich Römer, Sebastian Schöps	39
Session 3: Power Electronics 1: Design	
Design Methodology for Over-Temperature Protection of an LDO Voltage Regulator by Using Electro-thermal Simulations Cosmin-Sorin Plesa, Marius Neag, Cristian Boianceanu, Andrei Negoita	46
Smaller Size and Higher Reliability for Vertical Chip Mount Type IGBT	52

**Module** Naoki Yamanari, Toshiharu Ohbu, Hiroaki Ito, Shinichiro Matsuyama

Electro-Thermal Simulation for High Power IGBTs for Automotive	58
Applications	
Asantha Kempitiya, Wibawa Chou	

Asantha Kempitiya, Wibawa Chou

## Session 4: Compact Thermal Modeling

Model Order Reduction in Inductors for Rapid Virtual Prototyping in Power Electronics Chris Bailey, Catherine Tony		
<b>Calibration of Detailed Thermal Models by Parametric Dynamic Compact Thermal Models</b> Lorenzo Codecasa, Vincenzo d'Alessandro, Alessandro Magnani, Niccolò Rinaldi	69	
<b>Evolution of the DELPHI Compact Thermal Modeling Method:</b> <b>an Investigation on the Boundary Conditions Scenarios</b> Eric Monier-Vinard, Valentin Bissuel, Brice Rogie, Najib Laraqi, Olivier Daniel, Marie-Cécile Kotelon	76	
Novel Partition-Based Approach to Dynamic Compact Thermal	82	
Lorenzo Codecasa, Vincenzo d'Alessandro, Alessandro Magnani, Niccolò Rinaldi		
Session 5: Session 5: 3D IC / Packaging		
Analysis of the Impact of Power Distribution on the Efficiency of Microchannel Cooling in 3D ICs Piotr Zajac, Cezary Maj, Andrzej Napieralski	90	
<b>Closing the Power Delivery/Heat Removal Cycle for Heterogeneous</b> <b>Multi-Scale Systems</b> Mircea Stan, Kevin Skadron, Ke Wang	96	
Session 6: Quantiheat Project / Nano-scale Thermal Investigations		
<b>QUANTIHEAT Project: Main Progresses</b> Séverine Gomès, QuantiHeat Consortium	104	
<b>Calibration Methodologies for Scanning Thermal Microscopy</b> Eloïse Guen, David Renahy, Mouhannad Massoud, Jean-Marie Bluet, Pierre-Olivier Chapuis, Séverine Gomes	110	
<b>Thermal Analysis of Advanced Microelectronic Devices Using</b> <b>Thermoreflectance Thermograhy</b> Dustin Kendig, Andrew Tay, Ali Shakouri	115	
Modeling and Measurement of the Thermal Conductivity of Composites with Silver Particles	121	
Jose Ordonez-Miranda, Mohamad Abo Ras, Bernhard Wunderle, Sebastian Volz		
DPL Thermal Model of Test Microchip Structure without Cavity Dedicated to Estimation of Nanoelectronic Circuits Thermal Properties Tomasz Raszkowski, Mariusz Zubert, Agnieszka Samson, Marcin Janicki,	125	

Andrzej Napieralski

## Session 7: Power Electronics 2: Testing

Extracting Structure Functions of Power Devices in Induction Motor Drives	130
Attahir Murtala Aliyu, Alberto Castellazzi	
<b>Characterization of Thermal Interface Materials for IGBT Inverter Applications</b> Xavier Jordà, Xavier Perpiñà, Miquel Vellvehi, Manuel Fernández, Sergio Llorente, Sandra Aranda	136
<b>Difficulties in Characterizing Transient Thermal Resistance of SiC MOSFETs</b> Tsuyoshi Funaki, Shuhei Fukunaga	141

## Session 8: Thermal Design with CFD Simulation

<b>A Novel Approach to Heatsink Mass Minimisation</b> Robin Bornoff, John Parry, John Wilson	148
Flexible CFD Simulation Model Of A Thin Vapor Chamber For Mobile Applications Lauri Petteri Niittymäki, Catharina R Biber	152
<b>Heat Transfer Enhancement in Micro-scale Air Flows</b> Moshe Rosenfeld, Efi Zemach	158
Detailed Analysis of IC Packages Using Thermal Transient Testing and CFD Modelling for Communication Device Applications Yake Fang, Gang Wang, Andras Vass-Varnai	164
Methodology to Achieve the Thermal Management of a 6U Conducted-cooled Board with 130W Power Dissipation and an Operating Temperature of 85°C	169

Jérôme Maquet

## Session 9: DELPHI4LED Special Session

Delphi4LED - From Measurements to Standardized Multi-Domain Compact Models of LEDs: a New European R&D Project for Predictive and Efficient Multi-domain Modeling and Simulation of LEDs at all Integration Levels Along the SSL Supply Chain Robin Bornoff, Volker Hildenbrand, Sangye Lugten, Genevieve Martin, Christophe Marty, Andras Poppe, Marta Rencz, Wil Schilders, Joan Yu	174
Multi-domain Modelling of Power LEDs Based on Measured Isothermal and Transient I-V-L Characteristics Gábor Farkas, Márton C. Bein, Lajos Gaál	181
<b>LED Module Multi-physic Approach</b> Theo Renaudin, Julien Joly, Benoit Hamon, Benoit Tothe	187
Investigation of the Temperature-Dependent Heat Path of an LED Module by Thermal Simulation and Design of Experiments Lisa Mitterhuber, Stefan Defregger, Elke Kraker, Julien Magnien, René Hammer	194

## Session 10: LEDs and LED Lamps

<b>Modelling LED Lamps with Thermal Phenomena Taken into Account</b> Krzysztof Górecki, Przemysław Ptak		
<b>Embedded Multi-domain LED Model for Adaptive Dimming of Streetlighting Luminaires</b> János Hegedüs, Gusztav Hantos, András Poppe	208	
Experimental Study of Electroluminescence and Temperature Distribution in High-power AlGaInN LEDs & LED Matrixes Anton Chernyakov, Andrey Aladov, Ivan Kalashnikov, Aleksander Zakgeim, Michael Mizerov Session 11: Reliability Investigations	213	
Aging Tendencies of Power MOSFETs – A Reliability Testing Method Combined with Thermal Performance Monitoring Gusztav Hantos, Janos Hegedus, Marta Rencz, Andras Poppe	220	
Implementation of Moisture Diffusion Model in Multi-material System Including Air Cavities Norbert Péter, Péter Tóth, Boldizsár Kovács, Gergely Kristóf	224	

In-situ Monitoring of Interface Delamination by Local Thermal	
Transducers Exemplified for a Flip-chip Package	
Bernhard Wunderle, Daniel May, Mohamad Abo Ras, Sergey Sheva,	
Marcus Schulz, Markus Woehrmann, Joerg Bauer, Juergen Keller	

## Session 12: Thermal Characterization and Modeling

<b>Design of Heated-micro-Resonator Rings</b> Shenghui Lei, Ryan Enright, Alexandre Shen	238
<b>Novel Test Stand for Thermal Diffusivity Measurement of Bulk and Thin Films</b> Mohamad Abo Ras, Daniel May, Bernhard Wunderle	243
Temperature Characterization of Small-Scale SOI MOSFETs in the Extended Range (to 300°C) Konstantin O. Petrosyants, Sergey V. Lebedev, Lev M. Sambursky, Veniamin G. Stakhin, Igor A. Kharitonov	250
Investigation of Heat Transfer Coefficient Variation in Air Cooled Hybrid Electronic Circuits Marcin Janicki	255
Posters	
<b>Fabrication and Characterization of Microscale Heat Sinks</b> Gábor Takács, György Bognár, Enikő Bándy, Gábor Rózsás, Péter Gábor Szabó	264

Reliability assessment of Wafer Level Chip Scale Package (WLCSP) 268 based on Distance-to-Neutral point (DNP)

Tung Ching Lui, Balaji Nandhivarm Muthuraman

<b>Investigation on Solder Voids in Flip-Chip Light-Emitting Diodes Using Thermal Transient Response</b> Byungjin Ma, Chang Wan Kim, Kun Hyung Lee, Won-Bae Suh, Kwanhun Lee	272
<b>Digital Thermal Sensor Based on Ring-Oscillators in Zynq SoC Technology</b> Charles-Alexis Lefebvre, Leire Rubio, Jose Luis Montero	276
<b>Peltiér Cells Cooling System for Switch Mode Power Supply</b> Giovanni Casano, Stefano Piva	279
<b>Dynamical Phase Transitions on Nanoscale</b> György Kocsis, Ferenc Márkus	283
<b>Cost-efficient In-situ End-of-life Prognostics of Power Dies and LEDs by Junction Temperature Measurement</b> Sergey Sheva, Raul Mroßko, Jens Heilmann, Bernhard Wunderle, Gusztáv Hantos, Sander Noijen, Jürgen Keller	287
Electronic Module for the Thermal Monitoring of a Li-ion Battery Cell through the Electrochemical Impedance Estimation Marco Ranieri, Diego Alberto, Hélène Piret, Viviane Cattin	294
<b>Multi-objective Optimization of Fin Array Heat Sinks</b> Reijo Karvinen, Kaj Lampio	298
Improved Method for Logi-Thermal Simulation with Temperature Dependent Signal Delay Lázár Jani, András Poppe	302
<b>Modelling of the Thermoelectrical Performance of Devices Based on VO<sub>2</sub></b> Soma Ur, János Mizsei, László Pohl	307
Influence of the Photoactive Layer Thickness on the Device Parameters and their Temperature Dependence in Thin Crystalline Silicon Photovoltaic Devices Balázs Plesz, János Mizsei	311
A Study of Electrolytic Capacitors Thermal Conductivity, Behavior and Measurement Zhigang Na	315
<b>Effect of Flow and Geometry Parameters on Performance of Solar Air Heater</b> Ram Subhash Maurya, Zaid A J Ansari	319
Mathematical Modelling of Coupled Heat and Mass Transport into an Electronic Enclosure Zygimantas Staliulionis, Mirmasoud Jabbari, Jesper Henri Hattel	323
Simulation of the Thermal Behavior of a Composite Conductive Adhesive Stánhana Lefèvra, Avlin Yuksal, Gungar, Sávarina Gamàs	327
Modelling of Thermal Processes in Heat Flux Sensors Alexander Kozlov	332
Fabrication, Performance and Reliability of a Thermally Enhanced Wafer Level Fan Out Demonstrator with Integrated Heatsink André Gil Cardoso, Hugo Barros, Gusztav Hantos	334

345

**SESSION 1** 

# **SESSION 1** Advanced Thermal Management

# Fabrication of a Micro-Thermoelectric Cooler for Room Temperature Applications by Template Assisted Electrodeposition

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## Abstract

Solid state refrigeration is of great interest due to its potential application in electronic and optoelectronic systems. Nowadays, macroscopic thermoelectric coolers are part of such systems and their cooling performance and reliability are well proven. However, the feasibility of microstructuring such kind of devices by means of photolithographic techniques, opens the possibility of integration on a chip for better local thermal management. Together with previous facts, electrodeposition processes are well known to be low cost, highly scalable and compatible with lithographic techniques. In this work we report on the fabrication of BiTe-based Micro-Thermoelectric Coolers by means of a mixed process flow involving photolithography and electrodeposition techniques. Materials and geometry of the device have been chosen to optimise the cooling performance on an integrated photonic system.

## 1. Introduction

Solid state refrigerators based on thermoelectric materials are currently used in actual optoelectronic devices. However, such coolers are incorporated as a second component of the chip due to their macroscopic sizes, acting as a cooling block around the whole circuit. Thermal management integrated in optoelectronic circuits can improve the performance of the device. Such local thermal control can be achieved by the integration of micro-thermoelectric coolers (µ-TEC's) around the element which temperature has to be controlled [1]. Currently photonic systems used for high-bandwidth communications, show an optimum performance at a precisely defined working temperature, around 40°C, requiring temperature control of ±0.1 °C [1,2]. Therefore, the thermoelectric materials need to have high thermoelectric efficiency ZT at room temperature. BiTe-based materials are the main candidates to achieve the previous requirements since ZT values around 1 at room temperature have been reported in the literature [3-6]. Moreover, novel thermoelectric materials based in ternary alloys as, for example n-doped Bi<sub>2</sub>(Te<sub>x</sub>Se<sub>1-x</sub>)<sub>3</sub> and p-doped (Bi<sub>x</sub>Sb<sub>1-x</sub>)<sub>2</sub>Te<sub>3</sub> V-VI semiconductors, have been found to show lower thermal conductivities and thus higher ZT values than their respective binary compounds[7, 8, 9].

The sizes of photonic active elements are in the micrometer range, opening the possibility to use of standard photolithographic techniques to fabricate suitable  $\mu$ -TEC's adapted to the geometrical characteristics of the device [10]. Furthermore, such microstructured lithographic masks can be used as templates in electrochemical deposition processes which in addition, are low cost and scalable techniques compatible with CMOS technologies [11, 12]. The combination of both previous fabrication routes allows the implementation of  $\mu$ -TEC's during the fabrication process of the photonic integrated circuit.

In this work, we report on the fabrication of a  $\mu$ -TEC composed of Bi<sub>2</sub>(Te<sub>x</sub>Se<sub>1-x</sub>)<sub>3</sub> and (Bi<sub>x</sub>Sb<sub>1-x</sub>)<sub>2</sub>Te<sub>3</sub> as a n- and p-type material, respectively. Both materials are fabricated by means of electrodeposition technique. The deposition parameters have been optimized in terms of morphology and maximal thermoelectric efficiency of the material. The process flow followed in the fabrication of the  $\mu$ -TEC is also reported.

## 2. Methodology

## 2.1. Materials synthesis

For the electrochemical deposition of BiTe-based materials a pulsed plated technique in a conventional three electrode arrangement was employed. The substrates used in this study consist of thermally oxidized Si-wafers coated with Cr/Au metal contact acting as the working electrode. A Pt wire is used as counter electrode and all potentials are measured versus an Ag/AgCl reference electrode. Ternary Bi<sub>2</sub>(Te<sub>x</sub>Se<sub>1</sub>- $_x)_3$  and  $(Bi_xSb_{1-x})_2Te_3$  have been synthesized as n- and p-type material, respectively. All depositions were performed at room temperature from an electrolyte containing 1 mol  $L^{-1}$ nitric acid at pH 0. The electrolyte for n-type Bi<sub>2</sub>(Te<sub>x</sub>Se<sub>1-x</sub>)<sub>3</sub> depositions is prepared dissolving 0.01 mol  $L^{-1}$  TeO<sub>2</sub> in the nitric acid followed by 0.01 mol  $L^{-1}$  Bi(NO<sub>3</sub>)<sub>3</sub>\*5H<sub>2</sub>O and 0.0011 mol L<sup>-1</sup> SeO<sub>2</sub>. To prepare the p-type (Bi<sub>x</sub> Sb<sub>1-x</sub>)Te<sub>3</sub> electrolyte 0.007 mol  $L^{-1}$  TeO<sub>2</sub> and 0.002 mol  $L^{-1}$  Bi(NO<sub>3</sub>)<sub>3</sub> are first dissolved in nitric acid while a separate solution is made by dissolving 0.25 mol L<sup>-1</sup> tartaric acid as a complexing agent in distilled water followed by subsequent dissolution of 0.006 mol  $L^{-1}$  Sb<sub>2</sub>O<sub>3</sub>. After mixing both solutions the

electrolyte is filled with water up to the desired volume. Pulsed deposition technique has been used for the fabrication of both kinds of materials. Such technique consists on a deposition pulse at fixed deposition potential ( $E_{on}$ ) during short pulse time ( $t_{on}$ ). During this pulse time, the net deposition of material on the working electrode is carried out. This pulse is followed by a resting time holding a reverse potential ( $E_{off}$ ) with the off pulse time ( $t_{off}$ ). All the parameters have been optimized in order to obtain materials suitable for the  $\mu$ -TEC fabrication and specific values are summarized in following sections.

Finally, for top contact fabrication, Nickel has been electroplated from a bath containing 300 g/l NiSO<sub>4</sub> + 50 g/l NiCl<sub>2</sub> + 40 g/l H<sub>3</sub>BO<sub>3</sub> + 5 g/l Saccharine. The electrodeposition has been carried out at a constant current density of  $1A/dm^2$  under vigorous stirring and the electrolyte has been maintained at 60°C to avoid boric acid precipitation.

## 2.2. Characterization techniques

Morphology and composition of the materials are evaluated with an SEM equipped with an EDX analyser (SEM Leo 1530 Gemini/Zeiss with EDX X-Flash detector, Esprit/Bruker). The SEM is also employed for general imaging of the final  $\mu$ -TEC and EDX analysis of the different components.

In order to quantify the thermoelectric performance of the materials investigated in this work, the power factor (PF) of the samples has been characterized. The power factor

$$PF = S^2 \sigma \tag{1}$$

can be obtained from the measured Seebeck coefficient *S* and the electrical conductivity  $\sigma$ .

First of all, room temperature Seebeck coefficient has been measured by means of a Potential Seebeck Microprobe-PSM (PANCO GmbH), and has been used as the first quality indicator. In order to measure the power factor as a function of temperature, a Seebeck coefficient and electric resistivity measurement system from Linseis (LSR-3) was used. In order to double check the electrical conductivity values, van der Pauw measurements have been performed in a physical properties measurement system (Dynacool) from Quantum Designs. In order to avoid the electric and thermal shortcut of the Au seed layer used as contact for the electrodeposition, the samples were transferred to a glass matrix. Therefore, after the electrodeposition of a continuous film sodium silicate solution (Merck KGaA) has been deposit on top of the film covering the entire surface and dried on a hot plate at 80°C, becoming solid glass after 20 minutes. Directly after the annealing process, the sample was placed on a cold Cu block at 8°C. Due to the different thermal expansion coefficients of glass and metal seed layer, the deposited film embedded in the glass matrix is detached from the substrate. An example of a Hall-bar structure transferred by this method can be seen in Figure 1. In the EDX analysis of the surface that was in direct contact with the seed layer (Cr/Au), no rests or traces of Au were detected.

## 2.3. Photolithographic process

In order to fabricate the templates for the electrodeposition process, AZ 9260 photoresist (MicroChemicals GmbH) was spin-coated on the Au coated Si wafer. This process consisted on a first spin-coating at 2400 rpm for 60 s followed by a soft bake at 110°C for 80 seconds. This step leads to a photoresist thickness of 10 $\mu$ m. To increase the photoresist thickness, a second spin-coating is performed at 2100 rpm for 60 seconds, followed by a soft bake at 110°C for 160 seconds. This two-step process results in a 24  $\mu$ m thick homogeneous photoresist film. The exposure is carried out by direct writing technique, using a laser writer  $\mu$ PG-101 from Heidelberg Instruments, equipped with a diode laser at 405 nm. The power of the laser is fixed to 7 mW and all exposed structures are developed for 12 minutes in AZ 400K developer diluted in four parts of DI water.



Figure 1:a), b) and c) Schematic cross section views of the sample transferring process into a glass matrix. d) Optical image of a transferred  $Bi_2(Te_xSe_{1-x})_3$  Hall-bar structure.

The specific process flow followed in this work combines the material synthesis and photolithographic processes. The first lithographic step is used for pre-structuring the metal seed layer previously sputtered on top of the Si/SiO<sub>2</sub> wafers. This step is performed in order to avoid electrical shortcut between consecutive leg-pairs which separation is around 8 µm. After exposing and developing the photoresist with the pattern that can be appreciated in Figure 2 a), the Au contact and Cr adhesion layer are wet chemically removed by short dipping in Ki+KI<sub>2</sub> and Kodak EB-5 etchants, respectively [13, 14]. The length of the etched structures is 180 µm. The electrical path at this point is not completely shortcut because of the requirement of electrical contact for the electrodeposition processes, see Figure 2 b). The second lithographic process consists on the spin coating of a 24 µm thick positive photoresist and the photolithographic structuring of cavities  $(20x140 \ \mu m^2)$  for the first material type deposition as shown in Figure 2 c). The electrodeposition time is chosen to achieve 10  $\mu$ m thick thermoelectric films, partially filling the cavity as it is schematized in Figure 2 d). Following the previous steps, the substrate is coated with the photoresist for the third lithography structuring. In this step, the cavities for deposition of the second type of material are structured, as presented in Figure 2 e).



Figure 2: Schematic process flow followed in this work to fabricate the  $\mu$ -TEC. j) represents the electrical contact arrangement for single leg characterization.

With those parameters used in the lithographic process, the first material that was deposited is completely covered by the

photoresist, avoiding any degradation or contamination of the material during the second electrodeposition step, Figure 2 f). In order to fabricate the top contact between the n- and p-type legs, a fourth lithographic step is required. In this case, the photoresist on top of each leg is exposed and completely developed. However, in order to have a metal contact on the free space between legs, the exposure dose is reduced as such in the same developing time the height of the photoresist is levelled with the thermoelectric materials. An example of this step is schematized in Figure 2 g). Last step consisted on the sputtering of a second Au layer that acts as an electrical contact for the electrodeposition of the Ni top contact, Figures 2 h) and i).

Finally, the remaining Cr/Au seed layer is structured to connect in series the leg-pairs of the  $\mu$ -TEC. In addition, within this process, metal contacts can be structured for single leg-pair characterization as is shown in Figure 2 j).

## 3. Results

## 3.1. Materials optimization

Before the electrodeposition on structured samples, the electrochemical parameters of continuous films have been optimized in terms of their compactness and smoothness. Pulsed deposition method has been found to provide smoother deposits since the resting pulse allows homogenizing the electrolyte's concentration near the working electrode. The difference on the film morphology between potentiostatic and pulsed deposition methods is shown in Figure 3 a) and b) for Bi<sub>2</sub>(Te<sub>x</sub>Se<sub>1-x</sub>)<sub>3</sub>. In Figure 3 c) and d), the effect of the pulse time on the film morphology is also compared for (Bi<sub>x</sub>Sb<sub>1-x</sub>)<sub>2</sub>Te<sub>3</sub> samples.



Figure 3: Cross-section SEM images of potentiostatically a) and pulsed  $(t_{on}/t_{off}=10ms/50ms)$  deposited  $Bi_2(Te_xSe_{1-x})_3$  films. c) and d) show  $(Bi_xSb_{1-x})_2Te_3$  films deposited at different pulse times,  $t_{on}/t_{off}=10ms/250ms$  and  $t_{on}/t_{off}=100ms/2500ms$ , respectively.

In the case of pulsed deposition, potential values for the deposition pulse ( $E_{on}$ ) and the rest pulse ( $E_{off}$ ) and their duration ( $t_{on}$  and  $t_{off}$ , respectively) need to be adjusted for optimized morphological characteristics of the deposits and their thermoelectric properties. For the p- type material longer

pulses were needed in order to achieve compact deposits with lower roughness (Fig. 3(c,d)). In structures as small as 20x20  $\mu$ m<sup>2</sup>, fine tuning of  $t_{off}$  results in an improved homogeneity of the deposits as discussed later. For the n- type material, best results were obtained in structured substrates by fine tuning  $E_{on}$ . With respect to the thermoelectric properties, the value of  $E_{off}$  during the resting pulse proved to have strong impact on the Seebeck coefficient (Fig. 4) weakly affecting the compactness and roughness of the deposits, which as commented above has been found to be more dependent on the electrodeposition potentials and pulse times. Thus, the final deposition parameters were chosen as a compromise between thermoelectric properties and homogeneity of the films.



Figure 4: Seebeck coefficient as a function of the off-potential for  $Bi_2(Te_xSe_{1-x})_3$  (close squares) and  $(Bi_xSb_{1-x})_2Te_3$  (open squares).

Electrochemical parameters that show the optimum values of the Seebeck coefficient in homogeneous films, have been used in the  $\mu$ -TEC fabrication process. A summary of these parameters and their Seebeck coefficient and electrical conductivity values can be found in Table 1.

Table 1: Deposition parameters used for the fabrication of  $\mu$ -TEC's. Seebeck coefficient and electrical conductivity are also shown.

	Eon	ton	Eoff	toff	S	σ
Units	mV	ms	mV	ms	$\mu V/K$	S/cm
Bi <sub>2</sub> (Te <sub>x</sub> Se <sub>1-x</sub> ) <sub>3</sub>	-100	10	180	50	-60	1000
(Bi <sub>x</sub> Sb <sub>1-x</sub> ) <sub>2</sub> Te <sub>3</sub>	-250	100	87	2500	140	2000

## 3.2. µ-TEC fabrication process

Previous parameters were used for the electrodeposition of both materials in the templates prepared by photolithographic structuring. However, a strong edge effect is observed in  $20x20 \ \mu m^2$  small structures, where the deposits grow extremely fast and rough in both Bi<sub>2</sub>(Te<sub>x</sub>Se<sub>1-x</sub>)<sub>3</sub> and (Bi<sub>x</sub>Sb<sub>1-x</sub>)<sub>2</sub>Te<sub>3</sub> as can be seen in Figure 5 a) and b), respectively. As material is not being deposited where the working electrode is covered with the photoresist, this effect can be explained with a higher concentration of the electrolyte close to the edges of the photoresist. Moreover, this effect could be minimized by stirring the electrolyte during deposition, homogenizing the ions over the whole cavity where the thermoelectric material is deposited. Ultrasonic assisted stirring, has been found to be the most promising route to achieve confined electrodeposited structures which results are shown in Figure 5 c), showing the fact that the edges of the structures are well defined.

Making use of this approach for structured electrodeposition of the thermoelectric materials, together with the process flow detailed above, a working  $\mu$ -TEC has been fabricated which geometrical characteristics fits with the requirements for its application on a real photonic system. A tilted SEM image is shown in Figure 6. As can be seen, high compactness of legpairs has been achieved. Furthermore, Ni free standing contacts between the legs are stable enough for a robust  $\mu$ -TEC device. Such top contacts are deposited on top of both n-type and p-type materials ensuring homogeneous contacts.



Figure 5: SEM pictures of  $20x20 \ \mu m^2$  small structures where the edge effect can be easily appreciated in both a) Bi<sub>2</sub>(Te<sub>x</sub>Se<sub>1-x</sub>)<sub>3</sub> and b) (Bi<sub>x</sub>Sb<sub>1-x</sub>)<sub>2</sub>Te<sub>3</sub>. c) Shows the well-defined structures of both kind of materials achieved by ultrasonic assisted electrochemical deposition.

In order to electrically characterise a single leg-pair, the remaining Cr/Au seed layer has been patterned in configuration shown in the inset of Figure 6, where the current path is also highlighted (black line). The values of the total resistance measured in different leg-pairs has been found to be around 80  $\Omega$ . Taking into account the low resistance of the n- and p-type legs fabricated in this work, the strong contribution of the contact resistance between the thermoelectric material and the contacts has a strong impact on the total resistance. This effect is even more pronounced due to the high roughness that increases the total contact area, especially in the case of the (Bi<sub>x</sub>Sb<sub>1-x</sub>)<sub>2</sub>Te<sub>3</sub> material.



Figure 6: Tilted SEM picture of a portion of the  $\mu$ -TEC. Inset shows the electrical configuration for single leg-pair configuration.

## 4. Conclusions

In this work,  $Bi_2(Te_xSe_{1-x})_3$  and  $(Bi_xSb_{1-x})_2Te_3$  ternary films have been successfully fabricated by means of pulsed electrodeposition process. The electrochemical parameters have been found to affect strongly the morphological, compositional and thermoelectric properties of both types of materials. The optimal conditions have been used to fabricate µ-TEC by alternating both lithography and а electrodeposition Electrical processes. resistance measurement on single leg-pairs reveal the high influence of the contact resistance that, in fact, can reduce the performance of the device. Further efforts need to be done on achieving smoother as-deposited films in order to decrease the contact area and thus the total resistance of the device.

## Acknowledgements

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# Thermo-Mechanical Assessment of Copper and Graphite Heat Spreaders for Compact Packages

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## Abstract

Graphite-based materials have been proved to be an enhancement over copper heat spreaders when directly integrated at the silicon level. However, not only they outdo copper in terms of thermal performance, but their in-plane CTE (coefficient of thermal expansion) is much closer to that of silicon. As a result, mechanical stress due to deformation mismatches is reduced during thermal cycling. Thus, thermal interface thickness can be reduced to optimize the heat flow from the hotspot.

Heat management of 3D structures implies several challenges. The silicon die and intertier thickness are limited by the vertical connexions height in these heterogeneous stacks. These constraints will also imply strongly thinned heat spreaders and thermal interfaces in a future intertier implementation. This work investigates the thermo-mechanical constraints of integrating a heat spreader at the die level. Copper and PGS (pyrolytic graphite sheet) heat spreaders are compared. Their deformation subjected to thermal cycling is measured experimentally via Thermo-Moiré measurements. The differences in the deformation between the silicon die, molding and the substrate are also measured.

## 1. Introduction

Packaging technologies are now turning heads towards 3D integration, as it has already become a state of the art technology for a few low power applications. Poor thermal behavior and high heat flux densities, amongst other problems, are however delaying a wider implementation. Heat management of 3D structures implies several challenges [1]. In the case of compact packages, space constraints limit to passive solutions the choice of cooling methodologies.

Feasible cooling solutions are now being explored. Interleaving heat spreaders in the 3D stack could mitigate the strong hotspot dissipation issues in advanced 3D ICs [2,3]. Efforts are being made to stack as many layers of materials as possible within a confined space. The materials possess different mechanical and thermal properties. Mismatches in the coefficient of thermal expansion could induce mechanical constraints in these heterogeneous stacks. Mechanical stresses induced by the Coefficients of Thermal Expansion (CTE) mismatch of materials (around 2.6 ppm/K for Si, 17 ppm/K for Cu, and 19 ppm/K for BGA substrates) have proven to be detrimental in a thin-die integration flow. Warpage is a global effect of interfacial stress and displacement. Several failure modes can occur as a consequence of these CTE mismatches and warpage [4], such as: Interface delamination at die level, stress concentration spots leading to cracks, open or short-circuits during solder reflow or bumps deformation. State of the art passive cooling solutions need to be assessed from a thermo-mechanical scope. Moiré measurements are a powerful tool to describe the topography of heat spreaders during thermal cycles. They

are non contact and full field. This optical technique has already been used to characterize the mechanical behavior of boards [5], BGAs [6], and even interposers [7].

## 2. Methodology

## 2.1. Test vehicles

Two different structures are considered. The first one consisting of a three layer sandwich: heat spreader, thermal interface and silicon die (Figure 1a). It allows a simple approach to the thermomechanical constraints between two layers with different CTE. The interface material acts as a mechanical buffer of stress when deformation is induced due to a temperature change. The surface area of all samples is 1 cm<sup>2</sup>. The silicon die thickness is 200  $\mu$ m.



(a) Heatspreader on a bare (b) Heatspreader on an die exposed package.

## Figure 1: Samples structures

The second one (Figure1b) consists of a heat spreader implemented on top of a flip-chip packaged die.

Heatspreaders are integrated on a die exposed molding configuration in order to contact the top silicon surface. The chip package comprises a 300  $\mu$ m thick BGA substrate of 1 cm<sup>2</sup> (Figure 2). The embedded silicon die surface is 5,5mm x 5,8mm. Its thickness varies from 420  $\mu$ m to 450  $\mu$ m due to the grinding process. A standard underfill distributes the possible stress induced by the copper bumps.



(a) Copper heatspreader (b) PGS heatspreader

Figure 2: FIB – SEM sections of Cu and PGS heatspreader implementations using epoxy (a) or silicone (b) TIM

Heat spreader materials used are copper and PGS (Pyrolytic Graphite Sheet). Bonding process differs regarding the thermal interface material (TIM): Silicone or epoxy. Silicone TIM is manually dispensed using a syringe. A pattern is drawn on the surface of the die/package to homogeneously distribute the glue. The heat spreader is bonded on top of the sample. Uniform pressure is applied with a constant load to assure homogeneous distribution of the TIM. Epoxy TIM is dispensed using a Datacon automatic tool. Both interface materials are then annealed:  $100^{\circ}$ C or  $150^{\circ}$ C for epoxy and  $150^{\circ}$ C for silicone. Results show different levels of bow deformations regarding the heat spreader material (Figure 4).The layer thickness is  $107 \,\mu$ m for copper and  $70 \,\mu$ m for PGS.

## 2.2. Measurement set-up

Measurements are based on shadow moiré technique under thermal cycle [4]. This optical method assess the warpage evolution of a surface via the interference between two sets of light and dark gratings. When a beam of light illuminates the grating, it projects its shadow onto the surface of the sample under measurement. The shadow of the fixed reference grating evolves as the oven temperature changes. The light reflexion of the sample surface is captured by a camera placed on a different angle from the light beam. When the surface of the sample deviates from a flat plane or is not parallel to the grating, fringes are visible. The governing equation of shadow moiré is:

$$w = \frac{p}{\tan \alpha + \tan \beta}$$

Where w is the out of plane displacement of the sample surface between adjacent fringes, p is the grating pitch and  $\alpha/\beta$  angles are the light beam and the camera observation angle, respectively.



Figure 3: JEDEC thermal cycle used for moiré measurements

The thermal cycle is a JEDEC standard (J-STD-020D) with a maximum temperature of 260°C corresponding to a reflow process over 1600 s. (Figure 3).

## 3. Results and discussion

## 3.1. Heatspreader on bare silicon

Sample preparation needed an annealing process of the interface material in order to assure bonding. Measurements at ambient temperature show a significant deformation of Cu heat spreaders (Figure 4a) bonded to silicon dies. The samples are warped during cooling after the epoxy's curing. Samples show different warp results at 100°C or 150°C (Figure 5).



- (a) Cu heatspreader. Epoxy TIM. Profile at 25°C.
- (b) PGS heatspreader. Epoxy TIM. Profile at 25°C.

Figure 4: Warpage of samples at ambient temperature after TIM annealing process. Structure (a): Heatspreader on Si

On the other hand, PGS heat spreaders (Figure 4b) show no significant warp after curing and cooling for the same epoxy interface. PGS anisotropic structure implies different CTE values depending on the deformation direction. XY in plane CTE is slightly lower (0.9 ppm/K) than that of Si (2.6 ppm/K). On the other hand, Z axis CTE is significantly higher (32 ppm/K) even to that of copper (17 ppm/K). However, warp is induced by XY CTE mismatches between bonded layers. This warp induces shear stress when the temperature varies.





Figure 5 shows how temperature rise in the Cu samples produces a warp relaxation. Both layers, silicon and Cu, approach to a no warp state previous to the curing process. A slight hysteresis can be observed. The warp is inferior to 20  $\mu$ m above 150°C, this temperature being close to the Tg of the epoxy used as TIM. Calculations using the Stoney formula suggest that yield strength limit of the Cu is reached during the cycle, meaning possible plastic deformations.



*Figure 6: Warp evolution in a thermal cycle PGS Heatspreader on Si. Epoxy TIM cured at 150 °C.* 

PGS samples remain stable all over the thermal cycle, no significant variation has been measured (Figure 6). The heat spreader layer is therefore mechanically negligible in this case. Copper heat spreaders have a major influence in the mechanical behavior of the stack.

## **3.2.** Heatspreader on package

Mechanical behavior of real packages differ from that of a simple two layer stack. Warp deformation is highly influenced by the molding and the BGA substrate. However, significant modifications can be found when integrating an additional layer on top. Molding interaction with the BGA has been characterized. Figure 7 shows the thermal cycle of 450  $\mu$ m of epoxy molding on a BGA substrate. Comparisons between Moiré measurements of the package front and backside in a thermal cycle show a symmetrical warp in the absence of other layers. The symmetry remains during the whole thermal cycle. However, epoxy higher CTE produces a warp inflection of the package at 175°C, being this the



curing temperature of the molding.

*Figure 7: Front & Backside Warp in a thermal cycle. Epoxy Molding on a BGA substrate. No heatspreader.* 

Figure 8 shows a standard package with a die exposed molding configuration: A 5,5mm x 5,8mm silicon die embedded in an epoxy molding.



Figure 8: Front & Backside Warp in a thermal cycle. Standard package. Exposed silicon chip on a BGA substrate. No heatspreader.

Symmetry between the front and the backside is also found all along the thermal cycle, however, warp is not inverted with temperature increase. Minimum warp occurs around 200°C. The silicon die acts as a stiffener blocking the epoxy



deformation to warp the stack.

Figure 9: Front & Backside Warp in a thermal cycle. Cu heatspreader on an exposed package. Silicone TIM.

Heat spreader thickness and TIM characteristics can modify this symmetry. A decorrelation of the front and backside warp is shown in figure 9. Silicone TIM (Tg =  $-80^{\circ}$ C) remains viscous all over the thermal cycle. Stress is now transmitted to the rest of the package. The TIM layer acts as a buffer, damping heat spreader deformations. The addition of a copper heat spreader doesn't produce additional constraints to the package if the TIM is thick enough.

## 4. Conclusions

PGS heat spreaders appear to be a harmless cooling solution in terms of mechanical induced stresses. No significant warp has been measured over a wide thermal cycle. Copper heat spreaders, being at the state of the art, still need an interface thick enough to damp the mechanical stress of its deformation. The thermo-mechanical constraints of copper limit the use of thin interfaces, as needed for a close 3D die integration. PGS clearly exceed copper advantages.

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## **Optimal Thermal Design of CMOS for Direct Integration of Carbon Nanotubes**

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## Abstract

Carbon nanotubes (CNTs) exhibit many remarkable mechanical, electrical and thermal properties, which can be exploited in various smart sensing applications by integrating them in a standard CMOS process. However, such integration process is challenging since CMOS process is not suitable for high temperature application required for local CNT synthesis. This work involves designing power efficient CMOS compatible micro-heaters that can generate CNT growth temperature while maintaining CMOS compatible temperature in the microsystem. One metal interconnect layer and a polysilicon layer available in AMS 0.18  $\mu$ m CMOS technology have been used to design the micro-heaters. This paper proposes and compares four optimal micro-heater designs alongside their thermal & thermomechanical analysis using ANSYS. The promising results are expected to lead the way for successful implementation of carbon nanotube based sensors in a commercial CMOS process.

## 1 Introduction

Discovery of carbon nanotubes (CNTs) by Sumio Iijima, in 1991 [1] have opened the door for numerous research to utilize their unique properties in many applications. Their exceptionally high surface area to volume ratio, together with extraordinary electrical [2], mechanical [3], and thermal [4] properties make them lucrative for sensing applications [5]. CNTs have the potential to facilitate CMOS technology with ultra-sensing ability, hence, integration of CNTs in standard CMOS process is necessary for manufacturing low cost sensors. However, high CNT synthesis temperature (around 900 °C) is the main obstacle for the integration since CMOS circuits can only stand around 300 °C for a short period.



Figure 1: Concept of local CNT synthesis and direct integration into microsystem

Localized heating [6] is an effective solution for local synthesis where only a small portion of the structure (CNT growth region) is heated to such high temperature by joule heating. The microsystem has two micro-bridges as shown in *Figure 1*. A catalyst layer is deposited on the primary bridge before heating it to the desired temperature. High temperature breaks the catalyst layer into nanoparticles and carbon nanotubes start to grow when gas containing carbon is introduced in this CVD process. Generated electric field due

to potential difference between the bridges guide and attach CNTs to the secondary bridge, which completes a closed loop circuit. For gas sensors, electrical resistance of connected CNTs change when they interact with gas molecules.

This localized heating technique is well suited for MEMS microsystems. MEMS process is easier for fabricating freestanding bridges, which help to avoid direct heat transfer to the substrate. CNT growth in MEMS structures will require CMOS-MEMS integration. It needs complex post processing which is not cost effective for mass production. This work involves designing optimal micro-heaters that can be manufactured in a conventional CMOS process with the purpose of growing CNTs directly in CMOS. Different structures are designed; where some require a limited amount of dedicated post-processing, whereas others do not need any post-processing after the standard CMOS process.

## 2 Methodology

CMOS process is not intended for mechanical structures, and does not offer much flexibility for designing suspended structures. The material options are limited, and the design complexity is much higher than MEMS micro-heaters [7]. The micro-heaters need to generate high CNT synthesis temperature (around 900 °C) at low power within the stated restrictions, while avoiding significant bridge deformation. High thermal gradient is crucial to obtain CNT growth temperature and still keeping CMOS compatible temperature.

## 2.1 Material selection for micro-heater

Micro-heater material should have high resistivity and low thermal conductivity for efficient heating. The melting point must be significantly higher than the intended CNT growth temperature. For CMOS micro-heater design, metal interconnects or polysilicon layer are the available conductive layers. AMS 0.18  $\mu$ m process has aluminium and copper metal interconnects [8]. Aluminium has low melting point,

and both have low electrical and thermal resistivities, therefore, several alloys are considered. Alloys typically have higher electrical and thermal resistivities than pure metals. Alloys give better performance in this application, but require post-processing such as metal deposition and annealing.

An analytical model provides better perspective of the required material properties. Electrical power (P) dissipated for heating a small considered length ( $l_x$ ) of a micro-heater:

$$P = \frac{\rho \, I^2 l_x}{A} \tag{1}$$

where I is the current,  $\rho$  is the resistivity of the bridge material, and A is the cross-sectional area of the micro-heater.

Generated heat from resistive heating is considered to be transferred by thermal conduction due to negligible effects of convection and radiation. Following expression can be deduced from (1) and Fourier's law of thermal conduction:

$$dT = \frac{\rho I^2 l_x}{kA^2} dx \tag{2}$$

where k is the thermal conductivity of the material and dT/dx is the temperature gradient in the direction of heat flow.

The bridges have maximum temperature in the middle and temperature gradually reduces to the edges. An expression for the maximum micro-bridge temperature (*T*) can be derived by considering a length of  $l_x = l/2 - x$ , where *l* is the total bridge length. For this particular condition with an integration limit from the edge to the center of the bridge length, following expressions can be written:

$$\int_{T_0}^{T} dT = \frac{l^2 \rho}{k w^2 t^2} \int_0^{l/2} (\frac{l}{2} - x) \, dx \tag{3}$$

$$T = T_0 + \frac{l^2 l^2 \rho}{8w^2 t^2 k} \tag{4}$$

where  $T_0$  is ambient temperature and *w*, *t* are width & thickness of the bridge respectively.

Since the maximum temperature in (4) is proportional to the ratio,  $\rho/k$ , a higher value of this ratio results in more bridge temperature. Cupronickel alloy turned out to exhibit the best characteristics among the most feasible options. Nickel may be deposited on exposed Cu traces by electrodeposition, thus avoiding lithography in the required post-processing.



Figure 2: Bridge resistance and dominant power consumption factor for different cupronickel alloys

For optimum power (P), derived equation for maximum bridge temperature reveals the influential parameters. Equation (4) can be re-written in the following form:

$$P = \frac{8(T - T_0) \text{wtk}}{1} \tag{5}$$

Equation (5) reveals that the power consumption needed to obtain a given temperature difference depends on the product of cross-sectional area of the bridge and thermal conductivity of the bridge material. Therefore, this product is plotted in *Figure 2*, along with bridge resistance for different cupronickel compositions. Minimum width of the bridge should be equal to bridge thickness, while a higher width (20  $\mu$ m) has also been plotted. Considering both lower power consumption and higher bridge resistance, 70% copper and 30% nickel turns out to be the best alloy composition.

## 2.2 CMOS compatible surface temperature

Thermal resistance of the package has an influential impact on chip surface temperature. Bottom surface of chip package is assumed to be at room temperature, considering a heat sink is in contact. Calculating the thermal resistance [9], [10] and tuning the design accordingly is an effective way of reducing surface temperature. Lower thermal resistance of the package facilitates heat conduction although the micro-heater will consume more power to generate same bridge temperature. The micro-heaters can also have limited under-etching which creates large thermal gradient around them, resulting lower chip surface temperature. Therefore, partially underetched micro-heaters have also been designed in this work together with micro-heaters with no under-etching.

## 2.3 Thermo-mechanical stress

High bridge temperature may cause significant deformation for underetched designs. Buckling and stiction are two potential effects of thermo-mechanical stress, which can be minimized by decreasing the length of the microstructure.

Risk of buckling can be reduced by calculating the critical length for potential buckling of the partially suspended microheaters and keeping the under-etched length below the calculated values. The induced load on the micro-bridge due longitudinal thermal expansion ( $F_{TL}$ ) can be expressed by the following equation:

$$F_{TL} = \text{Ewt}\alpha\Delta T \tag{6}$$

where *E* is the Young's modulus,  $\alpha$  is linear thermal expansion co-efficient,  $\Delta T$  is change in temperature and *w*, *t* are width and thickness of the micro-heater respectively.

Critical buckling load for a rectangular beam with both ends fixed can be found from Euler's formula. Since the bridge load is caused by thermal stress, induced load due to thermal stress ( $F_{TL}$ ) is equal to the critical buckling load. Hence, following equation for critical buckling length ( $L_{cr}$ ) can be derived:

$$L_{cr} = \sqrt{\frac{\pi^2 t^2}{3\alpha\Delta T}} \tag{7}$$

## 2.4 Finite element analysis

Multiphysics FEM tool, ANSYS, has been used in this work to realize optimized micro-heater designs and performing necessary simulations. Several meshing techniques such as individual body sizing, refinement have been applied on the model to achieve efficient meshing with high mesh quality. Orthogonality and skewness of the meshes have been taken into account. Necessary FEM convergence tests have also been performed for model validation.

## 3 Results & Discussion

Thermal analysis of non-suspended Cu-Ni micro-heater and bridge temperature distribution of non-suspended polysilicon micro-heater are shown in *Figure 3* and *Figure 4* respectively. Micro-heater resistance should dominate in the microsystem, otherwise there will be high power losses in other regions of the circuit where resistance is higher. Cupronickel bridges have much lower resistance compared to polysilicon. The length of the cupronickel bridge is extended to 80  $\mu$ m to increase resistance. Bridge length can be further extended, but chip surface temperature and power consumption will also rise. In non-suspended polysilicon design, bridge length is kept short (30  $\mu$ m) since smaller length will make the chip surface less hot and thus decrease overall power requirement.



Figure 3: Thermal analysis of non-suspended Cu-Ni design



Figure 4: Temperature distribution of non-underetched polysilicon bridge across its length



Figure 5: Thermal analysis of partially suspended Cu-Ni design



Figure 6: Temperature distribution of partially underetched polysilicon bridge across its length

Thermal analysis of partially suspended Cu-Ni micro-heater and bridge temperature distribution of partially suspended polysilicon micro-heater are presented in *Figure 5* and *Figure 6* respectively. Bridge under-etching offers high thermal gradient around the micro-heater. Designed underetched lengths are smaller than the critical buckling length (around 15  $\mu$ m for Cu-Ni and 10  $\mu$ m for polysilicon) calculated from equation (7).

Table 1: Summary of the designed micro-heaters

Micro-heater Type	Non- suspended Cu-Ni	Non- suspended poly-Si	Partially suspended Cu-Ni	Partially suspended poly-Si
Required Power [mW]	220	10	80	6
Bridge Resistance [Ω]	35	6000	50	2400
Bridge Dimensions, l × w × t [µm]	80 × 1 × 0.86	$\begin{array}{c} 30 \times 0.4 \times \\ 0.2 \end{array}$	110 × 1 × 0.86	$\begin{array}{c} 30 \times 1 \times \\ 0.2 \end{array}$
Chip Surface Temperature [°C]	200	150	150	50

\*Chip surface temperature around 50 µm away from the micro-heater

A summary of the obtained results for the four micro-heater designs are presented in *Table-1*. The results are promising for practical implementation. Non-suspended bridge designs do not require post processing, although lower package thermal resistance is needed for these designs. It should be noted that non-suspended Cu-Ni design required 50% lower package thermal resistance to obtain CMOS compatible surface temperature. Polysilicon non-suspended design shows lower power consumption and lower surface temperature compared to cupronickel, hence, it is the clear choice in this design category. Partially suspended designs ensure low surface temperature and minimum power consumption, although carries risk of deformation during post processing.



Figure 7: Buckling analysis of fully suspended Cu-Ni design



Figure 8: Buckling analysis of fully suspended polysilicon design

Two fully suspended bridges have been designed to check the extent of potential deformation using thermo-mechanical analysis. The resultant deformation of the suspended cupronickel (*Figure 7*) and polysilicon (*Figure 8*) bridges are around 1  $\mu$ m. ANSYS eigenvalue buckling module predicts buckling on the basis of theoretical calculation. These results indicate that under-etching such long lengths carry high risks of buckling. Hence, there would be a trade-off between the amount of under-etching and mechanical strength of the micro-heater for the suspended designs.

## 4 Conclusion

The designed micro-heaters are able to generate high CNT growth temperature at low power, while keeping CMOS compatible temperature in the remaining regions of the

microsystem. Non-suspended polysilicon design is preferred if package thermal resistance requirement is met, otherwise partially underetched designs should be considered for the application. Mechanical strength of the underetched cupronickel and polysilicon micro-heaters need to be tested during post processing. Micro-heater with lower risk of deformation should be chosen among the partially underetched designs.

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SESSION 2

# **SESSION 2** Thermo-mechanical Reliability

# Location Resolved Transient Thermal Analysis to Investigate Crack Growth in Solder Joints

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## Abstract

An innovative new test method, location resolved transient thermal analysis (LrTTA), is developed based on transient thermal measurement (TTM). LrTTA uses several distinct diodes on a test chip to detect the thermal performance of interfaces and assemblies. The temperature is measured by the forward voltage time dependent at different locations and inhomogeneities in the interface, e.g. cracks, voids and thickness variations, can be resolved. This investigation is necessary for analysis of the failures in solder joints since the local temperature can be strongly vary due to local bad thermal contact. For first experimental application of the method, a silicon thermal test chip with four different located temperature diodes was employed and soldered on an Aluminium Insulated Metal Substrate (Al-IMS) and exposed to temperature cycles. Transient thermal measurements were performed directly after assembly and after specific temperature shock cycle numbers (-40°C/+125°C). After data processing the increase of the thermal impedance of each diode between the initial "0" cycles and "n" cycles was obtained and correlated with crack distribution in the solder joint by X-ray and scanning acoustic microscopy images. In addition, a finite element (FE) model was set up and used to analyze the solder joint with and without voids and also the crack propagation in the solder joint during temperature shock testing.

## 1 Introduction

TTM were first introduced in 1978 [1] for measuring the thermal resistance of an electrical device. Nowadays TTM is widely used in laboratories to measure the thermal resistance of electronic packages and it is also suited for reliability investigation, e.g. to investigate delamination of interfaces or crack development in solder joints [2] [3]. For detection of delamination and thin cracks it is a suited and sensitive method because the heat transfer is blocked and the thermal response of the system changes. On the one side, compared to other methods like scanning acoustic microscopy or X-ray microscopy the spatial resolution is usually limited because measurement signal relates to the average of the junction temperature. On the other side, with standard 2D X-ray delamination and cracks cannot be resolved. For example, in case of flux free soldering [4] bad wetting of the solder pads can't be observed. In contrast, TTM is able to detect bad wetted areas (see section 3.). Usually as best choice to detect



voids and delamination scanning acoustic microscopy is recommended. However, for complex devices with many material layers shadow effects are generated which reduce the resolution and the interpretation of signals becomes ambiguous.

In this paper it is investigated whether transient thermal analysis is able to spatial resolve crack propagation in die bond interfaces and more information in addition to scanning acoustic microscopy and X-ray can be gathered. The goal is to develop a local resolved transient thermal analysis (LrTTA). Therefore a thermal test chip with different diodes is used to investigate whether the transient thermal signals depend sufficient strong from the locations when cracks develop. Also the influence of tilting and voiding need to be taken into account and is addressed.

## 2 Methology

Before developing a dedicated test chip for LrTTA it was investigated whether a commercial available thermal test chip could be used. The thermal test chip TTC-1002-0100 from Thermal Engineering Associates was selected for this study. It is a semiconductor device that contains two thin metal film resistors as heaters and four different located diodes for temperature sensing (see figure 1). It has a size of 2.54mm x 2.54mm and is designed for die and wire bonding and therefore suited to investigate crack growth in a larger solder interface. The thermal test chip (TTC) was soldered on IMS. Two different IMS designs were manufactured. One was a standard Al-IMS design, so the TTC was soldered on the electrical layer and a dielectric layer was between electrical layer and metal core. In the second was a Co-IMS design where the dielectric layer was removed and the TTC was directly soldered onto the copper core. The two designs target to investigate the influence of the thermal pass, i.e. dielectric layer, on the potential spatial resolution.

Different solder material and processes were used: standard solder paste SAC305 soldered under nitrogen and flux-free solder paste soldered under activated atmosphere [4]. Afterwards the samples soldered with flux were cleaned before wire bonding. For the flux-free paste a cleaning step is not required. After die bonding the electrical contacts are formed by wire bonding, see figure 1 b).

An initial experiment was employed to investigate the special sensitivity: in one corner of the solder pad a thin layer of SMD adhesive was applied and cured to mimic a bad soldered area. Afterwards the TTCs were soldered and so a local insufficient wetting was obtained. Then the 4 diodes on the TTC-board were used to investigate the thermal performance at different locations, respectively. In addition, an optical profilometer was employed to obtain tilting information and X-ray images were used to detect voids in solder joints. This three distinct measurements were used as 0-hour inspection and were applied on the TTC-boards. Based on this 0-hour investigation the influence of tilting and voids of solder joint on the thermal performance could be investigated. Afterwards the samples were placed in the temperature shock chamber with a specified temperature range of -40°C to 125°C, based on AECQ101 standard [5]. After fixed temperature cycles the TTC-Boards were measured and analysed. This analysis targets to investigate crack propagation in the solder joint. In addition, a finite element Model (FEM) was established to analyse the transient temperature data.

IMS	2 removed dielectric		1 standard design	
design	layer			
Test	batch 1	Batch 2	batch 3	batch 4
Pre-		with thin		with thin
processing		SMD		SMD
		adhesive		adhesive
Soldering	flux free	flux free	standard	standard
process	paste	paste	soldering	soldering
			flux	flux

 Table 1: Experiment design (batch 1 and 2 are pre-test, batch 3 and

 4 are employed for investigation of LrTTA)

## 3 Experimental Analysis

## 3.1 Initial 0-Hour analyses

Batch 1 and 2, for which the dielectric layer was removed by a milling process to solder the devices directly on the copper core, revealed difficulties for soldering. Due to inaccuracy of milling processing of the manufacturer the depth of the cavities had large tolerances. In combination with the solder paste printing large tilting of the TTC after soldering occurred. In addition, the samples, soldered with flux free paste, proved the sensitivity of TTA for detection of delamination. After several temperature cycles the TTA measurement signal of all 4 diodes increased enormous although initial X-ray inspection had been OK. This, first unexpected, is explained by delamination due to bad wetting of the Ag surface finish of the TTC. It was revealed that the Ag surfaces is not reduced by the gaseous activator of the flux-free soldering. Therefore, the investigations of this paper focus on standard IMS design (with dielectric) and standard solder paste.

The sensitivity of the TTA for a bad soldered corner could be clearly proven (see Figure 2, a) and b)) comparing samples from batch 3 and 4. In the early time domain (1ms) the thermal signals of the diodes differ from each other. This phenomena was simulated using FEM and explained by the inhomogeneous temperature distribution in the silicon chip and location dependent heat spreading. In figure 2 a), the diode 3 in the middle measure the highest temperature after heating, therefore the total  $Z_{th}$  (9.45°C/W) is larger than the others. However during the cooling the middle area, where a sample in batch 3: standard soldering



Figure 2: For this initial analysis an image of X-Ray, measurement results of time depended  $Z_{th}$  and derivative of Zth from T3te-Measurement is given for samples in a) batch 3 and b) batch 4), respectively. The value near the diodes in a) represent the height of this corner (from board surface to the top surface of TTC). It was obtained by using a profilometer

on Thermal Investigations of ICs and Systems ))

#### Zth in [°C/W]

Diode	mean value	Standard deviation
1	8.89	0.21
2	9.24	0.21
3	9.72	0.23
4	8.76	0.24

#### Max. value of derivative of Zth in [°C/Ws]

Diode	mean value	Standard deviation
1	3.07	0.07
2	3.07	0.07
3	3.08	0.08
4	3.04	0.09

Table 2: summery of thermal measurement of batch 3.

diode 3 is located, has the maximum area for heat spreading in the silicon chip, so that the temperature changes quickly in the middle of thermal test chip, while the diode 2, located at the edge, has only half plane for heat spreading and diode 1&4, located in a corner have only a quarter plane. Accordingly, the curve of diode 2 raised slower than diode 3 and quicker than diode 1&4 from start to around 10ms. Which can also be explained, that the diodes cools down from different temperature to the same target temperature in the same time. Diode 1 and diode 4 almost overlap, since they are both located at a corner. The small difference can be explained by tilting. A higher thickness related to a larger thermal capacity and therefore the derivative curve of temperature sensor diode 4 raised slower than diode 1's in the time range from 3ms to 10ms. In section four, this sample was used as reference sample for validation and calibration of FEM model. The different curve shapes of the different diodes are reproduced in the transient thermal FE simulations (see section 4)

The calculated mean values with standard deviation of max.  $Z_{th}$  and max. derivative of  $Z_{th}$  (d( $Z_{th}$ )) are stated in table 2. The standard deviation within the groups varies from 0.21 to 0.24°C/W by max.  $Z_{th}$  and from 0.07 to 0.09°C/Ws by max. d( $Z_{th}$ ). The repeatability of the measurement equipment for the overall thermal impedance (junction to case) is 0.2°C/W. Root cause of the variations and measurement mistakes for the equipment and transient thermal analysis in general are reported in [6]. The algorithmic analysis can also be the main reason that causes inaccuracies in the data evaluation since the max. values were taken for each diode though they occur at different time (see figure 2 b)). Therefore, in the further the measured points will be fitted and described by a function.

For comparison, in figure 2 b) diode 1, where the SMD adhesive applied between copper pad and solder joint, is significantly larger than for the other diodes. Diode 1 (red curve) raises from beginning at 1ms faster than diode 4 and reaches a maximum value to 3.62°C/Ws by derivative curve





Figure 3: Detection of Crack propagation by using of LrTTA: Increase of thermal resistance of solder joint of a) good sample and b) bad sample in batch 3.

and 10.57°C/W by  $Z_{th}$ . The peak value of derivative of diode 2 gets close to diode 3, which can be explained from X-Ray image. The thermal signal of other diodes are also influenced by the voids and also by the solder joint thickness. The maximum of the peak height of the derivative Zth curve and the Zth curve itself was used to analyze crack growth.



## 3.2 Crack growth by Transient Thermal Analysis

Figure 4: comparison of d(Zth) signal of diodes of bad sample in figure 3 between 0 thermal cycle and after 500 thermal cycle. Red arrows indicate the time, where the red curve start to separate from the green curve. This can expression the locally earliest existent thermal interruption in solder joint from top to bottom.



Figure 5: scanning acoustic microscopy (SAM) inspection of bad sample in figure 3 of different plane: a) interface between chip and solder joint, b) internal cross section of solder joint. Their alignment are as same as X-Ray images in figure 3.

The total Z<sub>th</sub> values provide the overview of the thermal performance of the assemblies, however they are not sensitive to resolve solely the thermal resistance of the solder joint. Therefore, the maximum value of the derivative of the temperature rise is also investigated in dependence of temperature cycles. Figure 3 shows the total Zth and maximum values of  $d(Z_{th})$  for each diode after 25, 50, 100, 200, 400, 500 and 800 temperature cycles (800 cycle only for good samples). The initial growth at 25 cycles could be caused by early delamination at the solder interfaces or of the dielectric layer. Partly bad wetted areas or weak adhesion of layers would be initially in contact but separate after few stress cycles. After 100 cycles the maximum value of the derivative significantly increases of the depicted bad sample (large voids), this indicates the occurrence of cracks starting from the voids. After 500 cycles, the thermal signal of diode 4 and 3 of bad sample increased to 4.4°C/Ws, 3.8 °C/Ws by  $d(Z_{th})$  and 12.5°C/W, 11.6°C/W by  $Z_{th}$ , while the diodes of good sample changed slightly. The samples, which detect a



Figure 6: a) schematic description of top surface of TTC in simulation, small square with number are temperature sensor, brass long square represent metal resistor, i.e. heater. b) schematic cross section of TTC 3D Model with definition of Boundary conditions. c) simulated and experimental plot (for 0.2s measuring time) of derivation of thermal impedance.

max.  $d(Z_{th})$  smaller than 3.2°C/Ws after 500 cycles, were defined as good samples and they are further determined in thermal shock chamber. Right now the 800 thermal cycles were reached and an obvious increase of thermal signal of diode 1, 2, 4 were obtained and this shows the initiate of cracks starting from the outside of solder joint.

In addition, scanning acoustic microscopy has been employed to evidence the cracks in solder joint of bad sample in batch 3. Figure 4 a) shows images of scanning acoustic microscopy. It illustrates the interface between the chip and solder joint as well as issues in the solder joint after 500 cycle. Here it can be seen that the very bright areas that caused by a strong backscatter. This indicates that in these areas no connection between the chip and solder is present. Compare with X-Ray image of initial inspection, the white areas has been grown from voids to the other side and occupied more than 50% area on the solder joint as well as in the solder joint after 500 cycles. Due to the limit of the resolution of the SAM it is difficult to evaluate the cracks qualitative here. However, the transient thermal analysis is helpful. The figure 5 a) shows that air gaps right on the top of the solder joint are distributed under the diode 4 (bottom right), diode 3 (middle) and near by the diode 4 (upper left). Therefore the initial separation of d(Zth) curves from the 500 cycle to 0 cycle start very early by diode 4 (i.e. 1ms) and 3 (i.e. 2ms). Then the separation by diode 1 comes at 5ms and later on after 10ms the diode 2's signal start to increase. This effect can be detected within figure 5 b). The bright area in figure 5 b) are increased to the upper left corner, while the area by upper middle (diode 2) are relatively dark.

## 4 Finite Element Analysis

## 4.1 Finite Element Model



Figure 7: schematic description of temperature distribution of a) validated regular model and b) failure model like sample in batch 4. Upper left are temperature plot on chip surface, upper right are temperature plot under solder joint and temperature plot of cross section along the diagonal line (diode  $1 - diode \ 3 - diode \ 4$ ). The small squares with black point represent the non-contact area between solder joint and IMS.

A FE model (see figure 6) was set-up in Solid Works using the integrated Flo-EFD solver from Mentor Graphics to analyze the influence of different crack area in the solder joint on the transient temperature signal. Main target was to correlate the peak height of the maximum with the  $Z_{th}$ increase of the module and to investigate the potential crack which causes the effect. The thermal boundary conditions of the transient temperature measurements are reproduced in the model. The sample is connected by a thermal interface material (TIM), i.e. a heat pad, to a temperature controlled plate at 25°C. The model of the LED package is based on CAD data of thermal test chips. The heaters are thin metal layer and integrated in the chips. The diodes are presented as splinted square with temperature sensors on the TTC's top surface. The model size was about 2.7 million cells. The multiple, complex and thin electrical layers of the top surface of the thermal test chips are simplified to restrict the level of refinement and number of cells. The value of thermal conductivity and heat capacity of the materials were taken from literature. As thermal source a heat flux of P<sub>thermal</sub>=1.5W was applied on every heater. A boundary condition a constant temperature T=25°C was applied at the bottom of the temperature controlled plate.

The calculated temperature distribution from the steady state simulation is taken as initial temperature distribution for the transient simulation of the cooling down phase for which the heat load is switched to zero. From the time resolved cooling down simulation  $T_{diode}(t)$  is extracted. From the transient temperature curve the derivative of  $Z_{th}(t)$  are calculated and this was used as evaluation criterion for the calibration of the model (see figure 6 c)).

Temperature distribution of steady state simulations of validated regular model and a failure model are plotted in figure 7. The maximum temperature of regular model is located on the inside edge of heaters (see figure 7 a)), while the highest temperature of failure model is placed on the upper left corner of one heater, where the interruption of thermal transformation was applied under the solder joint, like sample in batch 4 (see figure 7 b)). The bottom surface of solder joint was equally divided into 100 small squares. Infinite contact resistances were applied on the small squares, where the voids (see figure 7 b)) and cracks (see figure 8) are present. By switching on and off the thermal resistance of the cells voids and cracks can be simulated and the transient



Figure 8: schematic description of crack propagation. Increase of crack area from outside to inside of the bottom of solder joint.

temperature signals reproduced by the simulation. By that voids and crack growth during temperature shock test shall be investigated. The bad soldered area as depicted in figure 2 can be reproduced.

The temperature is distributed symmetrical in the model without failure and temperature decreased from middle to the edges and from top to the bottom. The max. temperature differences are 2.74°C on chip surface and 1.74°C under solder joint. In the contrary, the max. temperature differences by failure model are 3.99°C on chip surface and especially 4.47°C under solder joint. Therefore the detected thermal resistance by diode 1 increased strongly and the difference of peak value of dZth between diode 1 and diode 4 turns into 0.44°C/Ws, while the difference by experiment (sample in batch 4) is 0.47°C/Ws. Due to the unsymmetrical heat dissipation the thermal signal of diode 2 was also influenced and its thermal resistance was increased.



Figure 9: (colour on line) increase of peak value of derivative of  $Z_{th}$  curve from 0% crack area to 96%, for each diode. The range until 50% crack area is magnified in the left loop window of figure 9. The experimental increase of peak value of each diode of good sample in batch 3 after 800 cycle are indicated and the corresponding crack area is estimated under the assumption of symmetric crack growth (Diode1: 32.5%, Diode 2: 35%, Diode 3: 46.5%, diode 4: 48.5%).

## 4.2 Solder Crack simulation

After qualitative matching of the experimental curves with the simulated ones in the relevant time domain, i.e. from start to 0.2s, for 0 temperature cycle conditions, the cracks were simulated by defining infinite thermal resistance on the bottom of the solder joint as the area of the crack from outer region of the solder joint toward the center of the package. This can be considered as the most severe condition: The heat transfer is assumed to be fully blocked by the crack area (see figure 8). It is also assumed that there is no voids or delaminations in the assembly after soldering, i.e. the initial growth after 25 cycle was not considered.

The crack growth was simulated and the max. peak value of derivative of  $Z_{th}$  were calculated and plotted in figure 9. Because of the different location of the diodes, the growth of their thermal signal is distinct. During the increase of the crack area the thermal signals are increased exponentially. Diode 1's and diode 4's signal are overlapping and raising quickly from beginning compared to diode 2 and 3 which raise slowly. After 40% crack area the crack reaches the position of diode 2 and the thermal signal of diode 2 also increases faster, almost parallel to the diode 1&4 till 76%

crack area. Since then it increased faster than diode 1&4 and get close to them at 96% crack area. The thermal signal of diode 3 increases slowly because the die remains thermally connected in its center. The max. peak of the good sample in batch 3 by 800 cycle was used to calculate the increase of the dZth and the corresponding crack area in figure 9 assuming the symetric crack growth. The crack area obtained of diodes are differentl (see Fig. 9). This can be explained by deviation of the crack area and location will be obtained by fitting the simulated change of the  $Z_{th}(t)$  and its derivation  $dZ_{th}(t)$  of all diodes to the experimental data.

## 5 Conclusion

LrTTA is a sensitive tool to detect solder cracks. The maximum of the peak of the  $d(Z_{th})$  curve indicates the thermal degradation and differ with different location significantly. Therefore the LrTTA can be used directly after soldering to detect the voids and delamations in solder joint locally. LrTTA can also be employed to observe crack propagation in solder joints.

The next step is to access and analyze cross sections to investigate the relationship between crack length and temperature cycle numbers..Crack growth observed with LrTTA will be compared and benchmarked in more detail with results obtained by SAM.Afterwards, the LrTTA will be employed to evaluate the reliability of die bonds using different bonding processes and bonding materials.

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## Collapse of a Liquid Solder Bump under Load

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## Abstract

In this work the collapse of a solder bump as a result of the weight load of a chip or a package is analysed. A new expression is derived for the opposing bump force that carries the load. Its validity is checked on known solutions. Calculated spring constant and hydrostatic pressure are compared between the new force based approach and the more conventional approach based on increase of free surface. It is shown that for a spheroid bump shape, the results are qualitatively similar but not quantitatively the same. It turns out that the spheroid bump shape does not fully satisfy the Young Laplace (YLP) equation. The new force expression is used to develop an alternative bump shape which satisfies the YLP equation better. It is expected that the new force expression and the new alternative collapsed contour will contribute to better reliability assessment of solder bump interconnects.

## 1 Introduction

BGAs, flip chips and flip chips inside BGAs are very much present in all electronics we use today. They use arrays of small solder balls as interconnect to a motherboard and the height and shape of the solder balls are factors in the reliability of the interconnect. During soldering, the weight of IC or the IC package flattens the liquid bump. When the load is removed, surface tension restores the original shape and height. In consequence, the bump can be considered as a nonlinear spring [1]. For small deformations, the nonlinear spring can be linearized, and the force constant or spring constant of the bump is defined as the ratio of loading force to bump collapse.

Conventionally, the effect of surface tension is described in terms of bump deformation enlarging the free surface, which requires work to be done, which is stored as energy, and the force constant or spring constant of the bump is given by the second derivative of the surface energy to the collapse displacement. The first published work on enlargement of the solder bump surface was published in the early nineties and was based on numerical modelling [2]. It was followed by Brakke's Surface Evolver [3] and further work on bump shapes in relation to self-alignment in relation to opto-electrical components [4, 5].

In the present work we will show that in contrast to the surface energy approach, the force constant can also be derived as the first derivative of the bump force opposing the load to the collapse displacement, and that this bump force can be derived from the free body diagram and the equilibrium of forces for an axisymmetric liquid bump under load. We show that for a spheroid bump contour the two different methods agree qualitatively, but not quantitatively. However, the spheroid contour does not completely satisfy the YLP equation governing surface tension and hence can only be considered to be an approximate solution to the problem of liquid bump shape under load. The insight that the equilibrium of forces implies that bump force described in the new expression must be constant over the bump height, is used to derive a new shape model, which is shown to be closer to a true solution of the Young Laplace equation.

The work described in this paper builds on earlier results [6,7,8], It has provided new insights and enabled making a more accurate but still analytical model for bumps in the liquid state, which is expected to contribute to solder bump interconnect reliability in future.

## 2 Model

The shape of a liquid bump is governed by the Young Laplace equation (YLP). This equation can be either derived from minimization of the work to create free surface or through static equilibrium of surface tension and hydrostatic pressure. For a liquid, the surface energy density  $\gamma$  [J/m<sup>2</sup>] is equal to the surface tension  $\gamma$  [N/m]. The Young Laplace equation reads:

$$P(z) = \gamma \left( \frac{1}{R_1(z)} + \frac{1}{R_2(z)} \right)$$
(1)

P(z) is the overpressure inside the liquid, and  $R_l(z)$  and  $R_2(z)$  are the principal radii of curvature of the surface. Both  $R_l(z)$ 



Figure 1: Principal radii of curvature

and  $R_2(z)$  lie along the surface normal through the tangent point. For the axisymmetric surface r(z) shown in Figure 1, the intersection curve associated with  $R_1(z)$  lies in the plane of the paper and the intersection curve associated with  $R_2(z)$  lies in the plane perpendicular to the paper.  $R_1$  and  $R_2$  are shown in different tangent points for reasons of visual clarity.

## **3** Surface energy approach

It is assumed throughout this paper that the solder bumps are so small that the weight of the solder itself can be neglected. The shape of the liquid solder bump is the shape where the minimum free surface is created. The free solder shape is a sphere, as this has the smallest surface area for a given volume. In case the bump is contained between bond pads, the surface is the sphere segment bounded by the bond pads.

When loaded, the liquid bump acts as a spring. For small displacements, the spring can be linearized with a constant force constant *c*. The bump collapse  $\Delta$  is proportional to the loading force *F*.

$$F = -c.\Delta \tag{2}$$

The energy *E* stored in the spring is given by:

$$E = \frac{1}{2} c \Delta^2 \tag{3}$$

This stored energy equals the work W done to create the additional the free surface S:

$$E = \int_0^{\Delta} dW(\Delta) = \gamma \int_0^{\Delta} dS(\Delta)$$
(4)

It follows that c can be derived from the stored energy through taking the second derivative to the bump collapse.

$$c = \left(\frac{d^2 E(\Delta)}{d\Delta^2}\right)_{\Delta=0} = \gamma \left(\frac{d^2 S(\Delta)}{d\Delta^2}\right)_{\Delta=0}$$
(5)

## 4 Force approach

Figure 2a shows a liquid bump deformed under a mechanical load. The free body diagram of the part outlined by the dotted contour is shown in Figure 2b.



Figure 2: Loaded bump (a) and free body diagram of the system inside the dotted contour (b)

In line with the conventions for a free body diagram, only the forces that act directly on the contour and the body forces (e.g. weight load of the IC) on the bodies inside the contour are to be considered. For the free body system inside the contour to be at rest, the forces must be in equilibrium, that is the resulting force must be 0. For the system under consideration the loads are the load *F* from the weight of the package, the force  $F_p$  resulting from hydrostatic pressure on the cut cross-sectional area at coordinate *z*, and the force  $F_\gamma$ 

resulting from surface tension on the cut circumference of the liquid bump at coordinate *z*.

The hydrostatic pressure P(z) is given by (1) The force exerted by the hydrostatic pressure is given by:

$$F_p = \pi r(z)^2 P = \pi r(z)^2 \gamma \left(\frac{1}{R_1(z)} + \frac{1}{R_2(z)}\right)$$
(6)

Mechanically speaking, surface tension at the cut circumference is a membrane line stress. It can only be tensile, and it can only act in the plane of the surface. The resulting line force at the circumference of the cut surface is tensile, tangent to the surface and has magnitude of  $\gamma$  times the length of the cut line. In the present axisymmetric case, all non-vertical components of the resulting force cancel out and the resultant vertical force is given by:

$$F_{\gamma} = 2 \pi \gamma r(z) \sin(\alpha) \tag{7}$$

It follows from figure 1 that the following relation holds for the tangent angle  $\alpha$ :

$$\sin(\alpha) = \frac{r(z)}{R_2(z)} \tag{8}$$

Substitution into (7) yields:

$$F_{\gamma} = 2 \pi \gamma \frac{r(z)^2}{R_2(z)}$$
 (9)

Drawing up the force balance in vertical direction results in:

$$-F + F_p - F_\gamma = 0 \tag{10}$$

$$F = \pi \gamma r(z)^2 \left( \frac{1}{R_1(z)} - \frac{1}{R_2(z)} \right)$$
(11)

Since the lower edge of the free body diagram contour made a cut at an arbitrary value of z, it follows that (11) is valid at each and every value of z in the bump and that the right hand side of the equation defines the bump force opposing the load. Since the load itself is a constant, and the expression is valid at arbitrary z in the bump, it follows that the right hand side of (11), or the force opposing the load, also is constant over the height of the bump. Thus, for a liquid bump under load, it follows from equilibrium of forces in the z direction that like the pressure is conserved over the vertical direction, so is the force opposing the load given by (11).

Expression (11) is easily verified on the known exact solutions for the Young-Laplace equation:

- For the sphere,  $R_1 \equiv R_2 \equiv R$ , and it follows that  $F \equiv 0$ . In other words, the sphere (or sphere segment) is the solution for the unloaded bump.
- For the vertical cylinder,  $R_1 \equiv \infty$ ,  $R_2 \equiv R$ , and it follows that  $F = -\pi \gamma R$ .
- For the hyperbolic cosine contour with p = hcosh(1), in which the hydrostatic pressure P=0,  $R_1 = -R_2$  and  $F = -2 \pi \gamma h$ .

#### 5 Force constant for spheroid contour

When the solder bump is loaded, the sphere segment will be flattened. For convenience this flattened shape is often approximated as a spheroid, truncated at the top and at the bottom by the solder pads. This spheroidal contour is an approximation because it is not a true solution of the Young Laplace equation, as will be shown later. The flattened solder bump is shown in Figure 3.



Figure 3: The compressed bump represented as a spheroid segment.

We consider a solder bump, axisymmetric around the z axis, with flattened height H=2h, truncated at the top and at the bottom by the solder pads with radius p. Using a cylindrical coordinate system (r, z) and shape factor a the contour of the free surface is then given by:

$$r(z) = \sqrt{p^2 + a(h^2 - z^2)}$$
(12)

Starting from an un-deformed spherical (a=1) bump with undeformed height K=2k, one can show from conservation of volume that the shape factor *a* of the deformed bump is given by

$$a = \frac{2 k^3 + 3 p^2 (k - h)}{2 h^3}$$
(13)

Surface approach: The free surface area associated with the contour (12) is obtained by taking the surface area of revolution around the *z* axis. Subsequent differentiation by the collapse displacement  $\Delta = H-K = 2h-2k$  leads to the following expression for the force constant  $c_c$ :

$$c_c = \frac{4\pi\gamma(2j^2+1)(30j^4+12j^2+1)}{5(4j^2+1)^{3/2}}$$
(14)

This shows that the force constant is solely dependent on the surface energy density  $\gamma$  and the bump ratio j. The ratio j is defined as the ratio of bond pad radius to initial bump height: j=p/K.

*Force approach*: The radii of curvature in an axisymmetric coordinate system are

$$R_1 = \frac{(1+r'^2)^{3/2}}{-r''} \tag{15}$$

$$R_2 = r(1 + r^2)^{1/2} \tag{16}$$

With the notation  $r' = \frac{dr}{dz}$  and  $r'' = \frac{d^2r}{dz^2}$ . Direct application of (12) into (15), (16) and (11) yields.

$$F(z) = \gamma \pi \frac{(p^2 + a h^2 - a z^2)^2 (a - 1)}{(p^2 + a h^2 - a z^2 + a^2 z^2)^{3/2}}$$
(17)

Using (12) this simplifies to:

$$F(z) = \gamma \pi \frac{r^4 (a-1)}{(r^2 + a^2 z^2)^{3/2}}$$
(18)

At the equator z=0, which yields:

$$F(0) = \gamma \pi (a-1)(p^2 + a h^2)^{1/2}$$
(19)

$$c_0 = \frac{3 \gamma \pi (4 j^2 + 1)^{1/2} (1 + 2 j^2)}{2}$$
(20)

At the bond pad z=h, which yields:

$$F(h) = \gamma \pi \frac{(a-1) p^4}{(p^2 + a^2 h^2)^{3/2}}$$
(21)

$$c_h = \frac{24 \,\gamma \,\pi \,\, j^4 \,(\,1 + 2 \,j^2)}{(4 \,j^2 + 1)^{\frac{3}{2}}} \tag{22}$$

Figure 4 compares  $c_0$ ,  $c_h$  and  $c_c$  as a function of j, the ratio of bond pad radius to the unloaded bump height. The results of the force approach and the results of the surface energy approach match qualitatively but not quantitatively. However, we also observe that  $c_0$  differs from  $c_h$  hence the force is not



Figure 4: Force constants for a spheroid shape model: as derived from the surface energy  $(c_c)$  and from the bump force at the location of the bond pad  $(c_h)$  and at the location of the equator  $(c_0)$ .

constant over the height of the bump, as it should have been. We attribute this to the fact that the spheroid bump is not a true solution to the YLP equation, hence the spheroid shape is not fully realistic.
#### 6 An alternative analytical contour

Extensive trials have yielded that a good alternative contour is found by the linear combination of a spheroid and a cylinder. The contour will read:

$$r_a(z) = (1+\beta)\sqrt{p^2 + a(h^2 - z^2)} - \beta p$$
(23)

It is easily verified that this contour touches upon the edges of the contact pad with radius p:  $r_a(h)=p$ . The parameters aand  $\beta$  and are a priori unknown and are to be solved for, as is the collapsed height h. Integration of the contour over r and zyields the volume  $V_a(a, \beta, h)$ . With known  $V_0$  as the undeformed volume of the bump, conservation of volume yields a first relation for a,  $\beta$  and h

$$V_a(a,\beta,h) - V_0 = 0 (24)$$

Substituting the alternative contour (23) into the expressions for the principal radii of curvature (15) and (16), and subsequently into (11) yields the general expression for the force opposing the load  $F_a(a, \beta, z)$ . Since this is conserved over the bump height, the force at the equator,  $F_a(a, \beta, 0)$  equals the force at the bond pad,  $F_a(a, \beta, h)$ .

$$F_a(a, \beta, 0) - F_a(a, \beta, h) = 0$$
(25)

h is connected to the bump collapse  $\Delta$ 

$$h = \frac{1}{2}(K + \Delta) \tag{26}$$

Finally, the magnitude of the force is determined by the weight load from the package mass M in gravity g

$$F_a(a, \beta, 0) - M g = 0$$
 (27)

The system of equations is solved for a,  $\beta$  and h, using a commercial symbolic math code.

An example calculation was performed with the following parameters:  $p=110 \ \mu m$ ,  $V_0$  from a spherical solder ball of diameter =300  $\mu m$ , g=9.81 m/s<sup>2</sup>,  $\gamma$ =0.4 J/m<sup>2</sup>, M=5 mg. This yields a value for K of 221.74  $\mu m$  in the unloaded case. After the mass M is placed, the bump will collapse. Numerical solution of the set of equations for the alternative contour yields: a = 2.516285,  $\beta = -0.4007354$  and the total collapse  $\Delta$  equals -15.10  $\mu m$ , which aligns well with values expected from experience.

Figure 5 shows the comparison of the hydrostatic pressure versus the height between the alternative contour and the spheroid bump for these case parameters. For a true solution to the YLP equation the hydrostatic pressure is constant over the height of the bump. In contrast, Figure 5 shows that for the spheroid contour the hydrostatic pressure depends strongly on z but the alternative contour has almost no such dependency. This proves that the alternative contour is a more realistic approximation to the true bump shape.

#### 7 The bump force for the alternative contour

By substituting the spheroid contour (12) into the alternative contour (23) one can rewrite the latter as



*Figure 5: The hydrostatic pressure over the bump contour for a collapsed bump loaded with 5 mg.* 

$$r_a(z) = (1 + \beta) r_s(z) - \beta p$$
 (28)

Where  $r_s$  is now used for the expression for the spheroid contour. Subsequent substitution into (11) yields:

$$F_{z}(z) = \gamma \pi r_{a}(z) *$$

$$\frac{((1+\beta) a r_{s}(0)^{2} r_{a}(z) - r_{s}(z)(r_{s}(z)^{2} + u^{2}))}{(r_{c}(z)^{2} + u^{2})^{3/2}}$$
(29)

Where

$$u = (1 + \beta) a z \tag{30}$$

Figure 6 shows the bump force over the height for the alternative contour in the example. For comparison we have added the force as obtained for the spheroid contour as well. Figure 6 shows that the calculated bump force is far from constant for the spheroid contour. There is a factor four variation between the value at the equator and at the bond pads. The alternative contour does not yield a perfectly straight horizontal line, but it comes a lot closer. This aligns with the earlier observation, based on the hydrostatic pressure, that the alternative contour is more a realistic bump shape. In addition it shows that the bump force is a more sensitive measure for the quality of the bump shape approximation.



*Figure 6: The calculated force over the bump height for a collapsed bump loaded with 5 mg* 

#### 8 Discussion

In the entire work it has been assumed that solder gravity can be neglected. It is generally accepted that solder gravity becomes an important factor at 2.2 mm ball diameter. The solder balls that we are investigating are 300  $\mu$ m in diameter and typically have a height of 200  $\mu$ m when reflowed, validating this assumption.

In addition, the spring was linearized. Figure 7 shows the bump force for the spheroid and for the alternative contour as a function of collapse displacement. For the sake of comparison the line for a linear spring is added as well. It can be seen that the displacements stay below 10% of the bump height (calculated as 221 µm for this example), therefore the linearization of the non-linear spring, which is valid for small displacements, is allowed. The energy stored in the spring is  $\int F(z)dz$ . This is the area below the F(z) curve in Figure 7. Since the bump force for the alternative contour is smaller than the one for the spheroid, the area below the curve is also smaller, which demonstrates that less energy is stored in the



Figure 7 Force versus collapse displacement for the spheroid and the alternative contour.

case of the alternative contour as compared to the spheroid. This is an additional indication that the alternative contour is closer to a true solution of the Young Laplace equation.

#### 9 Summary and conclusions

In this paper we have shown that the force constant or spring constant of a liquid bump under load can be derived in the conventional way as the second derivative of the surface to the collapse displacement from the increase of free surface as a result of bump collapse, and that for a spheroid bump shape the spring constant turns out to be a function only of the surface energy  $\gamma$  and the geometrical ratio of pad radius to unloaded bump height, j.

Alternatively the spring constant can be derived as the first derivative of the bump force opposing the load. Analysis of the forces involved and applying force equilibrium shows that the opposing force in the bump equals the product of the cross-sectional area, surface tension, and the difference of the inverse radii of curvature:

$$F = \pi \gamma r(z)^2 \left( \frac{1}{R_1(z)} - \frac{1}{R_2(z)} \right)$$
(11)

The bump force is constant over the height of the bump, just as the hydrostatic pressure. The validity of this newly derived force equation was verified on known solutions of the YLP equation.

The force constant for a spheroid contour was derived by the surface energy method and the alternative force method. Comparison shows good quantitative but poor qualitative agreement. However, the comparison also indicates that for this contour the force over the height of the bump is not constant and that the spheroid contour is less realistic even for small eccentricity. The results from the spheroidal model and the improved method for deriving force constants from the bump force F(z) have inspired us to develop an improved, alternative, bump contour which can be used for more accurate collapse calculation. It is shown that both the hydrostatic pressure and the bump force for this model are much more constant over the height of the bump and that the stored surface energy is smaller, hence this contour is a better approximation to the true bump shape.

In conclusion a new equation for the bump force opposing the load has been derived from equilibrium of forces. The force constant of the bump can be derived as the first derivative of the bump force to the collapse displacement. This is an advantage as this procedure is less mathematically cumbersome as compared to the conventional surface energy approach. The new insights enabled making a more accurate but still analytical model for collapsed bumps in the liquid state.

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#### **Determination of Bond Wire Failure Probabilities in Microelectronic Packages**

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#### Abstract

This work deals with the computation of industry-relevant bond wire failure probabilities in microelectronic packages. Under operating conditions, a package is subject to Joule heating that can lead to electrothermally induced failures. Manufacturing tolerances result, e.g., in uncertain bond wire geometries that often induce very small failure probabilities requiring a high number of Monte Carlo (MC) samples to be computed. Therefore, a hybrid MC sampling scheme that combines the use of an expensive computer model with a cheap surrogate is used. The fraction of surrogate evaluations is maximized using an iterative procedure, yielding accurate results at reduced cost. Moreover, the scheme is non-intrusive, i.e., existing code can be reused. The algorithm is used to compute the failure probability for an example package and the computational savings are assessed by performing a surrogate efficiency study.

#### 1 Introduction

In nowadays' micro- and nanoelectronic applications, constant downscaling leads to increasing power densities. Arising thermal problems can trigger the degeneration of materials, performance restrictions or even system failure. Typically, thermal designers use guidelines to avoid thermal problems in their designs. This may lead to inaccurate modeling and overdesign. Additionally, uncertainties in material and geometrical properties stemming from tolerances in the manufacturing process may result in unexpected behavior.

For a more accurate prediction of the manufactured functionality, numerical simulations are becoming increasingly popular. Using relevant (uncertain) parameters as inputs, uncertainty quantification techniques help to understand the influence of manufacturing tolerances on the devices' performance. The evaluation of failure probabilities becomes possible, yet the computation of very small failure probabilities is numerically challenging. These small probabilities inevitably occur in the context of a six sigma design goal.

One possible approach to compute failure probabilities was first presented by Li and Xiu in [1] and uses combined Monte Carlo sampling of the original computational model with a polynomial approximation. The idea is to use the computationally cheaper but less accurate polynomial model as long as a sample far away from the failure region is considered. Once a sample falls within the vicinity of the failure region, the original expensive model is used to ensure accurate results. The threshold, deciding which model needs to be evaluated, is determined iteratively as outlined in [1]. A possible extension to additionally compute rare failure probabilities, i.e., below  $10^{-5}$ , can be realized by, e.g., the usage of importance sampling as presented in [2]. To estimate the threshold a posteriori by using an adjoint error estimator, see [3].

In this paper, the method presented in [1] is applied to compute bond wire failure probabilities in a microelectronic chip package as shown in Fig. 1. The paper is organized as follows. First, Section 2 introduces the underlying electrothermal problem in the continuous and the discrete setting including the bond wire contribution. Then, different approaches to compute the failure probability are presented in Section 3, before the numerical results are given in Section 4. Finally, Section 5 concludes the paper.

#### 2 Electrothermal Problem

One of the main reasons why bond wires are subject to failure is because of the Joule heating effects that stem from applied currents. For the evaluation of failure probabilities, it is thus required to analyze the coupled electrothermal system.

#### 2.1 Continuous Setting

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Disregarding transient effects in the electrical problem, we consider the coupling of the electrokinetic problem with the transient heat equation. With the computational domain  $\Omega$ ,  $\vec{r} \in \Omega$  and  $t \in I = (0, t_{end}]$  being the coordinates in space and time, respectively, the continuous setting is given by

$$-\nabla \cdot (\sigma(\vec{r},T)\nabla \varphi(\vec{r},t)) = 0, \qquad (1a)$$

$$p(\vec{r})c(\vec{r})\dot{T}(\vec{r},t) - \nabla \cdot (\lambda(\vec{r},T)\nabla T(\vec{r},t)) = Q(\varphi,T), \quad (1b)$$



Figure 1: Microelectronic chip package with bond wires. For the study presented here, the geometry of bond wires 1 and 2 (red) is modeled to be subject to uncertainty while the parameters of the other wires are assumed to be known exactly.

with appropiate initial and boundary conditions. Note that the time dependence of the electric potential  $\varphi$  is induced by the coupling with the transient heat equation. In (1b), the Joule loss coupling term  $Q_{\rm el} = \sigma |\nabla \varphi|^2$  is incorporated as a contribution to the heat power density Q. The material parameters are given by the electrical conductivity  $\sigma$ , the volumetric heat capacity  $\rho c$  and the thermal conductivity  $\lambda$ . While we neglect the temperature dependence of  $\rho$  and c, we model  $\sigma$  and  $\lambda$  to be functions of temperature. The contribution of the bond wires (cf. Fig. 1) is omitted for now and will be included in the discrete setting in Section 2.3.

#### 2.2 Discrete Setting

For the solution of (1), a numerical scheme is required. Here, we choose the Finite Integration Technique (FIT) [4, 5] on a pair of hexahedral meshes to obtain the semi-discrete system

$$\begin{split} &-\widetilde{S}M_{\sigma}(T)G\Phi=0,\\ &M_{\rho c}\dot{T}-\widetilde{S}M_{\lambda}(T)GT=Q(\Phi,T). \end{split}$$

The time-dependent degrees of freedom are the potential vector  $\Phi$  and the temperature vector **T**. In analogy to the continuous problem, the Joule heating contribution  $\mathbf{Q}_{el}$  adds to the vector of source heat powers  $\mathbf{Q}$ . The materials are given by the electric conductance matrix  $\mathbf{M}_{\sigma}$  and the thermal capacitance and conductance matrices  $\mathbf{M}_{\rho c}$  and  $\mathbf{M}_{\lambda}$ , respectively. The dual face to volume incidence matrix  $\widetilde{\mathbf{S}}$  and the primary node to edge incidence matrix  $\mathbf{G} = -\widetilde{\mathbf{S}}^{\top}$  are the discrete analogons to the continuous divergence and gradient operator, respectively. Subsequent time discretization is done using the implicit Euler method together with a fractional step splitting for the algebraic equation.

#### 2.3 Bond Wire Contribution

Since the extent of bond wires is very small compared to the remaining feature sizes in a chip package, the wires are not resolved in the mesh but rather modeled by a lumped element approach. To include the wire contribution in the discrete setting, a stamping approach as outlined in [6] is applied. Then, the discrete system including  $N^{\text{bw}}$  bond wires reads

$$\begin{split} \widetilde{\mathbf{S}}\mathbf{M}_{\sigma}(\mathbf{T})\widetilde{\mathbf{S}}^{\top}\Phi + \sum_{j=1}^{N^{\text{bw}}}\mathbf{P}_{j}G_{\text{el}}^{\text{bw},j}(T^{\text{bw},j})\mathbf{P}_{j}^{\top}\Phi &= \mathbf{0}, \\ \mathbf{M}_{\rho c}\dot{\mathbf{T}} + \widetilde{\mathbf{S}}\mathbf{M}_{\lambda}(\mathbf{T})\widetilde{\mathbf{S}}^{\top}\mathbf{T} + \sum_{j=1}^{N^{\text{bw}}}\mathbf{P}_{j}G_{\text{th}}^{\text{bw},j}(T^{\text{bw},j})\mathbf{P}_{j}^{\top}\mathbf{T} &= \hat{\mathbf{Q}}(\Phi,\mathbf{T}), \end{split}$$

where  $\mathbf{P}_j$  is the incidence vector between the bond wire contacts and the dual volumes, containing entries 0, -1 and 1. The temperature  $T^{\mathrm{bw},j} = \mathbf{X}_j^{\top} \mathbf{T}$  of a bond wire, with  $\mathbf{X}_j = \frac{1}{2} |\mathbf{P}_j|$ , where  $|\cdot|$  refers to the vector of absolute values, is defined as the average value of the temperature at its end points. The source term  $\hat{\mathbf{Q}}$  comprises Joule heating of both the distributed part  $\mathbf{Q}_{\mathrm{el}}$  and bond wire part as

$$\hat{\mathbf{Q}}(\Phi, \mathbf{T}) = \mathbf{Q}_{\text{el}}(\Phi, \mathbf{T}) + \sum_{j=1}^{N^{\text{bw}}} \mathbf{X}_j G_{\text{el}}^{\text{bw}, j} (T^{\text{bw}, j}) (\Phi^\top \mathbf{P}_j)^2,$$

with the electrical and thermal conductance of bond wire *j* given by  $G_{el}^{bw,j}$  and  $G_{th}^{bw,j}$ , respectively. Here,  $\mathbf{X}_j$  distributes the heat generated in the bond wire to the dual volumes to which the bond wire is connected. In this paper, we model each bond wire with a length  $l_j$  and a uniform cross section  $A_j$ . Therefore, the conductance of wire *j* reads  $G_{\{el,th\}}^{bw,j} = \{\sigma, \lambda\}A_j/l_j$ .

#### **3** Failure Probability

Failures occurring in technological applications due to manufacturing tolerances (resulting in, e.g., uncertain geometries) are of stochastical nature. In the framework of a microelectronic chip package with bond wires connecting the chip with its package, we define a failure as the fusing or breaking of a bond wire. We thereby assume that failures originate predominantly from the bond wire and thus neglect any other possible sources for failure. The considered uncertain bond wire geometries shall be modeled by the realization **y** of a random variable in the observation space  $\Gamma \subset \mathbb{R}^N$ . Then, the electric and thermal conductance  $G_{\{el,th\}}^{bw,j}$  depends on **y** and so do  $\Phi$  and **T**, implicitly, through the electrothermal problem.

The evaluation of the associated failure probabilities is divided into the following steps. We give a mathematical discussion of the failure of a single bond wire and present methods to compute the associated failure probability. Afterwards, system failure probability is defined based on the individual bond wire failure probabilities.

#### 3.1 Bond Wire Failure

A single bond wire failure induced by stress, electromigration or other reasons shall be modeled by a critical temperature  $T_{cr}$  that we assume to be equal for all here considered wires. Then, a failure occurs when the maximum temperature of the wire exceeds the critical temperature  $T_{cr}$  at any instant in time, given by

$$\max_{t \in I} T^{\mathrm{bw}}(t, \mathbf{y}) > T_{\mathrm{cr}},\tag{4}$$

where the wire's temperature  $T^{\text{bw}}$  now depends on **y**. Following [1], the failure shall be modeled with the help of a performance function  $g : \mathbb{R}^N \to \mathbb{R}$  that describes a failure of the wire when g < 0. A possible choice for this function is

$$g(\mathbf{y}) = -\max_{t \in I} T^{\mathrm{bw}}(t, \mathbf{y}) + T_{\mathrm{cr}}.$$

Those points of  $\Gamma$  resulting in a negative performance function constitute the failure region, denoted as  $\Gamma_F$ . For the case of two uncertain input variables  $y_1$  and  $y_2$ , Fig. 2 depicts schematically the rectangular observation space  $\Gamma$  and its subspace  $\Gamma_F$ , separated by the solid line. With the definition of the characteristic function

$$\mathbb{1}_{\Gamma_F}(\mathbf{y}) = \begin{cases} 1, & \mathbf{y} \in \Gamma_F, \\ 0, & \mathbf{y} \notin \Gamma_F, \end{cases}$$

the failure probability is given by

$$P_{\mathrm{F}} = \int_{\Gamma} \mathbb{1}_{\Gamma_{\mathrm{F}}}(\mathbf{y}) \,\rho\left(\mathbf{y}\right) \,\mathrm{d}\mathbf{y}.$$



Figure 2: Separation of the domain  $\Gamma$  into a region where the full model is evaluated (gray) and where the surrogate model is evaluated (white). Full model evaluations within the gray area are triggered by the threshold through  $|g^{sur}| = \delta$ .

#### 3.2 Sampling Scheme

Commonly, failure probabilities are approximated using Monte Carlo sampling yielding

$$P_{\mathrm{F}} \approx \frac{1}{M} \sum_{i=1}^{M} \mathbb{1}_{\Gamma_{\mathrm{F}}}(\mathbf{y}^{i})$$

with *M* being the number of Monte Carlo samples and  $\mathbf{y}^i$  a random sample of  $\mathbf{y}$  drawn according to the probability distribution  $\rho$ . The complexity of this approach highly depends on the cost to evaluate  $\mathbb{1}_{\Gamma_F}(\mathbf{y}^i)$ .

#### 3.3 Surrogate Model

The problem for the sampling scheme described in the previous section is that for each sample, the evaluation of g requires the solution of a system of PDEs, i.e., system (1). Therefore, especially for small failure probabilities, a large number of samples M is required and an efficient surrogate model is necessary.

A class of polynomial surrogate models, referred to as generalized polynomial chaos, was proposed in [7]. These global polynomials are at the core of spectral stochastic methods, such as the stochastic Galerkin or collocation method. Here, the non-intrusive collocation procedure presented in [8] is adopted, as it is readily applicable to the present nonlinear, transient and coupled problem. In the simplest case of tensor grid collocation, with collocation points  $\hat{y}^m$ ,  $m = 1, \dots, (p+1)^N$ , with polynomial degree p, the model is approximated as

$$g(\mathbf{y}) pprox g^{\mathrm{sur}}(\mathbf{y}) = \sum_{m=1}^{(p+1)^N} g(\hat{\mathbf{y}}^m) L_m(\mathbf{y}),$$

where  $L_m$  are multivariate Lagrange polynomials. However, when a high number of uncertain input parameters is involved, more sophisticated methods such as sparse grids [9] and low-rank tensor approximations [10] are used.

In the following, the failure region evaluated with  $g^{\text{sur}}$  instead of g is called  $\Gamma_{\text{F}}^{\text{sur}}$  and the associated failure probability reads

$$P_{\mathrm{F}}^{\mathrm{sur}} = \int_{\Gamma} \mathbb{1}_{\Gamma_{\mathrm{F}}^{\mathrm{sur}}}(\mathbf{y}) \,\rho\left(\mathbf{y}\right) \,\mathrm{d}\mathbf{y}. \tag{5}$$

With this surrogate model, only polynomial evaluations are required, reducing the computational cost substantially.

#### 3.4 Hybrid Scheme

While the evaluation of the presented surrogate model is more efficient than the evaluation of the full model, the computed failure probabilities can be inaccurate. It has been shown, that this shortcoming may persist even if a very accurate surrogate model is employed together with a large number of samples [1]. As a remedy, a hybrid scheme, combining the accurate PDE model with the efficient surrogate model is used here [1].

The idea is to evaluate the surrogate model only when the considered sample lies far away from the boundary of the failure region, i.e.,  $|g^{\text{sur}}(\mathbf{y}^i)|$  larger than a certain threshold  $\delta$ . Once  $|g^{\text{sur}}(\mathbf{y}^i)|$  becomes smaller than this threshold and thus close to the failure region, the original model is used to evaluate  $\mathbb{1}_{\Gamma_F}$  instead of  $\mathbb{1}_{\Gamma_F^{\text{sur}}}$ . This idea is illustrated in Fig. 2 and reduces the problem to the one of finding an adequate value for  $\delta$ .

One possible approach to determine  $\delta$  is an iterative method [1] as outlined in the following. First, the surrogate model is evaluated for the full set of samples to obtain  $\{g^{\text{sur}}(\mathbf{y}^i)\}_{i=1}^M$ . For each  $g^{\text{sur}}(\mathbf{y}^i)$ ,  $\mathbbm{1}_{\Gamma_F^{\text{sur}}}$  can be evaluated with implicitely given  $\Gamma_F^{\text{sur}}$  and hence the hybrid failure probability  $P_F^{\text{hyb},(1)} = P_F^{\text{sur}}$  is computable. Then, the full model is evaluated for the  $\delta M < M$  samples that are the closest to the failure probability estimate. If the associated change in the failure probability  $P_F^{\text{hyb},(k+1)}$  is updated with the  $\delta M$  full model evaluations. Then, the next  $\delta M$  samples are chosen and the procedure is repeated until  $|P_F^{\text{hyb},(k+1)} - P_F^{\text{hyb},(k)}| \leq \eta$ . The here described procedure is given in Algorithm 1, where it is understood that  $M/\delta M$  is an integer.

1: **procedure** HYBRID( $g, g^{sur}, M, \delta M, \mathbf{y}, \eta$ ) set  $M^{(1)} = 0$ 2: set  $M^{(1)} = 0$  evaluate  $P_{\rm F}^{\rm hyb,(1)} = P_{\rm F}^{\rm sur}$  using (5) sort  $\{\mathbf{y}^i\}_{i=1}^M$  as  $\{\mathbf{y}_{\rm asc}^i\}_{i=1}^M$  s.t.  $\{|g^{\rm sur}(\mathbf{y}_{\rm asc}^i)|\}_{i=1}^M$  ascends ▷ Initialization 3: 4: for k = 1 to  $M/\delta M$  do ▷ Iteration 5: define  $M_1 = M^{(k)} + 1$ 6: define  $M_2 = M^{(k)} + \delta M$ evaluate  $g(\{\mathbf{y}_{asc}^i\}_{i=M_1}^{M_2})$  yielding  $\mathbb{1}_{\Gamma_{\mathrm{F}}}(\{\mathbf{y}_{asc}^i\}_{i=M_1}^{M_2})$ 7: 8: set  $\Delta P_{\rm F}^{\rm hyb,(k)} = \frac{1}{M} \sum_{i=M_1}^{M_2} \left( -\mathbb{1}_{\Gamma_{\rm F}^{\rm sur}}(\mathbf{y}_{\rm asc}^i) + \mathbb{1}_{\Gamma_{\rm F}}(\mathbf{y}_{\rm asc}^i) \right)$ set  $P_{\rm F}^{\rm hyb,(k+1)} = P_{\rm F}^{\rm hyb,(k)} + \Delta P_{\rm F}^{\rm hyb,(k)}$ if  $|P_{\rm F}^{\rm hyb,(k+1)} - P_{\rm F}^{\rm hyb,(k)}| \le \eta$  then return  $P_{\rm F}^{\rm hyb,(k+1)}$ 9: 10: 11: 12: end if 13: update  $M^{(k+1)} = M^{(k)} + \delta M$ 14: 15: end for return  $P_{\rm F}^{{\rm hyb},(k+1)}$ 16: 17: end procedure

Algorithm 1: Iterative algorithm to compute the hybrid failure probability using an expensive computer model g and a cheaper surrogate model  $g^{sur}$ . The tolerance  $\eta$  determines when the algorithm terminates.

This algorithm ensures that the error in the computed failure probability decreases as the accuracy of the surrogate model increases, in contrast to sampling the surrogate model solely [1]. However, the result might depend on the choice of the stepsize  $\delta M$ , which has to be determined empirically. As an alternative to this iterative approach, the value of the threshold  $\delta$  is estimated a posteriori using an adjoint approach in [3], yielding full control on the accuracy of the failure probability estimate.

Mathematically, the resulting hybrid failure probability is given by

with

$$P_{\mathrm{F}}^{\mathrm{hyb}} = \int_{\Gamma} \mathbb{1}_{\Gamma_{\mathrm{F}}^{\mathrm{hyb}}}(\mathbf{y}) \boldsymbol{\rho}\left(\mathbf{y}\right) \, \mathrm{d}\mathbf{y},$$

$$\mathbb{1}_{\Gamma^{\text{hyb}}} = \mathbb{1}_{\{g^{\text{sur}} < -\delta\}} + \mathbb{1}_{\{|g^{\text{sur}}| < \delta\} \cap \{g < 0\}}.$$

Here, the compact notation of e.g.  $\{g < 0\}$  is short for  $\{\mathbf{y} \mid g(\mathbf{y}) < 0\}$ .

#### 3.5 System Failure

In the previous sections, we introduced a method to compute the failure probability of bond wires efficiently. If a system of  $N^{\text{bw}}$  bond wires is considered, the system fails if any of these wires fails. Therefore, with (4), the condition for system failure is given by

$$\max_{j=1,\ldots,N^{\mathrm{bw}}} \max_{t \in I} T^{\mathrm{bw},j}\left(t,\mathbf{y}\right) > T_{\mathrm{cr}}.$$

It has been observed [10] that taking the maximum over all bond wires gives rise to a performance function that is not smooth and hence difficult to approximate with polynomials. For an efficient surrogate approximation, we thus calculate the failure probability  $P_{\mathrm{F},j}^{\mathrm{hyb}}$  for every wire independently. This also requires the repetitive application of Algorithm 1 for every single wire, as the  $\{\mathbf{y}^i\}_{i=1}^M$  are resorted in a different order for each wire. The event of failure of a single wire is not disjoint from the event of failure of another wire in general. Hence, we deduce from the basic axioms of probability theory, that the system failure probability can be estimated as

$$P_{\mathrm{F},\mathrm{s}}^{\mathrm{hyb}} \le \sum_{j=1}^{N^{\mathrm{bw}}} P_{\mathrm{F},j}^{\mathrm{hyb}}.$$
(6)

#### 4 Simulation Results

In this section, we apply Algorithm 1 to the example of a microelectronic chip package including bond wires of uncertain geometry (see Fig. 1). The goal of a bond wire designer is to dimension the bond wires such that the failure probability is low while minimizing the overall cost. For simplicity, we assume that the lengths of the wires are predetermined by the package, leaving the designer with the wires' diameter as the design parameter. Neglecting aging effects, the uncertain quantities **y** are modeled to be the relative change of the bond wire lengths. Therefore, we are assuming that the diameter of a wire is precisely controlled by the manufacturing process and a wire's geometry is only subject to an uncertain length  $l_i = l_{i,0}/(1 - y_i)$ , with a deterministic length  $l_{i,0}$  [6].

Table 1: Simulation settings.

Symbol	Description	Value
$N^{\mathrm{bw}}$	No. of wires in the model	12
d	Wires' diameter	12.07 µm
h	Heat transfer coefficient	$25 \mathrm{W/m^2/K}$
$N_t$	No. of time steps	51
tend	End time	50 s
$V_{\rm bw}$	Bond wire voltage	40 mV
$T_{\infty}$	Ambient temperature	300 K
$T_{\rm cr}$	Critical temperature	523 K
р	Polynomial degree of surrogate	1
Ν	No. of uncertain wires	2
М	No. of samples	$1 \cdot 10^{5}$
$\eta$	Tolerance for hybrid algorithm	$1 \cdot 10^{-10}$

#### 4.1 Numerical Setting

The here used setting for the simulation of the microelectronic chip package has been presented in [6]. In this paper, for simplicity and as shown in Fig. 1, we choose bond wires 1 and 2 to be subject to an uncertain length. Therefore, N = 2and the setup of the surrogate model is simplified. We can then focus on the iterative hybrid sampling algorithm which is the main topic of this work. For the high-dimensional case  $N = N^{\text{bw}} = 12$ , we refer to [3] and [10]. Since there is not sufficient measurement data available to determine the probability density function, we choose  $y_i$  to be uniformly distributed in the interval  $[\mu - \sigma, \mu + \sigma]$  with  $\mu = 0.17$  and  $\sigma = 0.048$ . If not otherwise stated, a first order surrogate (p = 1) with  $M = 1 \cdot 10^5$  samples was used. The tolerance to determine the termination of the hybrid algorithm is chosen to  $\eta = 1 \cdot 10^{-10}$ . For the bond wires' geometry, we assume that a designer has chosen the diameter to  $d = 12.07 \,\mu\text{m}$  and analyze this setting with the here presented method. The given simulation settings are also summarized in Table 1.

#### 4.2 Heating of the Chip

Due to the constant applied voltage and the convective thermal boundary conditions, the chip heats up until a stationary state is reached. Fig. 3 depicts the expected value of the temperature (blue) of bond wire 9 (cf. Fig. 1) based on the hybrid approach with  $\delta M = 10$  as presented in Section 3.4.



Figure 3: Temperature of bond wire 9 over time with  $6\sigma$  variation (blue) evaluated using the hybrid approach with  $\delta M = 10$ . The horizontal (red) line shows the critical temperature  $T_{cr}$  as a reference for failure.

The (red) horizontal line shows the critical temperature  $T_{\rm cr}$  as a reference for failure. Furthermore, error bars showing the  $6\sigma$ -deviation are plotted. At  $t = t_{end} = 50$  s, the standard deviation is given by  $\sigma_{MC} = 1.10 \text{ K}$ .

#### 4.3 Hybrid Failure Probability

From Fig. 3, we see that a small but nonzero failure probability is expected since the  $6\sigma$  deviation crosses the reference line for a wire failure. Note that in proper six sigma design, the upper limit of the six sigma interval would be expected to be entirely below the red line. However, in the present setting, the increased failure probability simplifies numerical investigations of the hybrid iterative algorithm.

We recall that a quantification of the failure probability based on the surrogate model solely may be inaccurate. Hence, Algorithm 1 is applied here. We compute the failure probability of each wire separately using different values for  $\delta M$ . Since the geometry of wires 9 and 10 ensures a higher conductance than all other wires, the highest temperatures are observed for these two wires. The here presented example is chosen such that the failure probability of these wires is very small. As the temperature of all other wires is lower, the failure probability is lower as well. However, the here chosen number of samples does not resolve these even smaller failure probabilities and are therefore computed to be zero.

The resulting evolutions of  $P_{\rm F}^{\rm hyb}$  of wire 9 and 10 (cf. Fig. 1) are shown in Fig. 4 and 5, respectively. The converged failure probability for wire 9 is  $P_{\rm F,9}^{\rm hyb} \approx 0.013$  and the one for wire 10 is  $P_{\rm F.10}^{\rm hyb} \approx 0.0071$ . It can be observed that the calculated failure probability changes only slightly during the execution of the algorithm. The reason for the small variation is that a change in the failure probability only occurs if a sample falls within the region where the surrogate model does not compute the failure of the wire correctly. Since this region is apparently very small compared to the failure region  $\Gamma_{\rm F}$ , there is only a very small but nonzero change observed. Additionally, we note that the number of required iterations until convergence depends highly on the chosen value for  $\delta M$ . Moreover, the algorithm might not converge at all if  $\delta M$  is chosen too small. This is e.g. observed for  $\delta M = 2$  in the case of wire 9 and



*Figure 4: Hybrid failure probability*  $P_{\rm F}^{\rm hyb}$  *over iteration k for* bond wire 9 and different choices of  $\delta M$ .



Figure 5: Hybrid failure probability  $P_{\rm F}^{\rm hyb}$  over iteration k for bond wire 10 and different choices of  $\delta M$ .

6

8

Iteration k

10

12

14

16

4

even for  $\delta M = \{2, 4, 6\}$  for wire 10 (cf. Fig. 4 and 5). Hence, to ensure the accuracy of the final probability estimate, repetitive runs of Algorithm 1 with different choices of  $\delta M$  are recommended.

Apart from the failure probability of a single wire, the system failure probability was defined in Section 3.5. With (6), it can be estimated for the here considered values of  $\delta M$ . The results range between 0.0191 and 0.0200. However, we recall that the results for  $\delta M = \{2, 4, 6\}$  have not converged as observed from Fig. 4 and 5. As already mentioned, the failure probability of all other wires was computed to zero since none of the Monte Carlo samples falls neither in the failure region nor in the threshold region defined by  $\delta$ . The algorithm for these wires therefore converges directly after the first iteration. The results for the system failure probability are summarized in Table 2.

#### 4.4 Efficiency of Surrogate Model

0

The surrogate is constructed using a tensor grid with  $(p+1)^N$ collocation points for which the full model needs to be computed. Therefore, the effort to construct the surrogate model depends on the number of uncertain parameters and on its polynomial degree. Furthermore, the number of required iterations to execute Algorithm 1 depends on the choice of  $\delta M$ as it is visible from Fig. 4 and 5. In Table 3, the total number of full model calls to calculate the hybrid failure probability of wires 9 and 10 is given as a function of the polynomial degree p and the iteration parameter  $\delta M$ . Comparing surrogate degree 1 and 2 under the condition that convergence was observed for the chosen  $\delta M$ , it is seen that the accuracy of the higher order surrogate leads to less iterations and therefore less full model calls. Furthermore, for degree 3, it is observed that the algorithm terminates directly after only one iteration.

*Table 2: System failure probability*  $P_{F,s}^{hyb}$  *for different*  $\delta M$ .

$\delta M$	2	4	6	8	10
$P_{\mathrm{F},\mathrm{s}}^{\mathrm{hyb}}$	0.0191	0.0197	0.0197	0.0200	0.0200

Table 3: Number of full model calls to compute the hybrid failure probabilities for wires 9 and 10 in dependence of the surrogate polynomial level p and the iteration parameter  $\delta M$ . The number of model calls to set up the surrogate model is included in the data.

wira	n	$\delta M$				
wite	p	2	4	6	8	10
	1	8	104	106	108	114
9	2	13	17	21	25	29
	3	18	20	22	24	26
	1	12	36	40	124	124
10	2	13	17	21	25	29
	3	18	20	22	24	26

The cost of using a surrogate with p = 3 is comparable to the case p = 2. However, the hybrid algorithm with surrogates of degree p > 3 require a more expensive setup without giving more accurate results. Moreover, it shall also be noted that all presented combinations lead to a much cheaper computation of the failure probability than using a pure Monte Carlo sampling with  $M = 1 \cdot 10^5$  full model evaluations.

#### 5 Conclusions

The hybrid scheme first presented in [1] has been applied to the evaluation of bond wire failure probabilities for the example of a microelectronic chip package as it has been presented in [6]. For a particular wire and a Monte Carlo sampling of a first order surrogate model (p = 1) with  $1 \cdot 10^5$  samples, the temperature as the result of the hybrid algorithm has been presented as a function of time. Since the six sigma deviation of this computed temperature exceeds the critical temperature  $T_{cr}$ , a non-zero failure probability was expected. For two wires, this failure probability has been computed using the iterative algorithm resulting in  $P_{\rm F,9}^{\rm hyb} \approx 0.013$  and  $P_{\rm F,10}^{\rm hyb} \approx 0.007$ . Then, the system failure probability was estimated to  $P_{\text{F,s}}^{\text{hyb}} \leq 0.0200$ . To assess the computational savings by the usage of a surrogate model, the surrogate efficiency has been evaluated. The main findings were that a more accurate surrogate model leads to a faster convergence of the hybrid algorithm. However, the cost of setting up higher order surrogates increases rapidly. In terms of efficiency, all investigated configurations showed significantly reduced computational cost with respect to pure Monte Carlo sampling. The drawback of the presented algorithm lies in the iteration parameter  $\delta M$  that needs to be determined empirically. An alternative to the here presented iterative approach is the usage of an adjoint error approach to obtain an a posteriori estimator for the threshold  $\delta$  [3]. This error estimator gives full control on the accuracy of the failure probability estimate.

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SESSION 3

## **SESSION 3** Power Electronics 1: Design

#### Design Methodology for Over-Temperature Protection of an LDO Voltage Regulator by Using Electro-Thermal Simulations

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#### Abstract

This paper presents a design methodology based on electro-thermal simulations for the over-temperature protection (OTP) of low drop-out voltage regulators (LDO). The OTP monitors the die temperature developed within the LDO and shuts down the circuit when the temperature reaches a set maximum level (the OTP trigger point). The proposed methodology involves running iteratively electrical, thermal and electro-thermal simulations. It addresses two major issues: first, it allows the designer to identify the suitable location of the OTP sensor by considering the temperature distribution within the LDO's power-stage. Second, the OTP trigger point can be set accurately taking into account coupled electro-thermal phenomena, so that the circuit is shut down when any section of the die reaches the maximum allowable temperature. The proposed methodology is validated by measurements performed on an LDO designed using it.

#### 1 Introduction

Low-dropout voltage regulators (LDOs) are part of most electronic circuits and are used to provide a stable and reliable voltage supply. LDOs can dissipate a lot of power during normal operation, most of it on the power-stage structure and this could affect its robustness and long-term reliability. The impact of thermal transients in normal operation for an LDO used for automotive applications and how the performances of the LDO are affected because of the dissipated power are studied in [1]. Furthermore, in fault condition like short-circuit at the output, the dissipated power on the power-stage increases even more.

Hence, the implementation of efficient over-temperature protection (OTP) becomes very important. As can be seen in Figure 1, the OTP circuit monitors the temperature of the OTP sensor and compares it with a reference. When the temperature of the OTP sensor increases over a threshold, the OTP<sub>OUT</sub> signal closes the power-stage by bringing down the base of the driver  $(T_{DRIVER})$ . The circuit is designed so that in normal operation (when the temperature on the sensor is lower than the threshold) does not influence the operation of the LDO. An essential aspect in designing the OTP of an LDO is the thermal coupling [2] between the sensor and the power-stage, that is the difference between the sensor's own temperature and the peak temperature (hotspot) within the LDO. The importance of this issue increases as the power density used in nowadays LDOs increase and their dies get thinner.

Thermal simulations are performed in order to obtain the thermal resistance and the thermal coupling resistance of an integrated circuit (IC) as a function of its power dissipation. However, the thermal-only simulations assume that the

electrical parameters of the circuit do not change when the temperature varies due to the applied power [3, 4].

Standard electrical-only simulators assume that all devices within a chip operate at the same temperature; even those which can take into account the thermal map of the IC, are not able to change this map during the simulation, to include the effects of self-heating.

The limitations of using un-coupled thermal and electrical simulations (that is, thermal-only and electrical-only simulations run independently) while designing LDOs are highlighted in [5]. The variation in time of the temperature distribution cannot be revealed by performing thermal-only simulations and this could cause the damage of the circuit. Also the dependency between the initial conditions (different scenarios regarding the polarization of the circuit) and the temperature distribution can be fully covered only by performing electro-thermal simulations [6, 7].

The electro-thermal simulations cover the coupled electrical and thermal phenomena. The parameters of the devices are changed during the simulation based on the temperature variation within the chip. Several methodologies for performing electro-thermal simulations can be found in literature [7-9]; their focus is in minimizing the simulation time and the resources used for the simulation. These methodologies also provide design and layout information for the entire device but not for its own protection circuits in particularly.

This paper provides a design methodology for the OTP of an LDO based on electro-thermal simulations. It allows the designer to optimize the placement of the OTP sensor according to the temperature distribution within the LDO's power-stage and to set accurately the OTP trigger points (activation and deactivation thresholds of the circuitry).



Figure 1: Block Diagram of an LDO with OTP circuit

This methodology is used to design an LDO and is validated by comparing electro-thermal simulations results with measurements performed on the integrated LDO. The outline of this paper is as follows: in Section 2 the proposed methodology is described, Section 3 provides a design example based on the proposed methodology and in Section 4 the summary and the conclusions are presented.

#### 2 Proposed Methodology

The methodology proposed for designing the OTP circuit relies on running iteratively electrical, thermal and electrothermal simulations to optimize its placement and trigger point values. The flow-chart that describes the methodology is presented in Figure 2.

Starting from a safety specification regarding the maximum temperature allowed within LDO, the methodology contains three important steps: Electrical-only Simulations, Thermalonly Simulations and Electro-Thermal Simulations. For each step in the methodology flow chart detailed in Figure 2, the inputs used to accomplish the intermediate results are represented with rectangular shapes. The outputs of each step are included in circular shapes. The temperature distribution map and the thermal coupling obtained after the second step are used to create the optimal layout configuration for the circuit. The trigger points are then finetuned in the third step based on the results obtained previously and after performing iteratively electro-thermal simulations.

#### 2.1 Electrical-only Simulations

Electrical-only simulations are used for the first-pass design of the OTP, but allowing for the known limitations of this method. These simulations assume a constant temperature distribution across the die, while the temperature of the hotspots within the LDO can be much higher. To account for this difference the OTP activation temperature should be set in this step to a lower value than the maximum temperature allowed for the LDO. The value of this temperature offset is set by the designers based on their experience, with obvious drawbacks. The traditional OTP design – still used when no thermal simulator is available – consists basically on this step. No layout information is necessary at this stage.



Figure 2: Flow-chart of the methodology proposed to design the OTP circuitry

#### 2.2 Thermal-only Simulations

Second, thermal-only simulations are used to adjust the trigger points of the OTP and to analyse the temperature distribution within the LDO. The latter depends on the size, shape and placement with respect to chip boundaries of the LDOs power-stage and on the power dissipated. Another important aspect considered in this step is the OTP sensor location. This is a crucial element in order to minimize the temperature difference between the peak temperature (hotspot) and the OTP sensor, hereby called thermal coupling. Therefore the thermal-only simulations are used to identify the best-suited shape of the power-stage and the optimal location of the OTP sensor. Usually the activation threshold (first trigger point) of the OTP is designed to be at a value lower than the maximum temperature allowed and the temperature difference corresponds to a safe thermal coupling (predicted from thermal simulator).

The inputs for the thermal simulations are the layout configuration, the amount of power dissipated and the physical description of the package of the device. The layout configuration does not need to be the final version.

#### 2.3 Electro-Thermal Simulations

The best option is chosen for the third step: electro-thermal simulations for fine tuning the OTP trigger points. A real-life scenario is used in order to replicate the OTP event of the LDO. The sensor temperature when the OTP disables the LDO is readjusted according with the specifications and with the results obtained for the thermal coupling in the second step.

For the electro-thermal analysis of the circuit operation two strategies can be involved. The direct method uses a  $Z_{TH}$  network that captures both the self-heating of each block considered in the simulation and the mutual heating component between block pair [10-11]. An alternative simulation approach is the relaxation method via simulator coupling. This uses the power dissipation data from an electrical analysis as input for a thermal simulation and then the temperature distribution data is annotated in the



Figure 3: Flow-chart of the electro-thermal co-simulation method based on the relaxation method, and the evolution in time of the power. [7]

electrical netlist in order to model the temperature of each device.

Modelling the LDO operation, where the heating in the system is dominated by the output stage, using the direct method has an important advantage: the  $Z_{TH}$  matrix will comprise only one non-zero diagonal element, which represents the self-heating of the output stage, while the other elements represent the heat transfer from the output stage to the other relevant circuits. The main disadvantage foreseen in this case is the difficulty to model correctly the silicon behavior over the automotive temperature range.

For our case when the relaxation method is used, the electrical simulation is performed using Cadence Spectre and the thermal simulation is done using an in house tool presented in [6] which takes into account the temperature dependence of thermal properties for the silicon substrate. We assume that the energy dissipated in the LDO can be correctly captured only via electrical steady states corresponding to different temperature distributions. Thus the transient analysis is driven by the thermal simulator. A mapping file sets the correspondence between the power source in the thermal domain and the devices/sub-circuits in the electrical netlist. As only the output stage of the LDO is considered to have significant power dissipation, for the other circuits in this analysis the power dissipation is ignored and only the average temperature in the area assigned to these elements in the thermal simulation is read. Thus we can annotate the temperature on full sub-circuits without analyzing each device individually. Accuracy is insured by performing the analysis for a given time step multiple times until the difference between the temperatures computed for consecutive iterations at the same time point is smaller than a predefined threshold and then the simulator proceeds to start computing the solution for the next time point (Figure 3).

#### 3 Design Example

#### 3.1 Requirements

The power distribution within the LDO's power-stage and the location of the hotspots depend on the size, shape and placement with respect to chip boundaries. We focus on the later considering the case of an LDO with defined power-stage size and position - near the top edge of the chip. In our case the specification regarding the maximum temperature allowed within the LDO is  $185^{\circ}$ C. The OTP thresholds are designed according to the latest: the activation threshold (T<sub>HIGH</sub>) is adjusted to fulfil this requirement considering the thermal coupling and the deactivation threshold (T<sub>LOW</sub>) is modified in order to obtain a minimum 15 °C hysteresis.

The scenario considered here is presented in Figure 4. The ambient temperature of the entire LDO is set at a fixed value, 150°C (which is the upper limit for the automotive temperature range) and then the input voltage is ramped-up. The output voltage is adjusted at 1.2V and the load current is 70 mA (resistive load). Thus, the dissipated power (1.8W) goes over the value corresponding to normal operation of the LDO, leading to an over-temperature event.



Figure 4: Scenario considered for the thermal simulations, electro-thermal simulations and measurements



Figure 5: Temperature maps for the three cases – OTP sensor placed below (a) and above (b) the rectangular-shaped power-stage and the OTP sensor placed in the notch of the power-stage (c)



Figure 6: Thermal analysis showing temperature vs. time whithin the third LDO option (Fig. 4c) for the: maximum temperature, OTP sensor temperature and minimum temperature within the power-stage

Table 1: Thermal coupling values (DeltaT [ $^{\circ}C$ ]) yielded by thermal simulations for four test scenarios

	T <sub>CHIP</sub> =-40°C		Тснір=150°С	
Power Dissipated	1.8W	10W	1.8W	10W
TSD sensor below	14	68	12	20.7
TSD sensor above	9	45	9	20.8
TSD sensor in a notch	5.8	30	6	20.4



*Figure 7: Simulated electro-thermal behavior of the powerstage and its OTP* 

#### 3.2 Design steps

The trigger points set in the first step of the methodology (electrical-only simulations) are 180°C for  $T_{HIGH}$  and 160°C for the  $T_{LOW}$ . The  $T_{HIGH}$  threshold was set by adjusting the reference used to compare it with the temperature of the OTP<sub>SENSOR</sub>. The activation threshold was set to this value because it was considered that at this value the peak temperature on the power-stage will not exceed the maximum temperature allowed within the LDO.

For the second step, three options are presented in Figure 5: a rectangular-shaped power-stage with the OTP sensor placed above and below, then a notched-rectangle, with a gap in the middle hosting the OTP sensor. It can be seen that the temperature distribution is more uniform for the notched-rectangle power-stage than for the compactrectangle cases.

The thermal-only simulations also provide temperature versus-time plots like those shown in Figure 6. This presents the variation in time of the maximum and minimum temperature within the LDO and the sensor temperature for the scenario considered here. The thermal coupling is extracted as the difference between the maximum allowed temperature in the output stage (185 °C) and the temperature at the sensing point (in this case the thermal coupling is  $6^{\circ}$ C). The T<sub>HIGH</sub> threshold of the OTP is adjusted according to the results obtained in this step: is set at 179 °C, a lower value than in the previous step. Table 1 summarizes data obtained from thermal simulations for four test scenarios: the initial chip temperature  $(T_{CHIP})$  equal to -40°C (blue column) or 150°C (orange column) and the power dissipated by the LDO equal to 1.8W (normal operation) and 10W (maximum value, corresponding to a short circuit at the output). Table 1 also shows that the notched-rectangle power stage has the best thermal coupling (smallest DeltaT [°C] value). In the second step the activation temperature of the OTP was adjusted and the best-suited configuration from the thermal coupling point of view was chosen (the notchedrectangle power stage).

In the third step electro-thermal simulations are performed for the same scenario described in Figure 4. The setup contains besides the floorplan and the electrical netlist, a structure definition. The structure definition is a list of properties (thermal conductivity, thermal capacitance and density etc.) for each layer contained in the floorplan. Also the structure definition must contain the parameters that define the vertical dimensions of the structure (thickness). The simulation takes into account the Si die, package and mounting elements. For time constants in the tens of milliseconds the Si die will have an important contribution in the energy dissipation in the system and thus one needs to account correctly for the temperature dependence of the thermal conductivity of Si. From [12] we consider a power low to model this behaviour:

$$k_{Si} = k_0 \left(\frac{T}{T_0}\right)^a \tag{1}$$

where for low doped Si,  $k_0=147W/K*m$  is the thermal conductivity at room temperature,  $T_0=300K$  and a=-1.28. Over the relevant automotive temperature range, the thermal conductivity of the die will halve in value according to (1).

In Figure 7 is presented the electro-thermal behaviour of the LDO: the OTP disables the LDO when its sensor reaches  $174^{\circ}C$  (value set after successive simulations), which corresponds to the power-stage hotspot reaching  $185^{\circ}C$ ; the OTP trips back when the temperature on its sensor decreases to  $159^{\circ}C$ , realizing the wanted hysteresis (minimum  $15^{\circ}C$ ).

#### 3.3 Measurement results

Table 2 presents sets of simulated and measured results for the OTP event. The measurements results from Table 2 for torp and toFF were extracted from the output voltage measurements (Figure 8) performed for the test scenario considered here and represent mean values of four samples. Another test setup was used to obtain the measured values for the OTP trigger points: the LDO was kept in normal operating mode, similar to the configuration shown in Figure 4 except for the value of the load current, which in this case is kept very small in order to neglect the power dissipation effects. Then the temperature of the LDO is increased with a step of 1°C and the output voltage is monitored. The T<sub>HIGH</sub> value is considered when the output voltage drops down to 0V. In order to measure the  $T_{LOW}$ , after the output voltage drops down to zero, the temperature is decreased with the same step, 1°C, until the output voltage reaches the nominal value.

The differences between the electrical and the electrothermal simulated values regarding the OTP trigger points are given by the different setups. For the electrical simulation the temperature of the entire circuit is set at the same level and varied until the activation and deactivation thresholds of the OTP are triggered. For the electro-thermal simulation the temperature of each device/sub-circuits is set according to the temperature distribution at each computed time step extracted from the simulator.

The proposed design methodology is validated by the good agreement between the measurements and the electrothermal simulations results regarding the time until the OTP event occurs (t<sub>OTP</sub>): 59.5 ms and 60.5 ms respectively. Using the correlation between the t<sub>OTP</sub> and the PowerStage TempMax (Figure 6) one can prove that the requirement regarding the maximum temperature allowed within the LDO is fulfilled. The inconsistency regarding the time between the start and the end of the OTP event  $(t_{OFF})$  is an ongoing work. The LDO is implemented in a bipolar technology for which we have some question marks regarding the model accuracy of the leakage current. The differences between the measurements and the electrothermal simulations, 1.3 ms respectively 13.4 ms, do not affect the requirement regarding the maximum temperature allowed within LDO.

The results yielded by the electro-thermal simulations based on the relaxation method are closer to measurements than those obtained by the direct method. Obviously, one cannot claim this is generally the case based on a single case.

The samples measured displayed a significant spread in  $t_{OTP}$  and thus only the average value was used in Table 2. One important driver for this behaviour is the variation of the thickness of the die attach material in the package. This is presented in Figure 9 for the full range of thickness, normalized at the typical value. As the die-attach thickness increases the thermal resistance increases and the LDO heats

Table 2: Comparison between simulated and measuredvalues for the OTP trigger points

	Тнібн [°C]	Tlow [°C]	toтP [ms]	toff [ms]
Electrical or Thermal Sims	180	160	86.1	-
Electro-Thermal Sims (relaxation method)	174	159	60.5	13.7
Electro-Thermal Sims (direct method)	173	157	19.5	9
Measurements	181*	166*	59.5*	1.3*

\*mean value of 4 samples



*Figure 8: Output voltage measurement performed for an LDO in a silicon implementation – one sample (the time until OTP occurs is detailed)* 



Figure 9: Variation of the  $t_{OTP}$  with the die thickness.

faster, leading to significantly lower  $t_{\rm OTP}$  values. The simulated results presented in this paper corresponds to the typical die attach thickness.

#### 4 Summary and Conclusions

A design methodology for the over-temperature protection of LDO is presented in this paper. First, the limitations of using un-coupled thermal and electrical simulations are highlighted: electrical-only simulators assume that all devices within a chip operate at the same temperature while thermal-only simulators cannot change the electrical parameters of the circuit during simulations, to follow changes in the die temperature. Only by performing electrothermal simulations one can adjust the electrical parameters of the circuit devices taking into account the temperature variations yielded by thermal simulations, and then adjust the power dissipation for the next thermal simulations.

The methodology proposed involves running iteratively electrical, thermal and electro-thermal simulations. It comprises three steps: first, the circuit is designed using electrical-only simulations, but setting the OTP trigger point at a lower level than the one corresponding to the required maximum allowable temperature. Next, thermal-only simulations are used to adjust the trigger points of the OTP and to analyse the temperature distribution within the LDO. Different layout configurations are verified and the bestsuited shape of the power-stage and the optimal location of the OTP sensor are chosen. Finally, electro-thermal simulations are run on the chosen layout configuration, including forcing the apparition of over-temperature events. Thus, the OTP trigger point can be fine-tuned, in order to ensure that the OTP will indeed disable the LDO when any section (worst-case hot-spot) of it reaches the maximum allowable temperature.

An example was presented: the design of an LDO for automotive applications, with the maximum temperature allowed within the LDO set to  $185^{\circ}$ C. Measurements performed on the integrated LDO validated the design methodology: when the LDO was forced to dissipate 1.8W the die temperature increased until it reached the maximum allowable value, triggering the OTP as expected; the simulated value of the time it took the OTP to flag the overtemperature event –  $t_{OTP}$  - was very close to the measured value, within 1.7%. The correlation was not as good for the time it took the OTP to de-activate itself –  $t_{OTP}$ . Of the many factors affecting the simulated value of the time attach thickness – was analyzed in the paper.

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## Smaller Size and Higher Reliability for Vertical Chip Mounted Type Power Device

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#### Abstract

This paper presents a new structure of the power device to reduce the size and improve the reliability. Our conventional device with vertical chip mounting is half size of the former device and we proposed a new one for further miniaturization and higher reliability. The proposed device with top and bottom surfaces cooling which allows higher power density is 30% smaller than our conventional one with only the bottom surface cooling. Also, to evaluate the reliability, the finite element analysis (FEA) of the thermal stress and the power cycle tests which are commonly used in evaluating the reliability were performed. The thermal stress of the proposed device can be reduced by 40%, and the power cycle test results showed the high reliability.

#### **1** Introduction

Recently, module type power devices have been applied to inverter equipment such as elevators, railroads, electric vehicles (EV), hybrid electric vehicles (HEV) and many other fields as shown in Figure 1.

By expanding the application fields, power devices offer a significant reduction in the packaging volume to make the best use of the available space. Thermal management of the power device needs to be considered because of their packaging constraints and high power density. For instance, the heat dissipation path from the semiconductor chips to the package surface is one of the most important matters.



*Figure 1: Application examples of module type power devices* 

In addition, since the devices are exposed to high ambient temperature and the rapid temperature change by acceleration and deceleration of motors, the reliability of the thermal stress is also required. Thermal stress fatigues the material interfaces and cause the failure by cracking at the interface because of the Coefficients of Thermal Expansion (CTE) mismatches between different materials [1].

In order to meet these miniaturization and reliability demands, a large number of highly qualified power devices have been researched and developed.

Wire-bonding, which is low cost and flexible in the process, is the most commonly used method for the semiconductor interconnection. However, wire-bonding could cause high thermal resistance and the difficulty of heat flow through wire bonds.

To reduce the thermal resistance and improve the heat characteristics, the double-sided cooling from top and bottom surfaces of the power device package is one of the good solutions.

The thermal and thermomechanical properties of solder-bumps and direct-solder bonded power device packages with double-sided cooling, which don't need wire-bonding, were investigated by using temperature cycle experiment and computer simulations by finite element modeling (FEM) [4]. Also, the Center for Power Electronics Systems at Virginia Tech developed a novel planar integration technology called Embedded Power [5]. To investigate the advantage of using double-sided cooling for Embedded Power devices, experiments were performed and verified the improvement in the thermal performance of integrated power devices with double-sided cooling [6].

Toshiba has also developed the vertical chip mounted type power device, which is cooled from both sides of a semiconductor chip [8, 10, 11, 12, 13]. This structure can realize that the generated heat loss of the semiconductor chip is cooled from both sides of the chip, and the thermal resistance is reduced. In addition, this device can suppress the temperature rise in a short time because of the large heat capacity. This characteristic is effective especially in inverters for driving motors such as railroads and EV/HEVs.

In this paper, for further miniaturization and higher reliability, we proposed a new device structure. Also, to evaluate the reliability of the proposed device, we analyzed the thermal stress by finite element analysis (FEA) and performed the power cycle test.

### 2 Conventional vertical chip mounted type power device

The perspective view of the conventional power device is shown in Figure 2. We developed the vertical chip mounted type power device cooled from both sides of a semiconductor chip, and it is half size of the former device with single-sided cooling. As shown in Figure 2, semiconductor chips, both sides of which are bonded to thermal diffusion blocks, are arranged vertically to the cooling surface.



Figure 2: Perspective view of conventional vertical chip mounted type power device

Figure 3 shows the front view and the heat dissipation path. This structure can realize that the generated heat loss of the semiconductor chip is cooled from both sides of the chip, and the thermal resistance is reduced. In addition, this device can suppress the temperature rise in a short time because of the large heat capacity of thermal diffusion blocks.

Figures 4 and 5 show the heat characteristic of the device. In these figures, generated heat loss of the semiconductor chip is 100 W, and cooling surface is 25 degrees. Figure 4 shows the simulation result of the temperature distribution when the temperature is saturated, and Figure 5 shows the simulation and experiment results of the thermal resistance

measurement. We can confirm that the heat is cooled from both sides of the semiconductor chip in Figure 4, and the transient thermal resistance is suppressed (rises slowly) in Figure 5 because the thermal diffusion blocks absorb the heat. Therefore, the structure makes it possible to reduce both of transient and saturated thermal resistance.

This characteristic is effective especially in inverters for driving motors such as railroads and EV/HEVs. For instance, when using inverters under the condition of huge current in a short time like the starting time of driving motor or acceleration, this device can suppress the rapid temperature rise.



Figure 3: Front view of conventional vertical chip mounted type power device and its heat dissipation path



*Figure 4: Thermal simulation result of conventional vertical chip mounted type power device* 



Time of Electric Current Supply

Figure 5: Heat characteristics of conventional vertical chip mounted type power device

### **3** Proposed vertical chip mounted type power device

In this paper, for further miniaturization and higher reliability, we proposed a new structure as shown in Figure 6. Conventionally our device has only the bottom surface cooled, but, by also designing a cooling surface on the top of the device, it is possible to reduce the device size because the heat radiating area increases.

The front view of the proposed power device and the heat dissipation path are shown in Figure 7. As shown in Figure 7, the generated heat loss of semiconductor chips is cooled not only from both sides of the semiconductor chip but also from both top and bottom cooling surfaces in this structure. Therefore, the heat radiating area increases and higher power density is realized compared to the conventional device.



Figure 6: Perspective view of proposed power device



Figure 7: Front view of proposed power device and its heat dissipation path



*Figure 8: Comparison of device size between conventional and proposed device* 

The Comparison of device size is shown in Figure 8. Though an upper heat sink is added, the device size reduces by 30% in the proposed device by reducing the size of lower heat sink and thermal diffusion blocks.

The heat characteristics, which are under the same thermal loading conditions in chapter 2, are shown in Figures 9 and 10. In these figures, we can see that even when the device reduces the size, the proposed device has the same saturated heat characteristic as the conventional one because of ensuring the radiating area by designing a cooling surface on top of the device.

Moreover, Figure 11 shows the relation between thermal diffusion block width and transient thermal resistance. In this graph, the change of transient thermal resistance when the thermal diffusion block width changes from the conventional block width (the conventional block width is 1) is shown. The transient heat characteristic can be kept within the range of more than 60% of the conventional block width. Therefore, we can design the smaller device that has the same transient and saturated heat characteristics as the conventional one by designing a top cooling surface and the thermal diffusion block which is more than 60% of the conventional size.



Figure 9: Thermal simulation result of proposed power device



Figure 10: Heat characteristics of proposed device



*Figure 11: Relation between thermal diffusion block width and transient thermal resistance* 

#### 4 FEA results of thermal stress at insulation part

Within the proposed structure, insulation part has a role of radiating and insulating between electric circuit and heat sink. Since the devices are exposed to high ambient temperature and the rapid temperature change by acceleration and deceleration of motors, it is important to guarantee the characteristics of the insulation and radiation from the thermal stress when an inverter drives.

However, the reliability of the proposed device for the thermal stress has not been fully investigated yet. To evaluate the reliability of the insulation part, we performed FEA of the thermal stress.

The FEA results are shown in Figure 12. It shows the enlarged view of the insulation part closed to the thermal diffusion block corner. These analyses are under the same thermal loading conditions. In these figures, we can confirm that the thermal stress is reduced in the proposed device.

The comparison of thermal stress is shown in Figure 13. The proposed structure can reduce the thermal stress by 40%. By cooling from the top and bottom surface, the heat flux passing through the insulation part can be reduced, compared with our conventional structure cooled only from the bottom surface. As a result, the temperature difference around the insulation part is reduced and the thermal stress can be reduced.



(b) Proposed device





*Figure 13: Comparison of thermal stress between conventional and proposed device* 

#### 5 Power cycle test with prototypes

Furthermore, using prototype devices, we performed power cycle tests which are commonly used in evaluating reliability for the thermal stress. In power cycle tests, the thermal stress is given to power devices by repeating turning on and off electricity and giving the junction temperature change. Thermal stress could cause the material bonding surface cracks because of the CTE mismatch between different materials.

To evaluate the power cycle lifetime of the bonding surface between thermal diffusion blocks and the insulation part, we performed the tests under the condition that the change of the junction temperature is  $\Delta T j$ =100K. We evaluated the reliability by measuring the increase of the thermal resistance from the semiconductor chip to the heat sink.

The results are shown in Figure 14. Thermal resistance from the semiconductor chip to the heat sink keeps almost the initial value until 50000 cycles.

Also, from the image of insulation part after 10000 cycles obtained by ultrasonic testing (Sample 1) in Figure 15, we can make sure there is no damage in the insulation part. We have confirmed that the prototype devices have had a high reliability.



Figure 14: Rate of thermal resistance increase



Figure 15: Insulation part after 10000 cycles obtained by ultrasonic testing (using Sample 1)

#### 6 Conclusion

This paper presents a new structure of the vertical chip mounted type power device to reduce the size and improve the reliability. The proposed device is 30% smaller than our conventional one, by cooling from the top and bottom surface.

In addition, to evaluate the reliability, we performed the FEA of the thermal stress and power cycle tests with prototype devices. We have confirmed that the thermal stress can be reduced by 40%, and the test results showed the high reliability of our proposed device.

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#### **Electro-Thermal Simulation for High Power IGBTs for Automotive Applications**

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#### Abstract

Safe and reliable operation of power electronics in a particular application hinges on the accurate design of thermal management systems that perform the task of heat removal from the devices. This requirement reaches paramount importance for IGBTs and Diodes used in high power automotive applications where ambient temperatures under the hood exceed 65°C. This work demonstrates in-depth system analysis via developed electro-thermal models that take into account both semiconductor losses and the overall system thermal stack-up. This knowledge not only allows design engineers to ensure proper operation of the device in a particular application but also evaluate the reliability of the silicon, bondwires and thermal interfaces of the package due to thermal stresses induced over various worst case converter operating conditions.

#### 1 Background

In order for power semiconductors to operate safely and reliably, the switching and conduction losses generated within the device that manifests itself as heat must be efficiently removed from the package. This requirement reaches paramount importance for IGBTs and diodes used in high power automotive applications such as traction inverter, DC/DC converter, and AC Compressor in electric and hybrid electric vehicles (EV / HEV). As such the design of a power converter regardless of the particular application goes beyond simply sizing components based on electrical operating conditions. Electro-thermal simulation has gained significant popularity due to its ability to perform very rapid cross domain analysis for a wide range of applications [1-11]. This work demonstrates in-depth system analysis via developed electro-thermal models that take into account both semi-conductor losses and the overall system thermal stack-up. This knowledge not only allows design engineers to ensure proper operation of the device in a particular application but also evaluate the reliability of the silicon, bondwires and thermal interfaces of the package due to thermal stresses induced over various worst case converter operating conditions [12-17].

#### 2 Methodology

In this work, we evaluate Infineon's AUIRGPS4067D1 copack IGBT in Super T0-247 package in a 3-phase inverter topology commonly seeing in automotive motor drive applications. The power dissipated in the IGBT and diode during steady state and transient operation is obtained by utilizing a device loss model that incorporates both switching (during IGBT turn ON / OFF and diode reverse recovery) and conduction losses as provided in the device data sheet.

#### 2.1 Loss Model for IGBT and Diode

An off the shelf IGBT can be taken to realize a single leg of a 3-phase inverter as shown by Figure 1. The turn ON  $(E_{on})$ ,

OFF  $(E_{off})$  and diode's reverse recovery  $(E_{rr})$ , losses for such a hard switched topology can be described as shown by the following equations.

$$E_{on} = f(V_{BUS}, R_{G,on}, T_J, I_{CE})$$
(1)

$$E_{off} = f(V_{BUS}, R_{G,off}, T_J, I_{CE})$$
<sup>(2)</sup>

$$E_{rr} = f(V_{BUS}, R_{G,on}, T_I, I_D)$$
(3)

For a system where there is a fixed bus voltage ( $V_{BUS}$ ) and turn on and off gate resistors ( $R_{G,on}$  and  $R_{G,off}$ ), the switching losses for the IGBT and diode are based only on current conducted ( $I_{CE}/I_D$ ) and silicon junction temperature ( $T_I$ ).

The forward voltage drop on the IGBT ( $V_{CE}$ ) and co-pack diode ( $V_F$ ) can be described by the following equations.

$$V_{CE} = f(T_J, I_{CE}) \tag{4}$$

$$V_F = f(T_J, I_D) \tag{5}$$

#### 2.2 Electro-thermal Model for a 3-phase Inverter

For an inverter leg shown in Figure 1, the instantaneous power dissipation arising from switching  $(P_{sw})$  and conduction  $(P_{cond})$  losses on the IGBT and diode can be represented with subscripts *I* and *D* as shown below.

Switching losses for the IGBT and diode,

$$P_{sw-I}(t) = \left[E_{on}(t) + E_{off}(t)\right] \cdot f_{sw} \tag{6}$$

$$P_{sw-D}(t) = E_{rr}(t) \cdot f_{sw} \tag{7}$$

$$P_{total-sw}(t) = P_{sw-I}(t) + P_{sw-D}(t)$$
(8)

Conduction losses for IGBT and Diode,

$$P_{cond-I}(t) = D(t) \cdot |I_L(t)| \cdot V_{CE}(t) \cdot S \qquad (9)$$

$$P_{cond-D}(t) = D(t) \cdot |I_L(t)| \cdot V_F(t) \cdot S^*$$
(10)

$$P_{total-cond}(t) = P_{cond-I}(t) + P_{cond-D}(t) \quad (11)$$

Here  $f_{sw}$  denotes switching frequency and D(t) represents duty cycle which can be based on either space vector pulse width modulation (SVPWM) or sinusoidal pulse width modulation (SPWM) schemes. Since the direction of current seeing by IGBT and co-packed diode are 180° out of phase as shown in Figure 1, directionality functions called *S* and  $S^*$  are defined as shown below.

$$S = \frac{|sign(x)+|sign(x)||}{2}, S^* = \frac{|sign(x)-|sign(x)||}{2}$$
(12)  
where  $x = I_L(t)$ 

The total instantaneous inverter losses  $(P_{total})$  can be expressed as shown below,

$$P_{total}(t) = P_{total-sw}(t) + P_{total-cond}(t)$$
(13)



Figure 1: Single leg of a 3-phase inverter realized with IGBTs with anti-parallel diodes (top) and depicts sinusoidal currents flowing through stator windings (bottom).

#### 2.3 Transient Thermal Model

A typical application environment is emulated by constructing the 3-phase inverter thermal model by mounting six co-pack IGBTs in Super T0-247 package on an Aluminum heatsink with thermal interface material (TIM). While higher power applications will require a liquid cooled heatsink, for illustration purposes in this simulation the other side of the heatsink surface is terminated by a fixed temperature boundary condition.



Figure 2: Thermal simulation of 3-phase inverter with copack IGBTs in Super T0-247 package mounted on Al heatsink with TIM. IGBT and diode junctions made visible (low left hand side).

The transient thermal impedance  $(Z_{th})$  can be used to completely characterize the thermal response of power semiconductors in a system [18-20]. The following four  $Z_{th}$ profiles are required to represent temperature response of IGBT and diode' silicon junctions as shown in Figure 2,

- Self  $Z_{th}$  of IGBT ( $Z_{th-I-self}$ )
- Self  $Z_{th}$  of diode  $(Z_{th-D-self})$
- Mutual coupling Z<sub>th</sub> from IGBT to diode within a package (Z<sub>th-I-D</sub>)
- Mutual coupling Z<sub>th</sub> from diode to IGBT within a package (Z<sub>th-D-I</sub>)



Figure 3: Transient thermal impedance profiles  $(Z_{th})$  for IGBT, diode and respective coupling between the two devices within a single package.

The coupling between packages must also be taken into account. Since there are a total of twelve dies (n) on the heatsink, there are ideally a n-1 of coupling paths that should be considered or each device. In this analysis all IGBT and diode dies are heated separately in order to simplify analysis and at the same time approximate the package to package thermal coupling. Figure 3 shows the normalized thermal responses obtained from this approach by Computational Fluid Dynamics (CFD) thermal simulations performed in Flotherm.

As a result, the transient thermal response of the IGBT  $(T_{J-I}(t))$  and diode  $(T_{J-D}(t))$  silicon junction can be expressed in matrix form as shown below,

$$\begin{bmatrix} T_{J-I}(t) \\ T_{J-D}(t) \end{bmatrix} = \begin{bmatrix} P_{total-I}(t) \\ P_{total-D}(t) \end{bmatrix} \cdot \begin{bmatrix} Z_{th-I-self}(t) & Z_{th-D-I}(t) \\ Z_{th-D-self}(t) & Z_{th-D-I}(t) \end{bmatrix} + T_{amb}(t) (14)$$

Here  $T_{amb}(t)$  represents the ambient temperature of the system which can also be time variant depending on application conditions. The transient thermal impedance profiles (Z<sub>th</sub>) shown in Fig. 3 for IGBT, diode and mutual coupling between the two devices are combined with a 3-phase inverter system model developed in MATLAB Simulink for electro-thermal co-simulation.

#### 3 Results

Electro-thermal simulations are performed to evaluate the IGBT and diode performance when configured as a 3 phase inverter in a motor drive application. The inverter is excited over various operation modes and device temperatures are predicted for key system parameters such as power factor (*PF*) and fundamental frequency ( $f_{fundamental}$ ). It will be shown in the following cases that this results in drastically varying amounts of power dissipation and consequently junction temperatures on the IGBT and diode respectively. For the following simulation examples, the inverter is supplied by a bus voltage,  $V_{BUS}$  of 400V, a common level for an automotive battery pack system. The initial ambient temperature,  $T_{amb}$  is assumed to be 85°C for these simulation cases.

#### 3.1 Motor Simulation Case 1 – High Speed Operation

In this simulation case, the motor's high speed operation is emulated by driving the inverter at a fundamental frequency  $f_{fundamental}$  of 100Hz. For a permanent magnet synchronous machine (PMSM), the resulting increase in back electromotive force (EMF) with motor speed requires an increase in stator winding current in order to maintain motor torque. Here the PMSM's high speed operation results in a resistive load appearing at the terminals of the 3 phase inverter evident by the phase difference between matching colored voltage and current waveforms in Figure 4 resulting in a power factor (*PF*) close to unity for this particular application condition.



Figure 4: Voltage (top) and current (bottom) waveforms for three phase inverter (PF=0.8 and  $f_{fundamental} = 100Hz$ ).

In Figure 5, the top plot shows the transient junction temperatures experienced by the IGBT and diode die within a single package while the bottom plot shows the total power dissipation due to switching and conduction losses generated on the devices. Here the peak loss for the IGBT and diode is approximately 520W and 100W respectively. The high modulation index results in higher power dissipation on the IGBT than the diode due to longer current conduction times in the switch.



Figure 5: Transient junction temperatures (top), transient total power dissipated (bottom) in the IGBT and Diode  $(PF=0.8 \text{ and } f_{fundamental} = 100 \text{Hz}).$ 

The 180° phase difference in device junction temperatures arises due to direction of current conduction of the individual inverter leg as explained in *Section 2.2*. The inflections in device junction temperature and power dissipation are owed to the space vector pulse width modulation (SVPWM) scheme used by the inverter. While the initial ambient temperature was defined as 85°C, depending on vehicle "under hood" conditions this can be varied over the duration of the simulation if a more realistic temperature profile is desired.

#### 3.2 Motor Simulation Case 2 – Low Speed Operation

For this simulation case, low speed operation is emulated by driving the inverter at a fundamental frequency of 10Hz  $(^{1}/_{10})^{\text{th}}$  the "high speed" case). Figure 6 illustrates how the lower speeds of the PMSM results in an inductive load to appear across the terminals of the inverter resembling a *PF* close to zero between voltage and current waveforms.



Figure 6: Voltage (top) and current (bottom) waveforms for three phase inverter (PF=0.1 and  $f_{fundamental} = 10Hz$ ).

Due to the lower speed operation of the PMSM, both IGBT and diode conduct currents over a longer period of time in comparison to the power devices during the high speed operation case. This condition results in power pulses sustained over larger time durations which corresponds to transient thermal impedances towards far right side of the  $Z_{th}$  curve shown in Figure 3. It should be noted that irrespective of the PMSM's fundamental frequency of operation, due to the power factor between voltage and current waveforms being close to zero, the diode current conduction times are higher than experienced by power devices in the previous simulation case. Both these factors produce higher dissipated power and ripple junction temperatures on the diode as shown in the bottom plot of Figure 7. Even though the power dissipated on the IGBT is lower than the high speed operation simulation case, the corresponding higher transient thermal impedances result in higher ripple temperatures on the IGBT. As a result, from the simulations performed it is evident that lower speed operation produces higher ripple temperatures on both power devices which can translate into reliability concerns for the silicon, bondwires and thermal interfaces of the power device due to thermal stresses induced over the lifetime of operation under this condition.



Figure 7: Transient junction temperatures (top), transient total power dissipated (bottom) in the IGBT and Diode  $(PF=0.1 \text{ and } f_{fundamental} = 10Hz)$ .

#### 4 Conclusions

This work illustrates the use of an electro-thermal model for designing a 3-phase inverter. Thermal simulations are performed in order to derive a model that characterizes the overall thermal response of co-pack IGBTs in Super T0-247 package. A loss model representing the conduction and switching losses of Infineon's AUIRGPS4067D1 IGBT and diode is developed. The thermal and loss models are exercised in a 3-phase inverter system model in order to determine IGBT and diode junction temperatures. Simulation results demonstrate that the thermal response of the devices can be predicted for sophisticated patterns of power pulses and that this knowledge can be used for ensuring robust converter operation and also verifying the devices reliability under worst case operating conditions. This work illustrates the benefits and necessity of performing electro-thermal co-simulation for designing power converters with high power IGBTs for automotive applications.

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SESSION 4

# **SESSION 4** Compact Thermal Modeling

#### Model Order Reduction in Inductors for Rapid Virtual Prototyping in Power Electronics

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#### Abstract

With the need for increasing efficiencies in power electronics combined with the trend for smaller device, optimisation of power electronic systems is needed. This paper considers the steps needed to model inductors for such optimisation techniques. The use of multi-domain methods to combine smaller component models into a larger system model is the first step for such virtual prototyping. For the modelling of the electrical performance of components, Partial Element Equivalent Circuit (PEEC) models have been used. Standard PEEC techniques, however, are not able to model magnetic components. The extension of these methods to incorporate magnetic materials allows for the modelling of inductors using these techniques. Model Order Reduction (MOR) techniques applied to the system matrices produced by PEEC allow for solving transient models quickly without loss of model fidelity. With all three of these techniques, combined rapid virtual prototyping of systems including inductors is possible.

#### 1 Introduction

In order to optimise the layout of power electronics devices it is necessary to take into account the electromagnetic interference and thermal profile of the components. Current modelling techniques are either inaccurate or very time consuming due to the computational requirements. To assist in the rapid virtual prototyping of power electronic circuits new techniques are required to ensure that computation can be done accurately and efficiently. Multi-domain tools that use multiple techniques have proven effective at modelling power electronic devices [1]. Such tools combine both physical and behavioural models depending on the information available to the power electronics designer. Reduction (MOR) technique can allow for the speeding up of simulation time by reducing the size of the system matrix to be solved at each time step. The calculation of the projection matrix reduces the size of the system matrix, but this only occurs before the first time step and can be then reused for each subsequent time step. Using the correct MOR technique gives a much smaller matrix that can be solved very quickly so vastly decreasing the computational time for each time step. Established MOR techniques rely on linear problems and though there are some techniques for non-linear problems they are not yet well established.

The combination of multi-domain tools with MOR allows for the rapid solving of complex power electronic devices. So these techniques once fully developed will enable the rapid prototyping of such devices by the testing of a large

Numerical Method	FDM	FEM	MoM	PEEC
Formulation of Maxwell equation	Differential equation	Differential equation	Integral equation	Integral equation
Solution Variable	Field	Field	circuit	circuit
Solution Domain	Time domain/Frequency domain	Time domain/Frequency domain	Time domain/Frequency domain	Time domain/Frequency domain
Advantages	<ul><li>Easy to use</li><li>Robust</li></ul>	<ul><li>Cell flexibility</li><li>Sparse system</li></ul>	Cell flexibility	Time/ frequency domain combination. Circuit & EM cell flexibility
Disadvantages	<ul> <li>Cell inflexibility</li> <li>Large storage requirement</li> </ul>	• Solution of large linear system	Dense system matrix, computationally heavy	Computationally heavy

Table1: Summary of the main features of common numerical methods used in power electronics modeling

For transient simulations the addition of a Model Order

number of different layouts for the device within a comparatively short amount of computational time. These solutions can then be used with optimisation techniques to suggest optimal circuit designs.

#### 2 Component Models

With multi-domain tools each component can be modelled with its own numerical model. These can then be combined into a larger model to consider the coupling between the components due to temperature, mutual inductance and parasitic capacitance. Each of the currently used techniques for modelling components have their disadvantages and advantages. These are summarised in Table 1.

Behavioural models, such as SPICE type models are based on the properties of an individual component and are usually empirical models based on the response of that individual component to given different inputs. These are usually accurate for the component considered; they are however limited in their accuracy due to limited ability to consider temperature changes and electromagnetic interference from other components.

Finite Difference (FD) schemes are usually quite fast to solve due to the knowledge of the structure of the matrices. However, they rely on either Cartesian or Polar meshes. This results in difficulties with complex geometries requiring either a very fine mesh in these areas thus increasing solution time. or other techniques that make numerical approximations for certain cells. FD schemes can also be solved line-by-line allowing for the linearization of a non-linear FD problem thus allowing linear MOR techniques to be used.

Full Finite Element Analysis (FEA) techniques allow for the meshing of complex geometries accurately and for whole domain solutions. The models produced often result in large matrices that take a long time to solve.

PEEC techniques solve in the circuit domain and so don't need to mesh as large a volume as required by FEA and FD techniques; this results in a smaller, though denser matrix, to solve. The matrices generated however are able to be reduced even further in size by using the correct MOR techniques.

#### **3 PEEC with electromagnetic components**

As a circuit domain modelling technique standard PEEC cannot be used for modelling electromagnetic components such as inductors accurately. Air-core inductors can be modelled using PEEC successfully as the domain external to the wires is not modelled. Standard PEEC cannot be used to model inductors with magnetic cores.

By using virtual circuits to represent the magnetic cores PEEC can be modified to take into account the magnetic core [2]. The current work on this considers solutions in the frequency domain. However, the formulations should also work for transient simulations. The modelling assumptions also mean that the current equations work only for Toroidal shaped inductors.

The modified PEEC technique (see figure 1) takes into account the magnetic medium cores of a toroidal inductor by using boundary element methods combined with virtual circuits to modify the Electric Field Integral Equation (EFIE). The modelling of toroidal cores in this way makes several assumptions. Firstly, that the influence of eddy currents can be neglected and, secondly, that the power losses due to hysteresis and residual losses are both negligible. In addition toroidal cores with uniform windings have a very low magnetic stray field and so the field lines can be assumed to be tangential to the magnetic path. So for the idealised case no magnetic charge exists.

The addition of the magnetic surface currents  $K_m$  leads to an extension of the standard PEEC EFIE adding the mutual inductances  $L_m$  between the fictitious surface currents and the winding currents I [3].

$$V_{n} = R_{n}I_{n} + \sum_{i=1}^{N_{j}} L_{in}\frac{dI_{i}}{dt} + \sum_{i=1}^{N_{s}} Q_{i}[pp_{in}^{+} - pp_{in}^{-}] + \cdots + \sum_{mi=1}^{N_{M}} L_{Kmi\phi,n}\frac{dK_{mi,\phi}}{dt} + \sum_{mi=1}^{N_{M}} L_{Kmi\theta,n}\frac{dK_{mi,\theta}}{dt}.$$
 (1)

The stray field can instead be modelled as factious magnetic charges  $\sigma_{mi}$  on the magnetic panels  $N_{\rm M}$ 

$$V_{n} = R_{n}I_{n} + \sum_{i=1}^{N_{j}} L_{in}\frac{dI_{i}}{dt} + \sum_{i=1}^{N_{s}} Q_{i}[pp_{in}^{+} - pp_{in}^{-}] + \cdots + \sum_{mi=1}^{N_{M}} L_{Kmi\phi,n}\frac{dK_{mi,\phi}}{dt} + \sum_{mi=1}^{N_{M}} L_{\sigma mi,n}\frac{d\sigma_{mi}}{dt}.$$
 (2)

This leads to an equivalent circuit of the inductor as shown in in figure 1.

The addition of the boundary element method for the magnetic currents gives a boundary equation for the mk-th magnetic panel,

$$\left(\frac{\boldsymbol{B}_{J(mk)}}{\mu_0} + \frac{\boldsymbol{B}_{M(mk)}}{\mu_0}\right) \cdot \boldsymbol{n}_{mk} - \left(\frac{1}{2} + \frac{1}{\chi_m}\right) K_{mk} = 0$$
  
$$\Rightarrow \boldsymbol{\lambda}_{MI} \cdot \boldsymbol{I} + \boldsymbol{\alpha}_{MM} \cdot \boldsymbol{K}_M = 0, \qquad (3)$$

where  $\mathbf{B}_{J(mk)}$  is the magnetic induction of the coil and  $\mathbf{B}_{J(mk)}$  is the magnetic induction fo the other panels. This adds new elements  $L_{M_2}$ ,  $\lambda_M$  and  $\alpha_M$  to the standard PEEC system



Figure 1: RLC diagram of modified PEEC technique

matrix.

$$\begin{pmatrix} \mathbf{A} & -(\mathbf{R}+j\omega\mathbf{L}) & -j\omega\mathbf{L}_{\mathbf{M}} \\ (j\omega\mathbf{P}^{-1}+\mathbf{Y}_{\mathbf{L}}) & \mathbf{A}^{T} & \mathbf{0} \\ \mathbf{0} & \lambda_{MI} & \sigma_{MM} \end{bmatrix} \begin{bmatrix} \mathbf{V} \\ \mathbf{I} \\ \mathbf{K}_{M} \end{bmatrix} = \begin{bmatrix} \mathbf{V}_{s} \\ \mathbf{I}_{s} \\ \mathbf{0} \end{bmatrix}.$$
(4)

If the fictitious magnetic charges are introduced the boundary equation becomes

$$(\boldsymbol{H}_{J,mk} + \boldsymbol{H}_{M,mk}) \cdot \boldsymbol{n}_{mk} - \left(\frac{1}{2} + \frac{1}{\chi_{m}}\right) \sigma_{mk} = 0$$
  
$$\Rightarrow \boldsymbol{\lambda}_{MI} \cdot \boldsymbol{I} + \boldsymbol{\gamma}_{MM} \cdot \boldsymbol{\sigma}_{M} = 0.$$
 (5)

This boundary equation leaves to the PEEC system matrix for a magnetic inductor

$$\begin{bmatrix} \mathbf{A} & -(\mathbf{R}+j\omega\mathbf{L}) & -j\omega\mathbf{L}_{\mathbf{M}} \\ (j\omega\mathbf{P}^{-1}+\mathbf{Y}_{\mathbf{L}}) & \mathbf{A}^{T} & \mathbf{0} \\ \mathbf{0} & \lambda_{MI} & \sigma_{MM} \\ \mathbf{0} & \lambda_{\sigma MI} & \gamma_{MM} \end{bmatrix} \begin{bmatrix} \mathbf{V} \\ \mathbf{I} \\ \mathbf{K}_{M} \\ \sigma_{M} \end{bmatrix} = \begin{bmatrix} \mathbf{V}_{s} \\ \mathbf{I}_{s} \\ \mathbf{0} \\ \mathbf{0} \end{bmatrix} (6)$$

This increases the order of the system matrix by  $2N_M$ , due to the increased number of unknowns due to the virtual circuits and charges.

#### 4 Model Order Reduction

Model Order Reduction (MOR) techniques use various mathematical techniques to reduce the order of a system matrix generated by the discretisation of a partial differential or integral equation. They involve the use of projection matrices to reduce the order of a system matrix; this matrix is then solved and then the solution is projected back using the original projection matrix. Figure 2 shows an overview of the steps involved in an MOR technique.

As these techniques are being used with PEEC methods here we consider techniques for use with LTI type equations. There are two main types of these techniques Krylov or moment matching and SVD or Gramian based methods [3]. Krylov techniques use Krylov subspaces to produce a reduced dimension system with a certain number of moments.

For PEEC techniques a technique known as Passive Reduced-Order Interconnect Macromodeling Algorithm (PRIMA) [4] is used. This technique, usually based on Block Arnoldi [5] methods though it does not have to be, is specifically designed for modelling RLC interconnects. Due to this it is the most stable method for reducing the order of PEEC system matrices.

A system of RLC circuits can be modelled as a set of equations

$$C\dot{x}_n = -Gx_n + Bu_n, i_N = L^T x_n, \tag{7}$$

where  $i_n$  represent the port currents  $u_n$  the port voltages and

$$C \equiv \begin{bmatrix} Q & 0 \\ 0 & H \end{bmatrix}, G \equiv \begin{bmatrix} N & E \\ -E^T & 0 \end{bmatrix}, x_n \equiv \begin{bmatrix} \nu \\ i \end{bmatrix},$$
(8)



Figure 2: Diagram of MOR methods

where v and i represent the voltage and current variables.

By assuming we are only interested in the voltage and current variables it can be shown that the y-parameter matrix may be written as

$$Y(s) = L^{T}(G + sC)^{-1}B.$$
 (9)

This can then be written as

$$Y(s) = L^{T}(I_{n} - sA)^{-1}R.$$
(10)

Using a Taylor expansion of Y(s) around s=0 a block Kyrlov subspace is generated

$$\begin{aligned} &Kr(A, R, q) \\ &\equiv coslp[R, AR, A^2R, \dots, A^{k-1}R, A^kr_0, A^kr_1, \dots, A^kr_l], \\ &k = \left[\frac{q}{N}\right]l = 1 - kN. \end{aligned}$$

This Kyrlov supsace can be used to derive the block moments for a block Arnoldi algorithm

$$A^{i}R = XH_{q}^{i}X^{T}R, 0 \le i < \left[\frac{q}{N}\right]$$
(12)

The algorithm itself use LU decomposition of G and q to create the block Kyrlov space.

For the PRIMA algorithm, block Arnoldi is used to generate the matrix X and upper Hessenberg matrix H such that

$$\operatorname{colsp}(X) = Kr(A, R, q), X^{T}X = I_{q}, X^{T}AX = H.$$
(13)

The classical Arnoldi approach gives a reduced order Y(S)

$$\hat{Y}(s) = L^T X (l_n - sH)^{-1} X^T R.$$
(14)

By reducing the conductance and susceptance matrices directly leaves

$$\hat{Y}(s) = \tilde{L}^T \left( \tilde{G} + s \tilde{C} \right)^{-1} B.$$
(15)

As  $\tilde{G}$  and  $\tilde{C}$  are typically very small it is tribulat to find the poles and zeroes of  $\hat{Y}(s)$ .

#### 5 Results

Some initial results for air core inductors using PEEC and MOR are presented here. These results are for a simple toroidal inductor with 10 windings. This inductor has an outer radius of 44.39mm and an outer radius of 75.01 mm its height is 35.92mm, the turns are of a wire of 2.3mm diameter. Figure 3 shows the geometry of the coil windings. The wire is modelled as copper ( $\sigma$ =5.998×10<sup>7</sup>S/m) and air ( $\sigma$  =0S/m) is assumed outside the wire. For the PEEC model and Model Order Reduction VPPE[1] was used with a modified Model Order Reduction algorithm, this was solved using a transient solution. For comparison an FEA model in COMSOL Multiphysics 5.1 was used along with a frequency domain solution. The simulations were run on a 16 Core 3.1GHz XEON workstation.





The magnitude of the impedance for different frequencies of alternating current can be seen in figure 4. As shown the MOR is a good match for both the standard PEEC and the FEA model, however as the frequency increases it diverges slightly from the true solution. This can be corrected by using different preconditioning to the MOR technique however that is not in the scope of this paper. Table 2 shows a comparison of the timings for both cases with and without MOR.



Figure 4: Comparison of the Impedence for FEA, PEEC and PEEC with MOR

For 1 GHz	Without MoR	With MOR
Building Projection Matrix	N/A	0.6s
Solution time	20 s	20e-3s
Total	20s	0.602s

Table 2: Speedup From MOR for the 1GHz solution

As can be seen, the initial generation of the projection matrix results in a small computational cost when using MOR. For comparison the FEA model using 16 cores took 2 minutes for each frequency in a frequency domain model. The PEEC solver is not multithreaded so used a single core.

#### 6 Conclusions and Future Work

This paper has outlined ongoing work aiming to incorporate the modelling of inductors with PEEC and MOR into a system level model. Results have been demonstrated showing the possible speedup from the use of MOR reduction techniques combined with PEEC code.

The authors are currently implementing the extended PEEC and once this has been combined with the MOR technique this will allow for magnetic core inductors to be solved. This having been completed will allow for more typical inductors to be modelled.

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#### Calibration of Detailed Thermal Models by Parametric Dynamic Compact Thermal Models

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#### Abstract

In this paper it is shown how parametric dynamic compact thermal models can be exploited for the calibration of detailed thermal models of electronic components and packages. A constrained least square fit of the thermal response of a parametric dynamic compact thermal model, having as parameters the material thermal properties and geometrical details to be calibrated, onto the measured temperature response is performed. Numerical results show that the use of parametric dynamic compact thermal models instead of detailed compact thermal models, in conjunction with an optimization algorithm solving the constrained least square problem, can reduce the computational time for calibration by more than two orders of magnitude.

#### 1 Introduction

The construction of accurate detailed thermal models of electronic components and packages is crucial in thermalaware design. Unfortunately, commonly in state-of-the-art applications, some material thermal properties or geometry details are not precisely known [1, 2]. For this reason, these parameters of the detailed thermal models have usually to be determined by calibration with respect to experimental data [3]. The calibration procedure can be performed manually or automatically by resorting to an optimization algorithm. In both cases, a significant set of transient thermal simulations of the detailed thermal model of electronic components and packages have to be performed. As a result such calibration procedure can be computationally very expensive.

The Authors have proposed novel families of Model Order Reduction (MOR) techniques for deriving Dynamic Compact Thermal Models (DCTMs) from the detailed thermal models [1, 36] and in particular for deriving DCTMs which are parametric with respect to a limited set of material thermal properties and geometry details. Such approaches are very effective, since they allow deriving accurate parametric DCTMs, in a computational time which is typically orders of magnitude lower than that for one transient simulation of the detailed thermal model in response to a single power step. Moreover, using the derived parametric DCTM, the thermal field in the electronic component or package can be reconstructed for any value of the chosen parameters in negligible computational time.

In this paper the case of linear heat diffusion problems is considered. It is shown how parametric DCTMs can be used instead of the detailed thermal model, in conjunction with an optimization algorithm, in order to perform calibration of the detailed thermal model. This approach presents several advantages with respect to the direct use of detailed thermal

models. Firstly since the ranges in which the parameters are assumed to vary are usually limited, the extraction of parametric DCTMs is particularly efficient, with respect to a single transient solution of the detailed thermal model. Secondly, since the numerical solution of the parametric DCTM requires negligible amounts of time, the time for the calibration procedure is essentially determined by the time for extracting the parametric DCTM. Thirdly, since parametric DCTMs allow accurately reconstructing the whole thermal field of the detailed thermal model, any measured temperature can be used for calibration. Lastly, since the sensitivity of temperature with respect to variations of the parameters can be efficiently computed for the parametric DCTMs at negligible computational time, this information can be provided to the optimization algorithm, for improving robustness and efficiency.

The proposed approach has been validated, on a Package on Package (PoP), showing a speedup of about 200 with respect to the conventional approach.

#### 2 Parametric Heat Diffusion Problems

Let a transient heat diffusion problem be considered in which both the *material thermal properties* and the *geometry details* depend on a limited number *P* of parameters  $p_1, ..., p_P$ , forming a vector **p** which varies in a chosen set  $\mathcal{P}$ . Extending [24] from the stationary to the transient case, it can be shown that such transient heat diffusion problem can be reformulated as an equivalent transient heat diffusion problem in which only the thermal properties vary with **p**, the spatial domain  $\omega$ being fixed. For such a problem the temperature rise  $\vartheta(\mathbf{r}, t, \mathbf{p})$  with respect to the ambient temperature, at each position vector **r** in  $\omega$  and at each time instant *t*, is ruled by the transient heat diffusion equation in which the heat capacity  $c(\mathbf{r}, \mathbf{p})$ , the thermal conductivity  $\mathbf{k}(\mathbf{r}, \mathbf{p})$ , and the power density  $q(\mathbf{r}, \mathbf{p})$  all depend on  $\mathbf{p}$ . Such equation is completed by conditions on the boundary  $\partial \omega$  of outward unit normal vector  $\mathbf{n}(\mathbf{r})$ , here assumed to be homogeneous of Robin's type

$$-\mathbf{n}(\mathbf{r}) \cdot \mathbf{k}(\mathbf{r}, \mathbf{p}) \nabla \vartheta(\mathbf{r}, t, \mathbf{p}) = h(\mathbf{r}, \mathbf{p}) \vartheta(\mathbf{r}, t, \mathbf{p}), \qquad (2)$$

in which the heat exchange coefficient  $h(\mathbf{r}, \mathbf{p})$  depends on  $\mathbf{p}$ , and by an initial condition, which can be assumed to be homogeneous

$$\vartheta(\mathbf{r}, 0, \mathbf{p}) = 0. \tag{3}$$

When a thermal model is defined, thermal ports are introduced. Powers  $P_i(t)$ , with i = 1, ..., n, injected at the ports determine the power density in the form

$$q(\mathbf{r}, t, \mathbf{p}) = \sum_{i=1}^{n} g_i(\mathbf{r}, \mathbf{p}) P_i(t), \qquad (4)$$

 $g_i(\mathbf{r}, \mathbf{p})$  being shape functions, dependent on  $\mathbf{p}$ , such that

$$\int_{\omega} g_i(\mathbf{r}, \mathbf{p}) \, d\mathbf{r} = 1.$$

Following [7], the port temperature rises  $T_i(t)$ , with i = 1, ..., n, are given by

$$T_i(t, \mathbf{p}) = \int_{\omega} g_i(\mathbf{r}, \mathbf{p}) \vartheta(\mathbf{r}, t, \mathbf{p}) \, d\mathbf{r}.$$
<sup>(5)</sup>

It is hereinafter assumed, as it can always be in practical cases [24], that the thermal properties vary with **p** as follows

$$c(\mathbf{r},\mathbf{p}) = \sum_{s=1}^{C} C_s(\mathbf{p}) c_s(\mathbf{r}), \qquad (6)$$

$$\mathbf{k}(\mathbf{r},\mathbf{p}) = \sum_{s=1}^{K} K_s(\mathbf{p}) \mathbf{k}_s(\mathbf{r}), \qquad (7)$$

$$h(\mathbf{r}, \mathbf{p}) = \sum_{s=1}^{H} H_s(\mathbf{p}) h_s(\mathbf{r}), \qquad (8)$$

$$g_i(\mathbf{r}, \mathbf{p}) = \sum_{s=1}^G G_s(\mathbf{p}) g_{is}(\mathbf{r}),$$
  
for  $i = 1, ..., n$  (9)

in which  $C_s(\mathbf{p})$ ,  $K_s(\mathbf{p})$ ,  $H_s(\mathbf{p})$ ,  $G_s(\mathbf{p})$  are functions of  $\mathbf{p}$  and  $c_s(\mathbf{r})$ ,  $\mathbf{k}_s(\mathbf{r})$ ,  $h_s(\mathbf{r})$ ,  $g_{is}(\mathbf{r})$  are functions of the position vector  $\mathbf{r}$ .

As it is well known, only in exceptional situations, in which geometries and material parameters are over-simplified, the transient heat diffusion equations can be solved in closed form. This difficulty can be overcome by discretizing the transient heat diffusion equation using any proper numerical method.

#### **3** Parametric DCTMs

Extending the multi-point moment matching algorithm proposed in [24] from the stationary to the transient case, a parametric DCTM can be extracted for the thermal model defined by equations (1)-(3), with port variables (4), (5), and parametric dependences (6)-(9). To this aim a set of basis functions  $v_i(\mathbf{r})$  defined in  $\omega$ , with i = 1, ..., M, is computed

and Eq. (1) is projected onto the space spanned by these basis functions. In this way the parametric DCTM takes the form

$$\hat{\mathbf{C}}(\mathbf{p}) \frac{\partial \hat{\vartheta}}{\partial t}(t, \mathbf{p}) + \left( \hat{\mathbf{K}}(\mathbf{p}) + \hat{\mathbf{H}}(\mathbf{p}) \right) \hat{\vartheta}(t, \mathbf{p}) = = \hat{\mathbf{G}}(\mathbf{p}) \mathbf{P}(t),$$
(10)

$$\widehat{\mathbf{T}}(t,\mathbf{p}) = \widehat{\mathbf{G}}^T(\mathbf{p})\widehat{\vartheta}(t,\mathbf{p})$$
(11)

in which  $\mathbf{P}(t)$  is the vector of powers  $P_1(t), ..., P_N(t)$ , and  $\widehat{\mathbf{T}}(t, \mathbf{p})$  is the vector of temperatures  $\widehat{T}_1(t, \mathbf{p}), ..., \widehat{T}_N(t, \mathbf{p})$ , approximations temperatures  $T_1(t, \mathbf{p}), ..., T_N(t, \mathbf{p})$ . Matrices  $\widehat{\mathbf{C}}(\mathbf{p}), \widehat{\mathbf{K}}(\mathbf{p}), \widehat{\mathbf{H}}(\mathbf{p})$  are *M*-order matrices given by

$$\widehat{\mathbf{C}}(\mathbf{p}) = \sum_{s=1}^{C} C_s(\mathbf{p}) \widehat{\mathbf{C}}_s, \qquad (12)$$

$$\widehat{\mathbf{K}}(\mathbf{p}) = \sum_{s=1}^{K} K_s(\mathbf{p}) \widehat{\mathbf{K}}_s, \qquad (13)$$

$$\widehat{\mathbf{H}}(\mathbf{p}) = \sum_{s=1}^{H} H_s(\mathbf{p}) \widehat{\mathbf{H}}_s, \qquad (14)$$

in which  $\hat{\mathbf{C}}_s = [\hat{c}_{ijs}]$ ,  $\hat{\mathbf{K}}_s = [\hat{k}_{ijs}]$ ,  $\hat{\mathbf{H}}_s = [\hat{h}_{ijs}]$ , are symmetric, positive semi-definite matrices of order *M* having the following elements at each *i*-th row and *j*-th column

$$\hat{c}_{ijs} = \int_{\omega} \nabla v_i(\mathbf{r}) c_s(\mathbf{r}) \nabla v_j(\mathbf{r}) \, d\mathbf{r},$$
  

$$\hat{k}_{ijs} = \int_{\omega} \nabla v_i(\mathbf{r}) \cdot \mathbf{k}_s(\mathbf{r}) \nabla v_j(\mathbf{r}) \, d\mathbf{r},$$
  

$$\hat{h}_{ijs} = \int_{\partial \omega} v_i(\mathbf{r}) h_s(\mathbf{r}) v_j(\mathbf{r}) \, d\mathbf{r}.$$

Matrix  $\widehat{\mathbf{G}}(\mathbf{p})$  is an  $M \times N$  matrix given by

$$\widehat{\mathbf{G}}(\mathbf{p}) = \sum_{s=1}^{G} G_s(\mathbf{p}) \widehat{\mathbf{G}}$$
(15)

in which  $\widehat{\mathbf{G}}_s = [\widehat{g}_{ijs}]$ , are  $M \times N$  matrix, having the following elements at each *i*-th row and *j*-th column

$$\hat{g}_{ijs} = \int_{\omega} v_i(\mathbf{R}) g_{is}(\mathbf{r}) \, d\mathbf{r}.$$

Vector  $\hat{\vartheta}(t, \mathbf{p})$  is formed by *M* Degrees of Freedom (DoF). The initial condition for the parametric DCTM is

$$\vartheta(0,\mathbf{p}) = 0. \tag{16}$$

The multi-point moment matching algorithm proposed in [24] for the extraction of the parametric DCTM is robust, efficient and accurate. In fact it applies to arbitrarily complex geometries. Parametric DCTMs of small dimensions M are extracted in a fraction of the time needed for a single transient simulation of a detailed thermal model. The relative error  $\varepsilon$  tolerated in the approximation of the thermal field, provided by the parametric DCTM, can be arbitrarily chosen. Any practical level of accuracy can be achieved, since the relative error  $\varepsilon$  exponentially decreases with the dimension M of the parametric DCTM.

#### 4 Inverse Heat Diffusion Problems

The calibration procedure can be formalized as an inverse heat diffusion problem. In fact the calibrated parameters can be assumed as the value of the parameters  $\mathbf{p}$  in the set  $\mathcal{P}$ solving the constrained least square problem

$$\min_{\mathbf{p}\in\mathcal{P}}\sum_{q=1}^{Q} \left( \widehat{\mathbf{T}}(t_q, \mathbf{p}) - \mathbf{T}(t_q) \right)^T (\widehat{\mathbf{T}}(t_q, \mathbf{p}) - \mathbf{T}(t_q))$$
(17)

in which  $\mathbf{T}(t)$  is the vector of N port temperatures, measured at time instants  $t_1, ..., t_Q$  and  $\mathbf{\hat{T}}(t, \mathbf{p})$  is the vector of the values of the N port temperatures provided by the parametric DCTM. Several constrained least square algorithms have been proposed in literature for solving inverse heat conduction problems. In this paper a widespread trust region algorithm [37, 38] is adopted.

Constrained least square algorithms need the computation of  $\hat{\mathbf{T}}(t, \mathbf{p})$  for some requested values of  $\mathbf{p}$ . This could be efficiently done, by approximating the solution of the linear system of ordinary differential equations (10), (11), by a proper numerical solver. Nevertheless, in order to further gain efficiency this can be performed analytically. To this aim, for the assigned value of  $\mathbf{p}$ , an *M*-order matrix  $\hat{\mathbf{V}}$  is determined as the solution of the generalized eigenvalue problem

$$\widehat{\mathbf{V}}^T \widehat{\mathbf{C}}(\mathbf{p}) \widehat{\mathbf{V}} = \mathbf{I},$$
  
 $\widehat{\mathbf{V}}^T (\widehat{\mathbf{K}}(\mathbf{p}) + \widehat{\mathbf{H}}(\mathbf{p})) \widehat{\mathbf{V}} = \mathbf{\Lambda},$ 

in which  $\Lambda$  is a diagonal, positive definite matrix. As it can be straighforwardly verified, using  $\hat{\mathbf{V}}$  as a transformation matrix, the value of  $\hat{\mathbf{T}}(t, \mathbf{p})$  at the requested value of  $\mathbf{p}$  can be expressed as

$$\widehat{\mathbf{T}}(t,\mathbf{p}) = \widehat{\mathbf{V}}^T \widehat{\mathbf{G}}^T(\mathbf{p}) \exp(-\Lambda t) \widehat{\mathbf{G}}(\mathbf{p}) \widehat{\mathbf{V}} * \mathbf{P}(t),$$

in which \* is the convolution operator in the time domain. Such convolution operation can be computed in closed-form for the most common choices of power vectors  $\mathbf{P}(t)$ , such as piece-wise constant functions hereafter considered.

In order to improve the robustness of constrained least square algorithms, the sensitivity matrix

$$\frac{\partial \widehat{\mathbf{T}}}{\partial \mathbf{p}}(t, \mathbf{p}) = \begin{bmatrix} \frac{\partial \widehat{\mathbf{T}}}{\partial p_1}(t, \mathbf{p}) & \cdots & \frac{\partial \widehat{\mathbf{T}}}{\partial p_p}(t, \mathbf{p}) \end{bmatrix}$$

has to provided at the requested values of **p**. To this aim, deriving both members of Eqs. (10), (11), (16) with respect to parameters  $p_r$ , with r = 1, ..., P, it follows

$$\widehat{\mathbf{C}}(\mathbf{p})\frac{\partial}{\partial t}\frac{\partial\widehat{\partial}}{\partial p_r}(t,\mathbf{p}) + \left(\widehat{\mathbf{K}}(\mathbf{p}) + \widehat{\mathbf{H}}(\mathbf{p})\right)\frac{\partial\widehat{\partial}}{\partial p_r}(t,\mathbf{p}) =$$
(18)

$$= -\frac{\partial \hat{\mathbf{C}}}{\partial p_r}(\mathbf{p})\frac{\partial \hat{\vartheta}}{\partial t}(t,\mathbf{p}) - \left(\frac{\partial \hat{\mathbf{R}}}{\partial p_r}(\mathbf{p}) + \frac{\partial \hat{\mathbf{H}}}{\partial p_r}(\mathbf{p})\right)\hat{\vartheta}(t,\mathbf{p}) +$$

$$+\frac{\partial \mathbf{u}}{\partial p_r}(\mathbf{p})\mathbf{P}(t),$$

$$\frac{\partial \mathbf{\hat{r}}}{\partial p_r}(t, \mathbf{p}) = \mathbf{\hat{G}}^T(\mathbf{p}) \frac{\partial \hat{\vartheta}}{\partial p_r}(t, \mathbf{p}) + \frac{\partial \mathbf{\hat{G}}^T}{\partial p_r}(\mathbf{p}) \hat{\vartheta}(t, \mathbf{p})$$
(19)  
with initial conditions

$$\frac{\partial\widehat{\vartheta}}{\partial p_r}(0,\mathbf{p}) = 0. \tag{20}$$

From Eqs. (18)-(20), it ensues that, once  $\hat{\mathbf{T}}(t, \mathbf{p})$  is determined, each  $\partial \hat{\mathbf{T}}(t, \mathbf{p}) / \partial p_r$  function can be determined by solving a linear system of ordinary differential equations, differing from (10), (11), (16) only for the known terms on the right hand sides. The approximation of the solution to

Eqs. (18)-(20), could be performed numerically by a proper solver. Nevertheless, in order to further gain efficiency this computation can be performed analytically. As it can be verified, the value of  $\partial \hat{\mathbf{T}}(t, \mathbf{p}) / \partial p_r$  at the requested value of  $\mathbf{p}$  is

$$\begin{split} \frac{\partial \hat{\mathbf{T}}}{\partial p_r}(t,\mathbf{p}) &= \left(\frac{\partial \hat{\mathbf{G}}^T}{\partial p_r}(\mathbf{p}) \widehat{\mathbf{V}}^T \exp(-\Lambda t) \widehat{\mathbf{V}} \widehat{\mathbf{G}}(\mathbf{p}) + \\ &+ \widehat{\mathbf{G}}^T(\mathbf{p}) \widehat{\mathbf{V}}^T \exp(-\Lambda t) \widehat{\mathbf{V}} \frac{\partial \widehat{\mathbf{G}}}{\partial p_r}(\mathbf{p}) \right) * \mathbf{P}(t) + \\ &- \widehat{\mathbf{G}}^T(\mathbf{p}) \widehat{\mathbf{V}}^T \left( \widehat{\mathbf{V}}^T \frac{\partial \widehat{\mathbf{C}}}{\partial p_r}(\mathbf{p}) \widehat{\mathbf{V}} \circ \frac{d \widehat{\mathbf{\Phi}}}{dt}(t) + \\ &\widehat{\mathbf{V}}^T \left( \frac{\partial \widehat{\mathbf{R}}}{\partial p_r}(\mathbf{p}) + \frac{\partial \widehat{\mathbf{H}}}{\partial p_r}(\mathbf{p}) \right) \widehat{\mathbf{V}} \circ \widehat{\mathbf{\Phi}}(t) \right) \widehat{\mathbf{V}} \widehat{\mathbf{G}}(\mathbf{p}) * \mathbf{P}(t). \end{split}$$

in which  $\circ$  is the matrix element-wise product and  $\widehat{\Phi}(t) = [\widehat{\varphi}_{ij}(t)]$  is an *M*-order matrix having the following elements at the *i*-th row and *j*-th column

$$\hat{\varphi}_{ij}(t) = \frac{\exp(-\lambda_i t) - \exp(-\lambda_j t)}{\lambda_i - \lambda_j}.$$
(21)

It is noted that for i = j Eq. (22) loses meaning. In this case the limit for  $\lambda_j \rightarrow \lambda_i$  has to be taken into account so that

$$\hat{\varphi}_{ii}(t) = -t \exp(-\lambda_i t).$$

Again the convolution operations can be computed in closedform for the most common choices of power vectors  $\mathbf{P}(t)$ . Also it is noted that, as a consequence of Eqs. (12)-(15), the derivatives of matrices  $\hat{\mathbf{C}}(\mathbf{p})$ ,  $\hat{\mathbf{K}}(\mathbf{p})$ ,  $\hat{\mathbf{K}}(\mathbf{p})$  and  $\hat{\mathbf{G}}(\mathbf{p})$  with respect to each  $p_r$  parameter can be straighforwardly computed by determining the derivatives of the scalars  $C_s(\mathbf{p})$ ,  $K_s(\mathbf{p})$ ,  $H_s(\mathbf{p})$ , and  $G_s(\mathbf{p})$ .

#### 5 Numerical Results

A PoP with two dies is here taken into account. A detailed heat conduction model is constructed by the finite volume approach using about 0.5M unknowns. A calibration of such detailed thermal model is performed with respect to the three heat exchange coefficients on the top, bottom, and sides of the PoP, assumed to vary in the ranges defined in Table 1.

To this aim, firstly the time-varying powers dissipated by the two dies and the heat exchange coefficients on the top, bottom and sides of the PoP are chosen as follows. Power  $P_1(t)$  is a step of amplitude 2 W and power  $P_2(t)$  is a step of amplitude 1 W. Heat exchange coefficients are  $p_1 = 10$  W/ $m^2K$ ,  $p_2 = 200$  W/ $m^2K$ ,  $p_3 = 100$  W/ $m^2K$ . With such choice of powers and heat exchange coefficients, an accurate transient simulation of the detailed thermal model is performed in about 2 hours. The computed port temperature rises  $T_1(t)$  and  $T_2(t)$  are sampled at Q = 1000 time instants logarithmically spaced between  $t_1 = 10^{-3}$  s and  $t_Q = 10^3$  s.

Secondly a parametric DCTM of the PoP is extracted, having as parameters the three heat exchange coefficients.

The parametric DCTM is extracted in less than 10 min on a 2.3 GHz Intel Core i7. It has two thermal ports, 46 DoFs, and ensures a relative error, in the approximation of the heat impulse responses, lower than  $\varepsilon = 0.1\%$ . The high accuracy of the approximation can be appreciated by Fig. 1, in which the port temperature rises of the parametric DCTM and of the detailed thermal model of the PoP are compared for a choice of step-wise constant powers injected at the ports, and of heat exchange coefficients.

Table 1: Ranges for the heat exchange coefficients  $p_1$ ,  $p_2$ ,  $p_3$  on the top, bottom and sides of the PoP.

	Minimum $(W/m^2K)$	Maximum $(W/m^2K)$
$p_1$ (top)	5	104
$p_2$ (bottom)	1	10 <sup>3</sup>
p <sub>3</sub> (sides)	5	$2 \cdot 10^2$



Figure 1: Port temperature rises of the parametric DCTM and of the detailed thermal model of the PoP for a choice of step-wise constant port powers and of heat exchange coefficients.

Such parametric DCTM is used for calibration as follows. The constrained least square problem for fitting the thermal response of the detailed model by the parametric DCTM is solved in 16 iterations of the trusted region algorithm, in less than 10 s. Practically the exact values of the chosen parameters  $p_1$ ,  $p_2$ ,  $p_3$  are reconstructed in this way, as shown in Table 2. As a result, the computational time for the solution of the calibration problem is essentially that for the extraction of the parametric DCTM. This time can be compared to the about 32 hours, necessary for the trust region algorithm to reach convergence when the detailed thermal model is directly used instead of the parametric DCTM, with a speedup of about 200.

In order to measure the robustness of the proposed approach, random gaussian noise with increasing values of standard deviation  $\sigma$  are summed at each time step  $t_1, ..., t_Q$ , to the thermal response of the detailed thermal model, as shown in Fig. 2. The solution of the constrained least square problem is then repeated using such noisy thermal responses. The reconstructed values of the DCTM parameters by means of the trust region algorithm are reported in Table 2. It is thus clear than even noises with large standard deviations leads to accurate estimations of the chosen parameters.



Figure 2: Response of the detailed thermal model summed to random gaussian noise with various values of standard deviation  $\sigma$ .

Table 2 Reconstructed values of  $p_1$ ,  $p_2$ ,  $p_3$  for different values  $\sigma$  of the standard deviation of noise.

	$\sigma = 0 \text{ K}$	$\sigma = 0.05$ K	$\sigma = 0.5$ K	$\sigma = 2.5$ K
$p_1 (W/m^2K)$	10.00	9.847	10.38	11.51
$p_2 (W/m^2K)$	200.0	198.0	203.1	182.6
$p_3 (W/m^2K)$	100.0	101.6	96.64	95.48

Similar behavior is observed even for extreme choices of powers and parameters. Let power  $P_1(t)$  be a a step of amplitude 5 W and power  $P_2(t) = 0$  W, heat exchange coefficients  $p_1 = 10^3$  W/m<sup>2</sup>K,  $p_2 = 2$  W/m<sup>2</sup>K,  $p_3 = 50$  W/m<sup>2</sup>K. An accurate transient simulation of the detailed thermal model with such choice of powers and heat exchange coefficients is again performed in about 2 hours. The computed port temperature rises  $T_1(t)$  and  $T_2(t)$  are again sampled at Q = 1000 time instants logarithmically spaced between  $t_1 = 10^{-3}$  s and  $t_Q = 10^3$  s.

The constrained least square problem for fitting the thermal response of the detailed model by the parametric DCTM is solved in 18 iterations of the trusted region algorithm, in less
than 12 s. Practically the exact values of the chosen parameters  $p_1$ ,  $p_2$ ,  $p_3$  are obtained in this way (Table 3). The computational time for the solution of the calibration problem is again essentially that for the extraction of the parametric DCTM. This time can be compared to the about 32 hours, necessary for the trust region algorithm to reach convergence when the detailed thermal model is directly used instead of the parametric DCTM, the speedup begin about 220.

Also, random gaussian noise with increasing values of standard deviation  $\sigma$  are summed at each time step  $t_1, ..., t_Q$  to the thermal response of the detailed thermal model, as shown in Fig. 3. The solution of the constrained least square problem is then repeated using such noisy thermal responses. The reconstructed values of the DCTM parameters by means of the trust region algorithm are reported in Table 3.



Figure 3: Response of the detailed thermal model summed to random gaussian noise with various values of standard deviation  $\sigma$ .

Table 3 Reconstructed values of  $p_1$ ,  $p_2$ ,  $p_3$  for different values  $\sigma$  of the standard deviation of noise.

	$\sigma = 0 \ \mathrm{K}$	$\sigma = 0.05$ K	$\sigma = 0.5$ K	$\sigma = 5 \ \mathrm{K}$
$p_1 (W/m^2K)$	1000	998.6	980.4	947.5
$p_2 (W/m^2K)$	2.000	1.900	1.486	1.028
$p_3 (W/m^2K)$	50.00	51.47	58.74	56.21

#### 6 Conclusions

In this paper parametric DCTMs have been exploited for the calibration of detailed thermal models of electronic components and packages. A constrained least square fit of the thermal response of a parametric DCTM, having as parameters the material thermal properties and geometrical details to be calibrated, onto the measured temperature response has been performed. Numerical results have shown that the use of parametric DCTMs instead of detailed compact thermal models, in conjunction with an optimization algorithm solving the constrained least square problem, can reduce the computational time for calibration by more that two orders of magnitude.

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## **Evolution of the DELPHI Compact Thermal Modelling Method: an Investigation on the Boundary Conditions Scenarios**

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#### Abstract

Board-level simulation has to consider, at the earliest stage of the conception, the impact of the vicinity of numerous high and medium powered devices. In 1996, the concept of Compact Thermal Model was defined, by the European consortium DELPHI to minimize the computation times, from days to minutes. A CTM resumes an electronic component as a simple cuboid form and a network of resistors that links a single temperature-sensitive node to major surfaces of heat extraction. Unfortunately the DELPHI method is restricted to steady-state model for mono-chip component. More complex issues such as multi-chip module or transient thermal model remain today for worldwide companies a non-trivial challenge. Our latest improvements made to generate steady-state multi-source CTM for System-In-Package devices showed that the number of boundary-condition scenarios is quite prohibitive when several nodes need to be monitored. The present work investigates the use of fractional factorial experiment, such as N-variables Doehlert design. The objective of this study is to define the lowest number of numerical simulations while keeping the highest accuracy level of the derived Boundary-Condition-Independent thermal network.

#### 1 Thermal modeling of electronic component

The creation of thermal model of electronic chip-carrier has always be a prime concern for thermal experts. The available standard thermal parameter, called Junction-to-Ambient resistance, does not permit to accurately interpret how the chip-heat is spread away from the package and the creation of relevant Detailed Thermal Models (DTM) is mandatory.

A DTM is an attempt to reconstruct the physical geometries of the actual package as well as the material properties of its constituents. The numerical representation requires the building of a many-thousand nodes model and a one-day computing time, in order to efficiently capture the temperatures and heat fluxes of the chip and its package.

A board-level simulation which involves thousands of component packages would be excessive if each package part is finely defined. This is why the concept of Compact Thermal Model (CTM) was established by the DELPHI Consortium, in 1996.

A CTM is an abstraction of a component thermal behaviour based on detailed component modelling and experiment test results. To build a compact model, DELPHI's approach promotes the use of a thermal resistances network which links the component exterior surfaces to a sensitive node, called junction.

As final results the DELPHI consortium established:

• the definition of a set of 48 boundary conditions using uniform heat transfer coefficients,

- the principle of a subdivision of the outer surfaces in a set of isothermal areas to improve compact model representativeness,
- a recommended objective (or cost) function, which weights the conventional junction temperature and heat fluxes leaving the package from all the surface nodes.

In 2008, the Delphi's CTM methodology was standardized by the JEDEC committee, as JESD15-4 guideline [1], in order to provide a clear guidance to those seeking to create Boundary-Condition-Independent multi-node network.

The proposed steps for CTM generation are outlined below:

- Step 1: Create a realistic numerical Detailed Thermal Model.
- Step 2: Define the objective function that is to be minimized during the optimization.
- Step 3: Define training and test boundary conditions sets in terms of heat transfer coefficient values.
- Step 4: Define number and locations of the external surface and internal sensitive nodes.
- Step 5: Simulate detailed model under training and test boundary conditions to generate heat flux and temperature data.
- Step 6: Choose appropriate statistical optimization technique.
- Step 7: Execute optimization using training boundary condition set.
- Step 8: Define error estimation method.
- Step 9: Generate error estimate using test boundary condition set.

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• Step 10: Make compact model available for dissemination in neutral file format.

The deducted steady-state compact model has to be valid for a given set of thermal environments, in fact, a "universal" set of 38 boundary conditions.

#### 2 38-set test boundary-conditions scenarios

The JEDEC 38-set reflects the spectrum of Fourier-type boundary conditions encountered by the package in typical electronics applications.

Four grouped surface areas of the package are defined and identified as the top, the bottom, the sides or the leads as described in Table 2.

Thus different heat transfer coefficients are successively applied on these external surfaces, which are varying from 1 to  $10^9$ W/m<sup>2</sup>.K. Thus the fitting domain seems to be very vast but in reality many scenarios are very concentrated geographically as shown on Figure 1.



Figure 1: Three-dimensional representation of 37Jedec top, bottom and sides values

For convenience, the domain lower ( $vl = \log hl$ ) and upper ( $vu = \log hu$ ) limits of each factor have been normalized for varying from -1 to 1.

According to the set of JEDEC heat transfer coefficients ( $v_n' = \log h_n'$ ), the blue-dot calculation is done using the following expression:

$$X_p = \frac{2 \cdot v_p' - \left[ v u_p + v l_p \right]}{\left[ v u_p - v l_p \right]}$$
(1)

with 
$$hl_p \le {h_p}' \le hu_p$$
 for  $1 \le p \le 3$ 

The Dirichlet-type scenario according to a heat transfer coefficient of  $10^9$ W/m<sup>2</sup>.K on each component external surface is the right highest point (1,1,1) of the Figure 1.

#### 3 In-house process flow for DELPHI CTM

As a DELPHI end-user partner, we pursue our own research to address the ceaseless needs of electronic board designers.

In order to perform, more efficiently, the step 6 of the CTMgeneration, the adoption of a Genetic Algorithm (GA) optimisation was done in 2006. The feasibility and potential of applying GA as a powerful tool to derive compact thermal for a plastic Micro Lead Frame package of 16 leads was initially published by Arunasalam et al [2]. These nature-inspired algorithms are the object of an always increasing interest in particular to approach problems in the field of heat transfers, as reported by Gosselin et al [3].

Initially, the DELPHI's 48-set of boundary conditions was used to generate our compact thermal model. However, DELPHI's methodology is based on the intensive use of Fourier-type boundary conditions but has to satisfy the Dirichlet-type one, too. A  $49^{th}$  scenario, where a heat transfer coefficient of  $10^9$ W/m<sup>2</sup>.K is applied uniformly on each component external surface, was implemented to solve that problematic.

Complementary investigations [4][5] demonstrate that the temperature of outer surfaces must be taken into account in the objective function (Step 2) to better match the physical behavior of the DTM. The final form of the weighted-sum objective function is expressed as:

$$F(\theta, Q) = W \cdot f(\theta) + (1 - W) \cdot f(Q)$$
<sup>(2)</sup>

Where the function  $f(\theta)$  accounts the discrepancies of the average temperature of every external surfaces as well as the maximum junction temperature one. The function  $F(\theta, Q)$  is the fitness score with 1 as optimum and W is the temperature weight factor.

Its performance for deducting steady-state resistances network was performed on a conventional Micro Lead Frame package of 48 leads [5][6].

The GA CTM-creation process dedicated to mono-chip package was automated and the supplying of a corporate thermal models database was launched. The main benefits were an easier model creation, a daily-based delivered BCI-CTMs and their reuse across multiple projects.

The automated process allows us to select indifferently the 49-set or 38-set of boundary conditions as training (Step 3) or test (step 9) scenarios.

Further, recent works highlighted that asymmetric-chip packages demand a smart definition of inner-outer subdivisions of the package surfaces (Step 4) to adequately characterize the heat fluxes and so keeps the  $F(\theta, Q)$  score close to 1.

A new GA optimization algorithm was developed to automatically determine the most compliant set of isothermal surfaces [7][8] of the network-including box.

The impact on the accuracy of CTM predictions of a GAoptimized subdivision of the package top and bottom surfaces is reported in the present study.

#### 4 **Extension of the DELPHI's cutting-edge spirit**

Moreover the recent 3D technology packaging trend such as System-In-Package (SIP) has intensified the need for suitable behavioural models [8].

SIP packages, comprising many embedded active packages, required to revise the Step 4 in order to e a more complex steady-state thermal network using internal nodes and an optimized subdivision of its surfaces.

Moreover, the mono-source optimization of the Step be completed by the use of linear superposition p Indeed, every chip of the package is at first active, successively each one is powered on when the or kept idle.

Eventually, the function  $f(\theta)$  has to take into acc discrepancies of n-junction temperatures.

Thus the creation of an n-source thermal resistances is achieved from a wide set of boundary conditions 38-set) which needs expensive computation time.

The definition of a reduced x-set of boundary conditions for the training stage (Step 3) is the topic of the next sections.

#### 5 New training boundary-conditions scenarios

An investigated way to reduce the boundary-condition scenarios number is to use a conventional fractional factorial set of experiments [9], such as proposed by Doehlert, for optimizing various design.

For instance, a Doehlert's four-level fractional factorial design is based on 21 experiments as reported in Table 1.

At the opposite of JEDEC boundary-condition scenarios, the Doehlert's experience cases are better spread in the domain analysis as displayed in Figure 2.



Figure 2: Three-dimensional representation of Doehlert's three-level values  $(1 \le p \le 3)$ 

	5	0.5	0.2887	0.2041
chips or	6	-1	0	0
elaborate	7	-0.5	-0.8667	0
n-source	8	-0.5	-0.2887	-0.8165
exterior	9	-0.5	-0.2887	-0.2041
	10	0.5	-0.866	0
5 has to	11	0.5	-0.2887	-0.8165
orinciple.	12	0.5	-0.2887	-0.2041
and then thers are	13	-0.5	0.866	0
	14	0	0.5774	-0.8165
	15	0	0.5774	-0.2041
ount the	16	-0.5	0.2887	0.8165
	17	0	-0.5774	0.8165
network	18	0	0	0.6124
((n+1) x	19	-0.5	0.2887	0.2041
~ /	20	0	-0.5774	0.2041
	21	0	0	-0.6124

p=1

0

1

0.5

0.5

case

1

2

3

4

Table 2 presents a new set of experiments which should be applied to the component-model external surfaces if the lower and upper limits of the heat transfer coefficient range are fixed respectively at 10 and  $10^8$ W/m<sup>2</sup>.K.

Table 2: 21-set of the deducted heat transfer coefficients

	Heat transfer coefficient per face $(W/(m^2.K))$			
case	Тор	Top Bottom Sides		Leads
1	31623	31623	31623	31623
2	10000000	31623	31623	31623
3	1778279	34154663	31623	31623
4	1778279	323929	22790298	31623
5	1778279	323929	163814	18496945
6	10	31623	31623	31623
7	562	29	31623	31623
8	562	3087	44	31623
9	562	3087	6104	54
10	1778279	29	31623	31623
11	1778279	3087	44	31623
12	1778279	3087	6104	54
13	562	33962527	31623	31623
14	31623	3318180	44	31623
15	31623	3318180	6104	54
16	562	323929	22790298	31623
17	31623	301	22790298	31623
18	31623	31623	4399466	54
19	562	323929	163814	18496945
20	31623	301	163814	18496945
21	31623	31623	227	18496945

Table 1: 21-set of Doehlert's geometrical coefficients

p=2

0

0

0.8667

0.2887

Four-level values

p=3

0

0

0

0.8165

p=4

0

0

0

0

0.7906

0

0

0

-0.7906

0

0

-0.7906

0

0

-0.7906

0

0 -0.7906

0.7906

0.7906

0.7906

#### 6 Calculation corner

The numerous numerical simulations are performed using Icepak® V17 software, a Computational Fluid Dynamics (CFD) tool from Ansys®.

#### 7 Main results and discussion

The investigation is carried out to derive thermal resistances networks dedicated to a Quad Flat No-lead package. This symmetrical single-chip package has a set of buried leads which not sticks out from its resin-body as seen on Figure 3.



Figure 3: Three-dimensional constitution of QFN-style package without any chip-lead gold wires

The die paddle area is not submitted to a specific set of boundary conditions as proposed by Janssen et al [10].

The characteristics of the studied 16-lead QFN package are given in Table 3. The lead pitch is equal to 0.65mm.

Table 3: Properties of 16-lead QFN package model

OEN16	L	W	Н	k
QFN10	(mm)	(mm)	(mm)	(W/(m.k))
Chip	1.75	2	0.3	148 @ 27°C
Glue	1.75	2	0.030	2.1
Diepad	2.25	2.5	0.2	260
Lead	0.23	0.4	0.2	260
Body	4	4	0.85	0.66

Table 4 provides the various comparisons made for identifying the most appropriate training-set of boundary conditions and the BCI-property of the derived network.

Table 4: Investigated process flow for the CTM generation

	Training BCs	Testing BCs
	(Step 3)	(Step 9)
Trial 1	49-set	38-set
Trial 2	38-set	49-set
Trial 3	38-set	21-set
Trial 4	21-set	38-set

#### 7.1 Trial N°1: In-house CTM generation

A six-node network was derived from DELPHI's 49-set scenarios, the latter is supplied in Appendix A.

Then its performances were compared with numerical results for the JEDEC 38-set scenarios.

The selected nodes are the junction, the grouped-sides and two subdivided areas, named inner and outer, for the two remaining top and bottom surfaces, as reported Figure 4.



Figure 4: Mean temperature prediction discrepancy of the 49-set deducted CTM on the 38-set scenarios.

Figure 4 reveals that the proposed steady-state CTM enables to estimate others boundary-condition scenarios while keeping a good agreement with DTM numerical results.

#### 7.2 Trial N°2: JEDEC CTM generation

This time the six-node network is generated from JEDEC's 38-set scenarios and tested using DELPHI's 49-set scenario.



*Figure 5: Mean temperature prediction discrepancy of the 38-set deducted CTM on the 49-set scenarios.* 

As for the trial N°1, the Figure 5 shows that the junction temperature predictions of the derived six-node CTM are quite good but the selected scenarios of DELPHI's or JEDEC's are very similar.

#### 7.3 Trial N°3: Boundary condition independence

In order to check the boundary-condition independence of our derived CTM, the previous six-node network has been tested with DOEHLERT's 21-set scenarios as seen Figure 6.



*Figure 6: Mean temperature prediction discrepancy of the 38-set deducted CTM on the 21-set scenarios.* 

It appears clearly that the discrepancies are higher, in particular for the average temperature of the external surface and consequently for heat fluxes leaving the package. The main issue is due to the weak coverage of domain regions by the JEDEC 38-set training scenarios.

#### 7.4 Trial N°4: a new way for scenario selection

The six-node network is created from DOEHLERT's 21-set scenarios then tested using the JEDEC's 38-set scenarios.



*Figure 7: Mean temperature prediction discrepancy of the 21-set deducted CTM on the 38-set scenarios.* 

The use of a set of experiments well-sampled within the domain region enables to reduce the CTM inexactness.

#### 7.5 Trial N°4: CTM predictions improvement

As mentioned, a GA optimization algorithm allows us to automatically determine the set of relevant isothermal external surfaces. The process result is the definition of a new node named bottom mean, as displayed in Figure 8.

The deducted seven-node network is given in Appendix B.



*Figure 8: Mean temperature prediction discrepancy of the 21-set deducted improved CTM on the 49/38-set scenarios.* 

The combination of the 21-set scenarios and a smart subdivision of the box external surfaces permits to reach a better accuracy level whatever the testing set of scenarios.

#### 8 Experimental feedback on QFN16 device

A DTM-CTM comparison with infrared measurements [11] has been conducted considering a more complex QFN16 case mounted on demonstration Printed Circuit Board.

Thus the numerical model takes into account the chip design and its electrical connexion to the leads, as drawn Figure 9.



Figure 9: Conception of a realistic over-moulded IC device

The results highlight the relevance of our in-house process to create DELPHI style Compact Thermal Model and their capability to properly identify its main hot spots.

#### 9 Practical steps for Dynamic-CTM supply

The creation of Dynamic CTM is considered as following the Step 10 of steady-state CTM's generation process. As Step 11, a specific objective function [12] based on transient node temperature was defined for determining a set of added thermal capacitances dedicated to each node of the deducted thermal resistances network.

The developed DCTM's networks were conceived from a temporal response of a detailed component model using, as Step 12, a training 10-set of boundary conditions [12].

The current scenario investigation, based on Doehlert's fractional factorial design, offers us a new perspective for efficiently optimizing the capability to derive DELPHI-style dynamic multi-source compact thermal models [13][14].

#### 10 Conclusion

The present work describes the first steps of an on-going analysis that is conducted to minimize the number of scenarios used to generate steady-state thermal network dedicated to electronic devices. A well-known approach of design-of-experiment is used to find a set of statistical heat transfer coefficient scenarios which have to guarantee the low discrepancy of our compact thermal models. Moreover, the study highlights the problematic of the spatial distribution of the JEDEC's or DELPHI's scenarios in the Dirichlet-Fourier boundary conditions fitting domain.

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Appendix A: Six-node resistance network (°C/W)

Node	Тор	Тор	Bottom	Bottom	sides
Noue	inner	outer	inner	outer	sides
Junction	160.0	-	5.4	144.9	-
Top inner	-	4300	-	-	-
Top outer	-	-	267.0	149.3	189.4
Bottom outer	-	-	-	-	180.2

 $S_{top-in} = (1.75 \text{x} 2.0) mm^2$ ,  $S_{bot-in} = (2.25 \text{x} 2.5) mm^2$ 

#### Appendix B: Seven-node resistance network (°C/W)

Node	Top inner	Top outer	Bottom inner	Bottom outer	sides
Junction	157.9	428.2	6.0	47.4	-
Top inner	-	3676	1731	33257	-
Top outer	-	-	-	-	112.4
Bottom inner	-	-	-	87732	-
Bottom mean	956.9	374.3	-	181.3	14392
Bottom outer	-	-	-	-	34.4

 $S_{top-in} = (2.54 \times 1.82) mm^2$ ,  $S_{bot-in} = (2.15)^2 mm^2$  $S_{bot-mean} = (2.77)^2 mm^2 - S_{bot-in}$ 

### Novel Partition-Based Approach to Dynamic Compact Thermal Modeling

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#### Abstract

A novel partition-based approach for the extraction of Dynamic Compact Thermal Models is presented. With respect to previous approaches, this methodology allows reducing the complexity of the constructed models, from quadratically to linearly dependent on the number of independent heat sources. The proposed methodology is validated through the application to two state-of-the-art electronic systems.

#### 1 Introduction

During the last decades, various approaches have been proposed in literature for constructing Dynamic Compact Thermal Models (DCTMs) of heat diffusion in electronic components and packages [1]-[3]. The Authors in particular have recently proposed a family of effective Model Order Reduction (MOR) methods for extracting DCTMs from the detailed thermal models of electronic components and packages [4]-[36]. In this way various families of DCTMs have been introduced, such as Boundary Condition respect Independent (BCI), parametric with to material/geometrical properties, including temperature dependence of material properties. In all these methods, proper basis are constructed for representing the thermal field, and the discretized equations of the detailed thermal model are projected onto the space spanned by these basis. These approaches have several advantages. They are efficient involving only the solutions of linear heat diffusion equations in the frequency domain, and not requiring transient simulations. The resulting DCTMs are accurate for estimating both the time evolution of junction temperatures of the electronic components and the whole space-time evolution of the thermal field. Moreover, usually the achieved DCTMs have small dimensions and can be numerically solved at negligible computational costs.

Nevertheless if the number of independent heat sources is large, the dimension of the basis can become large. This fact can lead to two main drawbacks: the construction of the basis by Singular Value Decomposition (SVD) and the projection of the discretized equations onto the space spanned by these basis can become infeasible due to RAM shortage; the complexity of the DCTMs, which increases at least quadratically with the dimension of the basis, reduces the advantages of the use of DCTMs.

In this paper, extending [35], a MOR approach is proposed for overcoming these drawbacks. In such approach, the spatial region filled by the considered electronic component or package, is partitioned into spatial sub-regions, each including a small number of independent heat sources. These sub-regions, separately modeled by DCTMs, are properly linked together so as to form a composite model of the whole spatial region. The resulting approach maintains the efficiency and accuracy of the original approach but leads to DCTMs defined by sparse matrices instead of dense matrices as in previous methods, the complexity of which linearly increases with the dimension of the projection basis. As a sole, the dimensions of these sparse matrices are somewhat larger than the dimensions of the dense matrices.

This method can be applied to any discretized forms of the heat diffusion equations, for instance by the Finite Element Method (FEM) or the Finite Volume Method (FVM). It does not require that the heat diffusion equations are discretized by any partition-based method, such as the Domain Decomposition or Discontinuous Galerkin's approaches [37]. Also it can be applied to all variants of DCTMs, in particular parametric with respect to material/geometry properties, hereinafter considered. Lastly the DCTMs defined by sparse matrices, can be exploited to extract DCTMs with smaller dense matrices. Thus they allow to perform the orthonormalization of the basis by SVD and the projection of the discretized equations onto the space spanned by the basis, avoiding the problems of RAM shortage.

The method has been validated by analyzing an IGBT module and an output stage of GaAs power amplifier.

#### 2 Discretized Parametric Heat Diffusion Problems

Let a transient heat diffusion problem be considered in which both the material thermal properties and the geometry details depend on p parameters  $p_1, \ldots, p_p$ , forming a vector **p**. Extending [24] from the stationary to the transient case, it can be shown that such transient heat diffusion problem can be reformulated as an equivalent transient heat diffusion problem in which only the thermal properties vary with **p**, the spatial domain  $\omega$  being fixed. For such a problem the temperature rise  $\vartheta(\mathbf{r}, t, \mathbf{p})$  with respect to the ambient temperature, at each position vector **r** in  $\omega$  and at each time instant t, is ruled by the transient heat diffusion equation Let a transient heat diffusion problem be considered in which both the material thermal properties and the geometry details depend on p parameters  $p_1, ..., p_p$ , forming a vector p. Extending [24] from the stationary to the transient case, it can be shown that such transient heat diffusion problem can be reformulated as an equivalent transient heat diffusion problem in which only the thermal properties vary with **p**, the spatial domain  $\omega$  being fixed. For such a problem the temperature rise  $\vartheta(\mathbf{r}, t, \mathbf{p})$  with respect to the ambient temperature, at each position vector  $\mathbf{r}$  in  $\boldsymbol{\omega}$  and at each time instant t, is ruled by the transient heat diffusion equation

$$c(\mathbf{r},\mathbf{p})\frac{\partial\vartheta}{\partial t}(\mathbf{r},t,\mathbf{p}) + \nabla \cdot (-\mathbf{k}(\mathbf{r},\mathbf{p})\nabla\vartheta(\mathbf{r},t,\mathbf{p})) = q(\mathbf{r},t,\mathbf{p}),$$

in which the heat capacity  $c(\mathbf{r}, \mathbf{p})$ , the thermal conductivity  $\mathbf{k}(\mathbf{r}, \mathbf{p})$ , and the power density  $q(\mathbf{r}, \mathbf{p})$  all depend on  $\mathbf{p}$ . Such equation is completed by conditions on the boundary  $\partial \omega$  of outward unit normal vector  $\mathbf{n}(\mathbf{r})$ , here assumed to be homogeneous of Robin's type

$$-\mathbf{n}(\mathbf{r}) \cdot \mathbf{k}(\mathbf{r}, \mathbf{p}) \nabla \vartheta(\mathbf{r}, t, \mathbf{p}) = h(\mathbf{r}, \mathbf{p}) \vartheta(\mathbf{r}, t, \mathbf{p}),$$

in which the heat exchange coefficient  $h(\mathbf{r}, \mathbf{p})$  depends on **p**, and by an initial condition, which can be assumed to be homogeneous

$$\vartheta(\mathbf{r},0,\mathbf{p})=0.$$

When a thermal model is defined, thermal ports are introduced. Powers  $P_i(t)$ , with i = 1, ..., n, injected at the ports determine the power density in the form

 $q(\mathbf{r}, t, \mathbf{p}) = \sum_{i=1}^{N} g_i(\mathbf{r}, \mathbf{p}) P_i(t),$  $g_i(\mathbf{r}, \mathbf{p})$  being shape functions, dependent on  $\mathbf{p}$ , such that

$$\int_{\omega} g_i(\mathbf{r}, \mathbf{p}) \, d\mathbf{r} = 1.$$

Following [7], the port temperature rises  $T_i(t)$ , with i =1, ..., n, are given by

$$T_i(t, \mathbf{p}) = \int_{\omega} g_i(\mathbf{r}, \mathbf{p}) \vartheta(\mathbf{r}, t, \mathbf{p}) \, d\mathbf{r}.$$

As it can always be assumed in practical cases [24], the material thermal properties vary with **p** as follows

$$c(\mathbf{r}, \mathbf{p}) = \sum_{s=1}^{C} C_s(\mathbf{p}) c_s(\mathbf{r}),$$
  

$$\mathbf{k}(\mathbf{r}, \mathbf{p}) = \sum_{s=1}^{K} K_s(\mathbf{p}) \mathbf{k}_s(\mathbf{r}),$$
  

$$h(\mathbf{r}, \mathbf{p}) = \sum_{s=1}^{H} H_s(\mathbf{p}) h_s(\mathbf{r}),$$
  

$$g_i(\mathbf{r}, \mathbf{p}) = \sum_{s=1}^{G} G_s(\mathbf{p}) g_{is}(\mathbf{r}),$$

in which  $C_s(\mathbf{p})$ ,  $K_s(\mathbf{p})$ ,  $H_s(\mathbf{p})$ ,  $G_s(\mathbf{p})$  are functions of  $\mathbf{p}$  and  $c_s(\mathbf{r})$ ,  $\mathbf{k}_s(\mathbf{r})$ ,  $h_s(\mathbf{r})$ ,  $g_{is}(\mathbf{r})$  are functions of the position vector r.

As it is well known, only in exceptional situations, in which geometries and material parameters are over-simplified, the transient heat diffusion equations can be solved in closed form. This difficulty can be overcome by discretizing the transient heat diffusion equation using any proper numerical method such as the Finite Element Method (FEM) or the Finite Volume Method (FVM). Using any of these discretization methods, the heat diffusion equation takes the form

$$\mathbf{M}(\mathbf{p})\frac{d\vartheta}{dt}(t,\mathbf{p}) + (\mathbf{K}(\mathbf{p}) + \mathbf{H}(\mathbf{p}))\vartheta(t,\mathbf{p}) = \mathbf{q}(t,\mathbf{p}), \quad (1)$$

In this equation  $\vartheta(t, \mathbf{p})$  is the columns vector with the Degrees of Freedom (DoF) of the temperature rise with respect to ambient temperature, M(p) and K(p) + H(p) are the mass and stiffness matrices respectively, both square of order M, depending on parameters  $\mathbf{p}$  as follows

$$\begin{split} \mathbf{M}(\mathbf{p}) &= \sum_{s=1}^{C} C_s(\mathbf{p}) \mathbf{M}_s, \\ \mathbf{K}(\mathbf{p}) &= \sum_{s=1}^{K} K_s(\mathbf{p}) \mathbf{K}_s, \\ \mathbf{H}(\mathbf{p}) &= \sum_{s=1}^{H} H_s(\mathbf{p}) \mathbf{H}_s, \end{split}$$

 $\mathbf{M}_s, \mathbf{K}_s, \mathbf{H}_s$ , being square matrices of order M. The column vector  $\mathbf{q}(t, \mathbf{p})$ , discretizing the power density, is given by

$$\mathbf{q}(t,\mathbf{p}) = \mathbf{G}(\mathbf{p})\mathbf{P}(t),\tag{2}$$

in which P(t) is the column vector with n port powers  $P_1(t), \dots, P_n(t)$  and  $\mathbf{G}(\mathbf{p})$  is the  $M \times n$  matrix

$$\mathbf{G}(\mathbf{p}) = \sum_{s=1}^{G} G_s(\mathbf{p}) \mathbf{G}_s$$

 $\mathbf{G}_s$ , being  $M \times n$  matrices. Lastly the column vector  $\mathbf{T}(t, \mathbf{p})$ with the *n* port temperature rises  $T_1(t), ..., T_n(t)$  is given by

$$\mathbf{T}(t,\mathbf{p}) = \mathbf{G}^T(\mathbf{p})\vartheta(t,\mathbf{p}).$$

#### 3 Parametric DCTMs defined by dense matrices

Extending the multi-point moment matching algorithm proposed in [24] from the stationary to the transient case, a parametric DCTM can be extracted from the discretized heat diffusion problem. To this aim, firstly m basis vectors, forming the columns of the  $M \times m$  matrix **W** are computed. The number m linearly increases with the number n of independent heat sources. Secondly a SVD of W is performed, so that

$$\mathbf{W} = \mathbf{U} \mathbf{\Sigma} \mathbf{V}^T$$

in which **U**, **V** are orthogonal matrices and  $\Sigma$  is the diagonal matrix with the singular values. This SVD is truncated to the first  $\hat{m}$  singular values in such a way that

$$\mathbf{W} pprox \widehat{\mathbf{U}} \widehat{\mathbf{\Sigma}} \widehat{\mathbf{V}}^T$$
 ,

with a chosen tolerance,  $\widehat{\mathbf{U}}$ ,  $\widehat{\mathbf{V}}$  being formed by the first  $\widehat{m}$ columns of respectively **U** and **V**, and  $\widehat{\Sigma}$  being formed by the first  $\hat{m}$  rows and columns of  $\Sigma$ .

The discretized temperature rises are approximated in form

$$\vartheta(t, \mathbf{p}) = \widehat{\mathbf{U}}\widehat{\vartheta}(t, \mathbf{p}),$$
 (3)

in which  $\hat{\vartheta}(t, \mathbf{p})$  is a column vector of  $\hat{m}$  DoFs. With this assumption, Eq. (1) is projected onto the space spanned by the columns of the  $\widehat{\mathbf{U}}$  matrix. In this way a parametric DCTM is achieved in the form

$$\widehat{\mathbf{M}}(\mathbf{p})\frac{\partial\widehat{\vartheta}}{\partial t}(t,\mathbf{p}) + \left(\widehat{\mathbf{K}}(\mathbf{p}) + \widehat{\mathbf{H}}(\mathbf{p})\right)\widehat{\vartheta}(t,\mathbf{p}) = \widehat{\mathbf{G}}(\mathbf{p})\mathbf{P}(t),$$
$$\widehat{\mathbf{T}}(t,\mathbf{p}) = \widehat{\mathbf{G}}^{T}(\mathbf{p})\widehat{\vartheta}(t,\mathbf{p}).$$

Matrices  $\widehat{\mathbf{M}}(\mathbf{p})$ ,  $\widehat{\mathbf{K}}(\mathbf{p})$ ,  $\widehat{\mathbf{H}}(\mathbf{p})$  are  $\widehat{m}$ -order matrices

$$\begin{split} \widehat{\mathbf{M}}(\mathbf{p}) &= \sum_{s=1}^{C} C_s(\mathbf{p}) \widehat{\mathbf{M}}_s, \\ \widehat{\mathbf{K}}(\mathbf{p}) &= \sum_{s=1}^{K} K_s(\mathbf{p}) \widehat{\mathbf{K}}_s, \\ \widehat{\mathbf{H}}(\mathbf{p}) &= \sum_{s=1}^{H} H_s(\mathbf{p}) \widehat{\mathbf{H}}_s, \end{split}$$

being

$$\mathbf{M}_{s} = \mathbf{U}^{T} \mathbf{M}_{s} \mathbf{U}, \qquad (4)$$

$$\hat{\mathbf{K}}_{s} = \hat{\mathbf{U}}^{T} \mathbf{K}_{s} \hat{\mathbf{U}}, \tag{5}$$

$$\widehat{\mathbf{H}}_{s} = \widehat{\mathbf{U}}^{T} \mathbf{H}_{s} \widehat{\mathbf{U}}.$$
 (6)

Matrix  $\widehat{\mathbf{G}}(\mathbf{p})$  is an  $\widehat{m} \times n$  matrix given by

$$\widehat{\mathbf{G}}(\mathbf{p}) = \sum_{s=1}^{G} G_s(\mathbf{p}) \widehat{\mathbf{G}}_s \tag{7}$$

in which

$$\widehat{\mathbf{G}}_s = \widehat{\mathbf{U}}^T \mathbf{G}_s.$$

The initial condition for the parametric DCTM is

 $\hat{\vartheta}(t,\mathbf{p})=0.$ 

The multi-point moment matching algorithm proposed in [24] for the extraction of parametric DCTMs is robust, efficient and accurate. In fact it applies to arbitrarily complex geometries. It does not require transient solutions of the heat diffusion problem but only selected solutions in the frequency domain. As a result, the method is very fast. The relative error  $\varepsilon$  tolerated in the approximation of the thermal field, provided by the parametric DCTM, can be arbitrarily chosen. The achieved DCTMs not only allow approximating port temperatures, but also, through (3), the whole space-time distribution of temperature throughout the electronic component or package.

Nevertheless if the number of independent heat sources is large, the number m of columns of matrix **W** can become large. This fact can lead to two main drawbacks: both the SVD of **W** and the projection of the discretized equations cannot be performed due to RAM shortage; since matrices  $\mathbf{M}_s$ ,  $\mathbf{K}_s$ ,  $\mathbf{H}_s$ ,  $\mathbf{G}_s$  are dense, the complexity of the DCTMs quadratically increases with the dimension  $\hat{m}$  of the parametric DCTMs, thus reducing the and advantages of their use.

#### 4 Parametric DCTMs defined by sparse matrices

A different approach overcoming the outlined drawbacks is here proposed. The spatial region with the considered electronic component or package is partitioned into a number q of spatial sub-regions, each enclosing a small number of independent heat sources. Let  $\mathbf{E}_i$ , with i =1, ..., q, be the  $M \times M_i$  rectangular matrix selecting the temperature rises of the discretized heat diffusion problem enclosed by the *i*-th spatial sub-region. Thus each row of  $\mathbf{E}_i$  has at most one value equal to 1 and each column of  $\mathbf{E}_i$  has exactly one value equal to 1, all the other values being zero.

By performing a SVD of matrix  $\mathbf{W}_i = \mathbf{E}_i^T \mathbf{W}$ , formed by the rows of  $\mathbf{W}$  with the temperature rises of the discretized heat diffusion problem enclosed by the *i*-th spatial sub-region, it results in

$$\mathbf{W}_i = \mathbf{U}_i \mathbf{\Sigma}_i \mathbf{V}_i^T.$$

in which  $\mathbf{U}_i$ ,  $\mathbf{V}_i$  are orthogonal matrices and  $\boldsymbol{\Sigma}$  is the diagonal matrix with the singular values. This SVD is truncated to the first  $\hat{r}_i$  singular values in such a way that

$$\mathbf{W}_i \approx \widehat{\mathbf{U}}_i \widehat{\mathbf{\Sigma}}_i \widehat{\mathbf{V}}_i^T$$
,

with the chosen tolerance,  $\hat{\mathbf{U}}_i$ ,  $\hat{\mathbf{V}}_i$  being formed by the first  $\hat{r}_i$  columns of respectively  $\mathbf{U}_i$  and  $\mathbf{V}_i$ , and  $\hat{\mathbf{\Sigma}}_i$  being formed by the first  $\hat{r}_i$  rows and columns of  $\mathbf{\Sigma}_i$ . This SVD computation can be performed without RAM shortage, because  $M_i$  is the smaller with respect to M the larger is the number n of independent heat sources. The number  $\hat{r}_i$  is much smaller than m and. In fact, as verified in numerical applications, it is just a small multiple of the number of columns of  $\mathbf{W}$  per independent heat source. This is consistent with the fact that the basis functions necessary to accurately represent the temperature field in the *i*-th sub-region and a small number of basis due to all the independent heat sources outside the *i*-th sub-region.

The temperature rise DoFs of the *i*-th spatial sub-region, forming vector  $\vartheta_i(t) = \mathbf{E}_i^T \vartheta(t)$ , can be approximated as

$$\vartheta_i(t, \mathbf{p}) = \widehat{\mathbf{U}}_i \widehat{\vartheta}_i(t, \mathbf{p}).$$
 (8)

Thus, repeating for all sub-regions, with i = 1, ..., q, it is

$$\vartheta(t,\mathbf{p}) = \widehat{\mathbf{U}}\widehat{\vartheta}(t,\mathbf{p})$$

in which

and being

$$\hat{\vartheta}(t,\mathbf{p}) = \begin{bmatrix} \hat{\vartheta}_1(t,\mathbf{p}) \\ \vdots \\ \hat{\vartheta}_q(t,\mathbf{p}) \end{bmatrix}$$

 $\widehat{\mathbf{U}} = \begin{bmatrix} \mathbf{E}_1 \widehat{\mathbf{U}}_1 & \dots & \mathbf{E}_q \widehat{\mathbf{U}}_q \end{bmatrix}, \tag{9}$ 

a sparse  $M \times \hat{r}$  matrix, with  $\hat{r} = \hat{r}_1 + \dots + \hat{r}_q$ , occupying a small multiple of the amount of RAM necessary for storing the columns of **W** per independent heat source. Using (8), with the sparse matrix  $\hat{\mathbf{U}}$  diven by (9), a parametric DCTM can be extracted, by the same equations (4), (5), (6), (7) used in previous Section 3. As a result, matrices  $\hat{\mathbf{M}}_s$ ,  $\hat{\mathbf{K}}_s$ ,  $\hat{\mathbf{H}}_s$ ,  $\hat{\mathbf{G}}_s$ , defining the parametric DCTM, are now sparse. Both their dimensions  $\hat{r}$  and the number of their non-zero elements linearly increase with the number n of independent heat sources.

Such parametric DCTM defined by sparse matrices can be exploited to derive a parametric DCTM defined by dense

matrices, without limitations due to RAM shortage. It is sufficient to construct the  $\hat{r} \times m$  matrix

$$\mathbf{R} = \begin{bmatrix} \widehat{\mathbf{\Sigma}}_1 \widehat{\mathbf{V}}_1^T \\ \vdots \\ \widehat{\mathbf{\Sigma}}_q \widehat{\mathbf{V}}_q^T \end{bmatrix}$$

and to perform, without limitations due to RAM shortage, the SVD

$$\mathbf{R} = \mathbf{P}\mathbf{S}\mathbf{Q}^T,$$

in which **P**, **Q** are orthogonal matrices and **S** is the diagonal matrix with the singular values. This SVD is truncated to the first  $\hat{m}$  singular values in such a way that

$$\mathbf{R} \approx \widehat{\mathbf{P}}\widehat{\mathbf{Q}}^T$$
,

with a chosen tolerance,  $\hat{\mathbf{P}}$ ,  $\hat{\mathbf{Q}}$  being formed by the first  $\hat{m}$  columns of respectively  $\mathbf{P}$  and  $\mathbf{Q}$ , and  $\hat{\mathbf{S}}$  being formed by the first  $\hat{m}$  rows and columns of  $\mathbf{S}$ . A parametric DCTM defined by dense matrices of order  $\hat{m}$  is obtained by substituting matrix  $\hat{\mathbf{U}}$  with  $\hat{\mathbf{U}}\hat{\mathbf{P}}$  in equations (4), (5), (6), (7). A parametric DCTM defined by dense matrices is thus achieved, substituting matrices  $\hat{\mathbf{M}}_s$ ,  $\hat{\mathbf{K}}_s$ ,  $\hat{\mathbf{H}}_s$ ,  $\hat{\mathbf{G}}_s$  of the parametric DCTM defined by sparse matrices, respectively with the dense matrices  $\hat{\mathbf{P}}^T \hat{\mathbf{M}}_s \hat{\mathbf{P}}$ ,  $\hat{\mathbf{P}}^T \hat{\mathbf{H}}_s \hat{\mathbf{P}}$ ,  $\hat{\mathbf{P}}^T \hat{\mathbf{G}}_s$ .

#### 5 IGBT Module

An IGBT module is discretized by the FVM using 580,032 unknowns. Parametric DCTMs are determined, taking as parameters the heat transfer coefficients on the top, bottom and sides of the structure. The ranges of such parameters are reported in Table 1.

Table 1: Ranges for the heat exchange coefficients  $p_1$ ,  $p_2$ ,  $p_3$  on the top, bottom and sides of the IGBT module.

	$\begin{array}{c} \text{Minimum} \\ (W/m^2K) \end{array}$	Maximum $(W/m^2K)$
<i>p</i> <sub>1</sub> (top)	5	104
$p_2$ (bottom)	1	10 <sup>3</sup>
$p_3$ (sides)	5	$2 \cdot 10^{2}$

In particular, two DCTMs are generated by imposing a 1% accuracy, using both the conventional (i.e., non-partitionbased) and partition-based approaches; in the latter the structure is partitioned as shown in Fig. 1. The DCTM derived by the conventional approach has smaller matrices of dimensions 419 but dense matrices with a larger number 892,889 of non-zero elements. The DCTMs derived by the partition-based approach has sparse matrices of larger dimensions 1,135 but smaller number 545,063 of non-zero elements. The extraction time of the two DCTMs are similar and equal to about 2 hours. Fig. 2 shows the sparsity patterns of the parametric DCTM defined by sparse matrices. Also a parametric DCTM defined by dense matrices of dimension 418 is extracted from the parametric DCTM with sparse matrices in less than 10s.



Figure 1: Partitioning of the power module structure.



Figure 2: Sparsity pattern of the matrices defining the parametric DCTM.

The accuracy of the resulting three DCTMs is measured by picking a random value for the heat transfer coefficients within the ranges given in Table 1 D i.e., 1000, 10, and 1 W/m  $^{2}$ K for the bottom, top, and sides, respectively D and performing a transient simulation with a typical power dissipation pattern for the 18 independent heat sources. For the three extracted DCTMs such transient simulations required less than 1 s, which has to be compared with about 2 h needed for the transient solution of the 3-D discretized problem. The output waveforms with the junction temperature rises of all the 18 independent heat sources are depicted in Fig. 3. A zoom of the figure showing the differences in the thermal responses of the different models is given in Fig. 4.





*Figure 3: Junction temperature rises due to the application of a power step superposed with a sine power wave.* 



Figure 4: Zoom of the junction temperature rises due to the application of a power step superposed with a sine power wave.

#### 6 GaAs Power Amplifier

The output stage of a GaAs Power Amplifier is discretized by FVM using 1,087,348 unknowns. A DCTM is determined by resorting only to the partition-based approach, since the conventional method cannot be used with only 16GB RAM. The structure is partitioned as shown in Fig. 5. A 1% accuracy is ensured by the resulting DCTM, which benefits from sparse matrices of dimensions of 2,709 and 343,029 non-zero elements, as reported in Fig. ??, and was extracted in slightly less than 2 h. A DCTM with dense matrices of dimension 566 and 695,048 non-zero elements is also extracted from the DCTM defined by sparse matrices in less than 25s.



Figure 5: Partitioning of the power module structure.



Figure 6: Sparsity pattern of the matrices defining the parametric DCTM.



Figure 7: Junction temperature rises of the independent heat sources due to the application of a nonuniform power distribution.

The two DCTMs were tested by performing transient simulations with a nonuniform power distribution: power steps with different amplitudes were applied to the independent heat sources at the same time instant t=0 s. These simulations required less than 1 s, which has to be compared with about 3 h needed for the transient solution of the 3-D discretized problem.

The output waveforms with the junction temperature rises of all the 96 independent heat sources are depicted in Fig. 7. A zoom of the figure showing the differences in the thermal responses of the different models is given in Fig. 8.



Figure 8: Zoom of the junction temperature rises of the independent heat sources due to the application of a nonuniform power distribution.

#### 7 Conclusions

In this paper, a novel partition-based MOR approach has been proposed for the construction of DCTMs. This approach has been applied to two state-of-the-art case studies. The proposed methodology allow extending the main benefits of a previous MOR approach developed the Authors in terms of accuracy, efficiency and robustness to the case of massive numbers of independent heat sources.

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**SESSION 5** 

# **SESSION 5** 3D IC / Packaging

## Analysis of the Impact of Power Distribution on the Efficiency of Microchannel Cooling in 3D ICs

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#### Abstract

Liquid microchannel cooling of 3D ICs is a very attractive idea which could help solving the problem of ever-increasing power dissipation due to its good cooling efficiency and potential scalability. However, this cooling method has some very different properties than the well-understood forced air convection. In particular, its cooling efficiency with respect to power variations in the chip is still not completely analysed. Therefore, in this paper a thorough study of microchannel cooling efficiency as a function of intra- and interlayer power consumption variation is presented. We use a finite element method analysis to run a coupled thermo-fluidic simulation of a dedicated 3D chip model. We show that the placement of chip units with respect to microchannels can significantly influence the peak chip temperature. In particular, for a 3D chip including Intel's i7-6950X 10-core processor, a temperature difference of nearly 9°C was observed.

#### 1 Introduction

3D integration of electronic circuits [1] is rapidly gaining interest among researchers and manufacturers due to its many advantages, most importantly due to the possibility of integrating various technologies on a single chip and increasing the number of transistors in the same chip footprint. One of the most important problems of these 3D architectures is high dissipated power density. Current cooling systems with heat sink and forced air convection will be insufficient for 3D ICs with many layers; it has been shown in [2] that even for a two-tier chip (processor and DRAM), maintaining the temperature below the acceptable level using standard cooling may be problematic. Therefore, the liquid cooling using integrated microchannels [3] was proposed. It is based on the idea of one or more dedicated cooling layers inserted into the 3D stack. These layers contain microchannels through which the coolant flows. Among its many advantages, there is one which makes this solution especially promising: the fact that the cooling system is theoretically scalable. In other words, increased power dissipation due to adding more tiers to the 3D stack can be compensated by simply adding more cooling layers to keep the peak temperature at the same level. The heat removal capability of microchannels depends on many parameters, e.g., their shape and size, coolant flow rate, etc. Many authors have analysed this impact, performing either measurements of a test chip or software simulation [4]. However, there is one more chip parameter which seems to be still under-analysed when it comes to microchannels efficiency, namely the power distribution in the chip. Intuitively, one may suspect that when assuming a uniform inter- and intra-layer power density the efficiency of microchannels will be somewhat overrated. Thus, the study which takes into consideration spatial power variations is required. Note that in 2D chips, there exists only planar power variation, in other words, the power density only

changes across one chip layer in horizontal directions. In a 3D stack the situation is much more complex; the power also varies across layers (in the vertical direction). The difference in power dissipation in chip layers can be sometimes very significant, e.g., the power consumption of a processor is much higher than that of DRAM or MEMS layer. Moreover, the thermal behaviour of the chip will depend how hotspots in various layers are located with respect to each other. Therefore, the goal of this paper is to provide a thorough study on how the spatial power variation in 3D chip affects the efficiency of microchannel cooling. We consider both horizontal and vertical non-uniformity and analyse how the hotspots' size, power density and location with respect to other hotspots influence the peak temperature in the chip.

#### 2 Methodology

We build a 3D chip model using COMSOL Multiphysics [5], which allows running a coupled thermo-fluidic FEM simulation. Our chip model has an area of  $15x15 \text{ mm}^2$  and consists of six tiers: three power dissipating tiers and three cooling ones (Fig. 1).



*Figure 1: Vertical view of the simulated 3D chip model (not to scale)* 

Additionally, each tier is further divided into a silicon layer, a dielectric layer and an active layer. The chip tiers are connected using underfill with metal microbumps. In each cooling layer, there are 14 evenly distributed rectangularshaped microchannels, each with 350  $\mu$ m width and 100  $\mu$ m height. In each tier, half of the power is dissipated in active layer (which represents the power dissipated in transistors' channels) and the other half in metal layer (which represents the power dissipated in interconnects). The layer thicknesses are typical for 3D packages and were set based on data taken from recent publications on 3D ICs. Note that some chip layers are heterogeneous because they are composed of two or more different materials (underfill layer containing copper microbumps, silicon layer containing copper TSVs, etc.), they should be modelled with effective thermal conductivities. Many authors [6] use here an approach based on the area ratio of materials in the layer: the effective thermal conductivity for the entire layer is then calculated using a simple formula  $k_{eff} = k_1 d + k_2 (1-d)$ , where  $k_1$  and  $k_2$  are the thermal conductivities of the two materials and d is the fill ratio of the first material in the layer. We follow this approach in this paper with one substantial change: instead of using isotropic thermal conductivity for the whole layer, it was decided to differentiate between vertical and horizontal conductivity. Indeed, if we consider for example the underfill layer with uniformly distributed microbumps, it is obvious that the vertical thermal conductivity will increase due to the presence of metal microbumps. However, the horizontal thermal conductivity will not be affected as much. Therefore, in our model we calculated separately the effective conductivities in x, y and z directions for all heterogeneous layers. For instance, horizontal and vertical thermal conductivity of a silicon layer is appropriately calculated assuming it contains a given number of copper TSVs. Similar approach is used for dielectric layer, which contains metal interconnections and for underfill layer with microbumps. Water is used as a coolant which flows at a flow rate of 144 mL/min through all microchannels. The temperature of water at the inlets is fixed at 30°C. Single-phase laminar flow is assumed (this assumption is correct because the calculated Reynolds number is equal to 385, well below the value where the flow becomes turbulent. We also model convection though BGA balls and PCB (we assumed a convection resistance of 50 K/W), although it was discovered that its impact on results is practically negligible. In all simulations all model dimensions, material parameters and input values stay the same. We vary only the power dissipation between all layers and within a layer, while maintaining the total power dissipation constant (300 W). Then, we observe the temperature distribution in the chip as a function of this power variation. It should be also noted that the mesh generated for the model is non-uniform: the mesh is finer in channel area and thin layers, whereas it is coarser in thick layers. The mesh is also anisotropic: mesh elements are elongated according to the shape of the block, for example for channels, the mesh density is higher in y and z directions and lower in x direction (along the channel). For more

detailed information regarding the modelling methodology, please consult authors' previous paper [7].

#### 3 Microchannel cooling vs. forced air cooling

In this section, a quick discussion of differences between microchannel cooling and forced air cooling is presented. We will not concentrate on the heat transfer mechanism, but rather on the impact of the used cooling method on the resulting temperature distribution. In the case of forced air cooling, the chip is cooled from the top layer and it can be assumed that the cooling is almost uniform on the entire chip surface. Therefore, a uniform power distribution in the chip area will always result in an almost uniform temperature distribution. Moreover, if any local power density hotspot appears, it will always result in higher peak temperature than the one obtained with uniform power distribution. As a consequence, when using forced air cooling, researchers and manufacturers have always intended to make the power density as uniform as possible (spatially or temporally) to achieve the lowest peak temperature in the chip. This approach needs to be completely revised when microchannel cooling is used. To better understand the reasons where these differences come from, let us first present the simulation results for microchannel cooling for the uniform power distribution (Fig. 2).



*Figure 2: Temperature distribution in the chip (for uniform power distribution) - outlet side view* 



*Figure 3: Temperature across chip (uniform power distribution)* 

Additionally, we plotted the temperature across the chip to better visualize the temperature profile (Fig. 3). It can be observed that the temperature profile is linear in the wide range along the chip cross-section. The non-linearity on the left side of the graph can be explained by the effect of the edge of the chip: no heat sources on the left side of the chip means that the temperature slope is a little steeper. The linearity of the temperature profile should not be a surprise: the water is heated uniformly along the channels, so its temperature rises practically linearly from inlets to outlets, which results in a similar temperature profile in the silicon layer. To describe this thermal property of microchannels, we introduce the term *diminishing cooling efficiency* (DCE) effect, due to which the side of the chip where the coolant enters is always better cooled than the side of the chip near the outlets. Therefore, one may reasonably argue that the uniform power distribution is not the optimal power distribution from the thermal point of view for microchannel cooling. Looking at the above results one may also suppose that a more thermally optimal power distribution should include higher power dissipation near the inlets and lower power dissipation at the outlets. Consequently, the thermal optimization of chip floorplan becomes a more complex task, because balancing the power density has to take into consideration the DCE effect. In the next chapters, the authors try to quantitatively analyse the impact of various power distributions on temperature and point out new surprising characteristics of microchannel cooling.

#### 4 Analysis of intra-layer power variation

The first analysis intents to show the impact of intra-layer power variation on temperature in liquid-cooled IC. Therefore, for the entirety of this chapter, the power is varied only within a layer, while the total power dissipated in every one of the three layers is the same and equal to 100 W. In the first simulations, each power-dissipating layer was divided into 9 tiles (3x3 grid). For convenience, we named these tiles using capital letters from A to I (see Fig. 4). In the first approach it was decided to vary the power only along the x axis (along the direction of the channels). In each layer, a dedicated high power density region was chosen which consists of A, B, and C tiles (the ones near the inlets). A parameter  $\beta$  was introduced, which is the fraction of the total power dissipated in this dedicated region. Simulations have been run for gradually increasing value of  $\beta$ , in other words for gradually increasing power consumption in the ABC region.



Figure 4: Illustration of a chip divided into nine tiles (top view)

Note that  $\beta=0.333$  corresponds to the uniform power distribution. Fig. 5 shows the peak temperature obtained in the chip as a function of the  $\beta$  parameter. The results confirm our initial reasoning: the lowest peak temperature was observed not for  $\beta=0.333$ . However, it may be surprising that the lowest peak temperature was observed for  $\beta$ =0.6, i.e., for the case where as much as 60% of total layer power was dissipated in the ABC region (so the power density was 3 times higher in the ABC region than the rest of the layer). It is also important to note that the maximum temperature obtained for this distribution was even 7°C lower than the one obtained for uniform power distribution. To better explain how the temperature in the chip changes for various values of  $\beta$ , we also plotted in Fig. 6 the temperature profiles across the chip for  $\beta=0.333$ ,  $\beta=0.6$  and  $\beta=1$ . Let us now analyse the presented curves. As we increase the value of  $\beta$ , more power is dissipated in the ABC region of the chip and the temperature there also increases. Meanwhile, the temperature at the outlet edge of the chip decreases but is still higher than the local hotspot temperature.



Figure 5: Peak temperature in the chip as a function of the percentage of power dissipated in ABC tiles



*Figure 6: Temperature across the middle of the chip for three different percentages of power dissipated in ABC tiles* 

For the best case of  $\beta$ =0.6 the resulting local hotspot temperature of the ABC region matches the temperature at the outlet edge. Further increase of power dissipated in the ABC region causes local hotspot temperature to increase and, therefore, to become the highest temperature in the chip. To sum up, for  $0.6 < \beta < 0.333$  the highest chip temperature is located on the outlet edge, while for  $\beta$ >0.6 the peak temperature is located in the local hotspot. The value of  $\beta$ =0.6 is the "sweet spot" where the temperature distribution is most uniform and, as a result, the maximum obtained temperature is the lowest. Second experiment was similar to the first one, however in this case, the power dissipated in two out of three layers was uniform, and the non-uniform power distribution was present only in one layer. Additionally, we considered four different regions, composed of tiles ABC, DEF, GHI and BEH (see Fig. 4). The results showing peak chip temperatures as a function of  $\beta$  parameter are shown in Fig. 7. The results are very interesting: it turns out that for ABC region, the lowest maximum temperature is obtained when all power ( $\beta$ =1) is dissipated in this region! This proves that having uniform power distribution in two layers allows for having very high power density areas in the third layer as long as these areas are located near the inlet side of the chip. This may be especially helpful for high-performance processors (very non-uniform power density) stacked with layers with fairly uniform power density like cache memory or DRAM. Other conclusion is that dissipating most power near the outlets obviously worsens the chip temperature profile. However, what is interesting, for  $\beta$ =0.5, the peak temperature obtained for BEH region was actually lower than the same temperature for ABC region. This shows that even though a general approach should be to put regions with highest power near the inlets, for some power distributions it may be even better to consider other options. From the conducted experiments it has been deduced that the lowest peak temperatures are obtained for the power dissipation profile which gradually decreases from inlet to outlet side of the chip.



Figure 7: Peak temperature in the chip as a function of the percentage of power dissipated in a three-tile region



Figure 8: Peak temperature in the chip as a function of the percentage of power dissipated in B, E or H tile

Third analysis takes into account smaller regions. It follows the same principle as the second analysis (in two out of three layers the power is dissipated uniformly), however this time, the power density hotspot region is only composed of one tile. The results showing peak chip temperatures are shown in Fig. 8. We considered three regions, first corresponding to B tile (near the inlets), second corresponding to E tile (in the centre) and third corresponding to H tile (near the outlets). Note that now the uniform distribution corresponds to the case of  $\beta$ =0.111. As one may expected, the chip thermal behaviour follows the same pattern as the results first presented in Fig. 5. As we increase  $\beta$ , the peak temperature first decreases, reaches the minimum and then starts to increase. Clearly, the B tile located near the inlets allows for dissipating more power consumption than the H tile located at the outlets. The lowest temperature was obtained when 50% of total layer power is dissipated in the B tile.

#### 5 Analysis of inter-layer power variation

In the previous section, the case when the power dissipated in each tier is the same was analysed. This is the clearly the case when the efficiency of microchannel cooling should be the highest because cooling layers are distributed uniformly. However, in practical applications particular tiers may have very different power consumption. For instance, in a threetier chip consisting of a high-performance processor, DRAM and a layer of MEMS sensors, there will be a significant vertical non-uniformity of dissipated power. Therefore, one may expect that the microchannel cooling efficiency will decrease with increasing inter-layer non-uniformity of power consumption. To quantify this effect, we have analysed two cases. This time, the dissipated power was varied only between the three tiers and not within a tier. In the first case, we assumed that the middle tier always dissipates 100 W, the top tier dissipates  $\beta$ \*100 W, whereas the bottom tier dissipates  $(2-\beta)*100$  W of power. Thus, the total power consumed is still 300 W, and the value of  $\beta$ 

determines the non-uniformity of the vertical power distribution (note that in the case of  $\beta=1$  the power distribution is uniform). The simulations have been performed for various values of  $\beta$  parameter. Fig. 9 depicts the peak temperature in bottom (hotter) and top (cooler) tiers as a function of the amount of power dissipated in the bottom tier. Predictably, the lowest peak temperature corresponds to the uniform vertical power distribution. It then increases linearly while the power in bottom layer is increased. With respect to the best case, the maximum temperature increases by 5°C when as much as 190 W of power is dissipated in the bottom layer. On the other hand, the peak temperature of the top layer decreases, but at a slower rate. In the second case, we analysed an even more extreme case in which one layer dissipates much more power than the other two: top tiers dissipate  $\beta$ \*100W each and the bottom tier dissipates  $(3-2\beta)$ \*100W. The simulation results (Fig. 10) show that this time, the peak temperature in the worst case (280 W out of total 300 W dissipated in bottom tier) is only 9°C higher than for the best case (uniform power distribution).



Figure 9: Maximum temperature in top and bottom layer for various distributions of power dissipation in chip tiers



Figure 10: Maximum temperature in top and bottom layer for various distributions of power dissipation in chip tiers (second case)

The results obtained in two analysed cases indicate that microchannel cooling shows a very good resilience to interlayer power variation. Of course, the exact results will vary depending on the parameters of the package such as microchannel dimensions, layer thicknesses and material properties, but it may be safely concluded that the efficiency of microchannel cooling should not be significantly degraded by non-uniform vertical power distribution between particular chip tiers.

#### 6 Analysis of a practical case

In this section, we show how the positioning of microchannels can have an impact on the resulting temperature distribution in 3D ICs. We consider a 3D integrated chip composed of three cooling layers and three power-dissipating tiers: a modern 10-core processor Intel Broadwell i7-6950X, a graphics unit and 16 GB of DRAM memory (Fig. 11). It is assumed that the DRAM dissipates 5 W of power, the graphics unit dissipates 55 W and in both these layers the dissipation of power is uniform. The third layer (the processor), is modelled assuming that the power density in the cores is different than the one in the rest of the processor. The power density in the cores was assumed to be  $1.5 \text{ W/mm}^2$  and the power dissipated in this area was calculated accordingly. The power consumption in the remaining area was calculated taking into consideration the total thermal design power (TDP) of the chip given by Intel as 140 W [8]. The simulations were performed for two microchannel orientations (Fig. 11 c and d). Fig. 12 presents the temperature distribution in the processor layer. In the first case, obviously there are two local hotspots, corresponding to the processor cores.



Figure 11: Analysed 3D chip: a) 3D stack, b) i7-6950X processor floorplan (source: Intel), c) orientation of inlets with respect to the processor (first case), d) orientation of inlets with respect to the processor (second case)

However, it can be visible that the core region located closer to the edge produces higher temperatures, because there are fewer microchannels which can remove the heat generated there. The peak temperature was 81.8°C. For the second case, also two local hotspots corresponding to cores can be seen. Although core regions dissipate the same amount of power, it is clearly visible that the region near the inlets is cooled much better. The maximum temperature was equal to 72.9°C in the hotspot located in the middle of the right-hand core region. It should be emphasized that this hotspot temperature is 8.9°C lower than the one obtained in the first case, which proves that orientation of microchannels with respect to chip units have a very strong impact on chip peak It may even be said that, in case of temperature. microchannel cooling, designers of the chip floorplan should take into consideration chip thermal behaviour and optimize the floorplan according to the efficiency of microchannels. The results presented in this section have also shown that microchannel cooling is able to maintain a reasonable peak temperature in a 3D chip with 200 W of total power dissipation and with 1.5 W/mm<sup>2</sup> power density areas. The required fluid flow rate which ensures this cooling efficiency is not high: the pressure drops across microchannels reported in our simulations were in the range of only 23-25 kPa.



Figure 12: Temperature distribution in the chip for the first (top) and second case (bottom). Black rectangles are processor cores. Note that bottom layers of the chip were hidden to make the hottest chip layer (the processor) visible.

#### 7 Conclusions

In this paper, the impact of intra-layer and inter-layer power variation has been studied. It has been shown that liquid microchannel cooling differs from standard forced air convection cooling due to the DCE effect: the cooling efficiency of microchannels is significantly higher at the side of the chip where inlets are located. For example, the presented results have shown that the best cooling efficiency was obtained not for the uniform power distribution, but when as much as 60% of total power is dissipated in the one-third of chip area near the inlets. It has been also shown that this effect is even stronger when the inter-layer power non-uniformity exists only in one layer and the power dissipation in other layers is uniform. It has been also shown that for typical package parameters, microchannel cooling efficiency is very resistant to inter-layer non-uniformity in power dissipation. For a total power dissipation of 300 W, there has been only a 9°C increase in peak temperature when moving from uniform power distribution to the extreme case when 280 W of power was dissipated in one layer. A practical case of a three-tier chip based on Intel's Broadwell i7-6950X processor has been also analysed. The presented results indicate that the proper orientation of microchannel with respect to the chip floorplan reduced the hotspot temperature in the chip by 8.9°C.

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## Closing the Power Delivery/Heat Removal Cycle for Heterogeneous Multi-Scale Systems

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#### Abstract

The semiconductor industry is poised to continue the historic Moore's law trend of doubling the level of integration every 1.5-2 years, even as the virtuous cycle benefits of Dennard scaling are quickly vanishing. Once devices no longer scale laterally, the only way to continue to increase areal density is by going vertical using 3D-IC. However, 3D-IC raises several fundamental difficulties in addition to the clear fabrication challenges: as the number of physical layers in a 3D-IC stack increases, from the present 2.5D multi-layer solutions (with an interposer, or only a couple of layers), to true 3D many-layer stacks, the energy cycle problem of delivering power to and removing heat from the 3D stack become daunting. The main reason for this power wall is the mismatch between the volumetric (cubic) power consumption and heat dissipation in 3D-IC, and the areal (quadratic) power delivery and heat removal through a 2D surface (top and/or bottom of the stack). In this paper we propose MultiSpot, a framework to provide fundamental solutions to the 3D-IC power wall that are also practical.

#### 1 Moore's law through 3D-IC

The semiconductor industry is poised to continue the historic Moore's law trend of doubling the level of integration every 1.5-2 years, even as the virtuous cycle benefits of Dennard's scaling (devices get simultaneously smaller, faster and lower power) are quickly vanishing or have already stopped. Once devices no longer scale laterally (Dennard scaling stops), one way to continue to increase density is by going vertical as three-dimensional integrated circuits (3D-IC) which can be monolithic (e.g. 3D-NAND Flash), or through-Silicon via (TSV)-based; but 3D-IC raises several fundamental difficulties in addition to the clear fabrication challenges. As the number of physical layers in a 3D-IC stack increases, from the present 2.5D multi-layer solutions, with an interposer, or only a couple of layers, to true 3D many-layer stacks, the energy cycle problem of delivering power to, and removing heat from, the 3D stack become daunting. The main reason for this power wall is the mismatch between the volumetric (cubic) power consumption and heat dissipation in 3D-IC, and the areal (quadratic) power delivery and heat removal through a 2D surface (top and bottom of the stack).

#### 1.1 3D-IC as an enabler for Moore's Law

Moore's original observation that later became a "law" had to do only with the exponential increase in the number of transistors that can be economically integrated in a single chip. The later various flavours of "Moore's laws" (e.g. exponential increases in performance, decreases in power, etc.) have been just a by-product of the way the semiconductor industry was able to stay on the Moore's law path by using transistor scaling rules first proposed by Dennard. Today Dennard scaling has reached several "red brick walls" – lateral overall transistor dimensions and power supply voltages scale at slower rates, if at all, thus clock rates and power densities are essentially staying constant – yet Moore's law in its originalist form (i.e. exponential increase in level of integration) is poised to continue, with 3D-IC as an essential mechanism for staying on the historical integration trend. There are several major advantages of 3D-IC: 1) reduction of average wirelength from a square root of lateral dimensions to a cubic root, 2) enabling heterogeneous architectures, heterogeneous technologies, such as CMOS and DRAM, 3) significant improvement of bandwidth and latency due to the availability of TSVs, 4) allowing low voltage and high power efficiency.

#### 1.2 Power delivery and heat removal walls for 3D-IC

3D-IC is a general term that describes technologies that either use monolithic integration methods (e.g. 3D NAND Flash) or use several Silicon layers on top of each other (stacked 3D-IC) such that more transistors can be integrated in the same lateral footprint. For the purpose of this work we are interested in future trends thus we will focus on 3D-IC schemes that are scalable to many layers; such 3D-IC solutions will use a large number of thinned Silicon layers that are connected to each other using through-Silicon vias (TSVs). Since these are true three-dimensional structures, power is usually delivered using controlled-collapse chip connections (C4s) on one side of the 3D stack (flip-chip), while heat is removed by a heat sink attached to the other side of the stack. To stay on the historical Moore's law trend will require the number of layers in the 3D-IC stack to increase, which means the power consumption and dissipation will increase in a cubic fashion (with the volume of the stack), while the power delivery and heat removal will be limited by the quadratic area of the top and bottom layers. Even without 3D-IC the number of power and ground pins and C4s on current chips is in the hundreds and can take more than half of the total number of pins, thus it is clear that simply trying to keep up by increasing the number of pins and C4s is unsustainable for 3D-IC. Similarly, the thermal envelope limits of cooling are already stretched by current chips, alternative cooling solutions will be needed for 3D-IC.

#### 1.3 Breaking the 3D-IC heat removal wall

3D-IC microchannel cooling offers a straightforward and efficient method to address the mismatch between volume and area by essentially offering some very low thermal impedance paths for the heat to travel from the inside of the 3D-IC stack to the outside. The heat transfer mechanism with microchannels is heat convection that is much more effective at removing heat than the heat conduction that would be the dominant mechanism in the stack without the microchannels. Regular liquid cooling on the top of the package also uses heat convection, but since it can only remove heat from the outside surface it does not resolve the mismatch – microchannels on the other hand, by traversing the actual volume of the 3D-IC stack can effectively "short-circuit" the high thermal impedance heat conduction paths, thus providing a fundamental solution.

#### 1.4 Paper Objectives

Would concepts similar to the microchannel cooling work also for power delivery for 3D-IC? Can we use some form of low impedance paths to provide current to the interior of the 3D-IC volume? Interestingly, many decades ago the Cray-2 supercomputer did exactly that by using gold rods to provide power to a 3D stack made at the time of tightly integrated printed circuit boards.

The main objective of this paper and the recently started MultiSpot project is to provide fundamental solutions to the 3D-IC power wall that are also practical. The main hypotheses are that: 1) comprehensive solutions need to address both heat removal and power delivery synergistically, by closing the energy cycle, otherwise solutions become suboptimal, 2) since the brain is one of the main energy consumers in the body that also needs to be efficiently cooled, and since it potentially has the same volumetric vs. areal mismatch as future 3D-ICs, biology can provide useful inspiration for the problem at hand, and 3) design space exploration of the power delivery/heat removal problem requires tools that can model heterogeneous Systems-on-Chip (SoC) and Systems-on-Package (SoP).

#### **1.5 Enhanced Micro-channels: Co-optimized** simultaneous cooling and power delivery

The heat dissipation issue of 3D-IC arises from the increase of volumetric power density but decrease of the heatdissipation surface area of the processors. The traditional aircooling techniques heavily depend on the deviceenvironment surface area and are obviously not adequate for 3D-IC. The emerging volumetric cooling technologies (e.g., micro-channel cooling) provide enough heat dissipation power to enable multi-layer 3D stacking. Pioneering studies have been done to investigate the effectiveness of liquid cooling for mitigating the thermal issues of 3D-IC. The results show that volumetric liquid cooling techniques, especially micro-channel cooling, extend the benefits of scaling for stacked processor and memory. Power efficiency can be further improved by optimizing the topology of microchannels. The power delivery issue is caused by the increasing power density, the increasing transistor-operation frequency and the decreasing operation voltage from technology scaling. High operation frequencies lead to even worse power delivery noise by increasing inductive voltage/power lost on the power delivery network (PDN). Decoupling capacitors (decap) are widely used as the major design-time technique to mitigate transient power delivery failures. A large amount of on-chip decap is desired to suppress the voltage supply noise under a given voltage variation level constraint. Larger decaps are needed to deal with the low-frequency noise. However, the intensive use of decap requires extra on-chip area, increases the cost, and becomes impractical if large capacitance values are needed. Runtime control voltage and rollback also can be effective in reducing software errors caused by unstable power supply but with significant performance overheads. Power pad allocation optimization and switchable power-I/O pins are emerging techniques to reduce power pad usage but power supply-I/O bandwidth contention still exists. The situation becomes worse when shifting to 3D-IC for two reasons: 1) the requirements of both I/O bandwidth and power supply increase while the 2D C4 interface for power and I/O connections remains unchanged 2) the cross-layer power supply with through silicon via (TSV) increases wirelength of power supply resulting in a higher impedance of PDN.

In addition to the remaining issues of power delivery and power-I/O contention, the traditional vertical power supply scheme and the horizontal liquid cooling scheme show conflicts. The vertical power supply prefers a thin dielectric layer for cross-layer signal isolation; while inter-layer liquid cooling needs more space for liquid flow, which significantly increases the wirelength of PDN and makes the voltage supply noise severe.

### **1.6** MultiSpot – a combined thermal and power delivery research infrastructure

The research community has typically tackled thermal and power delivery separately, with different types of tools and different types of solutions. The MultiSpot infrastructure recognizes that the volumetric vs. areal mismatch in 3D-IC applies to both sides of the energy cycle (power in/heat out), which represents a double challenge, but also offers the potential for coordinated solutions. We have previously developed several high-impact architecture modeling tools for power and thermals, such as HotSpot [1], HotLeakage VoltSpot [2], and ArchScope that have enabled extensive research at academic institutions and industry in the areas of temperature-aware computing and pre-RTL power delivery optimization. While the described microchannel enhancement and circuit aspects are essential, breaking the 3D-IC power wall will be suboptimal if the other abstraction levels are not fully engaged. The technological details of the liquid metal fluid or of the embedded capacitor technology are essential for overall system optimization, while the architecture details of how compute cores are distributed in the stack and how the compute threads are scheduled determine the imbalances in current consumption.

### 2 3D-IC, microchannel cooling, electronic blood, thermal modeling, power delivery

Our work bridges thermal and power delivery with 3D-IC integration, microchannel cooling and voltage stacking by proposing several unique and combined solutions that enhance the microchannel cooling structure with the capability of power delivery and/or energy storage for heterogeneous systems.

One project that is the most similar to some aspects of this work is the "electronic blood" project pursued by IBM Zurich [3]. The motivation is also the volumetric vs. areal mismatch, and the biology inspiration is taken to the extreme: the electronic blood proposed by IBM both cools the system, but also provides power/energy by using a polarized fluid that can be "charged" off-chip and the charge used on-chip by coupling with the micro-channel that carries the "blood." While this is quite revolutionary, it also happens to be quite impractical as the amount of energy that can be transferred this way is very limited, and the "charging" and "discharging" of the polarized fluid is inefficient. The solution proposed in our work is still to align the power delivery solution to the microchannel cooling, but in a practical way: the energy is delivered still in the form of a current like in the traditional case, except that the current is carried either by the microchannel walls, or by a conductive fluid (liquid metal). The idea of using the microchannel walls as supercapacitors is completely novel as far as we know.

In terms of pre-RTL thermal modeling, our own tool HotSpot is one of the more popular in the research community, and it has also been enhanced with 3D-IC extensions. 3D-ICE from EPFL [4] was specifically developed to model microchannel cooling, but it has many limitations when trying to use it in a architecture-level design space exploration scenario (e.g. is not directly compatible with the set of architecture tools used in the community, such as GEM5, McPAT, etc.). Another limitation of current thermal modeling tools is that they mostly consider homogeneous systems. For power delivery pre-RTL modeling there have been several solutions previously proposed, with our own VoltSpot producing the most detailed spatial and temporal on-chip traces. MultiSpot significantly pushes the envelope in thermal and power delivery modeling by allowing cross-layer coupled analyses while enabling the design space exploration of heterogeneous SoC and SoP systems.

#### **3** Fundamental yet practical solutions for **3D-IC**

In this work we are targeting to improve the PDN of 3D-ICs, minimize the power-I/O contention and exploit the design trade-offs between liquid cooling and power delivery. We propose fundamental changes to the power delivery system for 3D-IC and bring out major methodologies of power delivery - liquid cooling co-design for 3D processors and memory (some of the methods are mutually exclusive as they are more appropriate in specific scenarios): 1) reuse microchannels to build voltage noise reduction components – supercapacitors on walls, 2) 3D hierarchical power delivery for 3D-IC and spatially overlap power delivery and liquid cooling – conductive microchannel walls, and 3) physically merge liquid cooling system and power delivery system – liquid metal for cooling and power delivery. Our goal is to seek co-design opportunities of liquid cooling and power delivery to mitigate three major issues for 3D ICs: 1) power delivery instability, 2) power–I/O connections contention, and 3) design conflicts of liquid cooling – power supply.

#### 3.1 Large decoupling capacitors in cooling layer

To increase the amount of decap for better voltage noise suppression, we propose an approach to construct supercapacitors by using the structure of the liquid cooling micro-channels. The supercapacitors, based on the electrochemical phenomena of electric double-layer, can provide very high capacitive density, usually 10 to 100 times more energy per unit volume or mass than traditional electrolytic capacitors. However, the supercapacitors need a liquid-solid interface. We therefore propose to utilize the liquid-solid interface of the microchannel to create the electric double layers of supercapacitor. The doublefunctionality microchannels are therefore called coolingcapacitive microchannel (CCM). To evaluate the benefits of area, cooling and noise reduction when using the CCM, an architectural level chemical physics-electric simulation tool is needed that will extend our existing HotSpot tool and will be integrated in MultiSpot. The real-world benchmark programs will be tested based on this new cooling-power delivery structure. We also propose an approach to partition the micro-channel into multiple short segments to create distributed decaps instead of centralized large decaps. Based on the CCM we construct, we will also build high-efficiency on-chip voltage regulators (VR-CCM). The PDN with VR-CCM will be evaluated against real-world benchmarks.

A supercapacitor has three important components: current collectors, porous electrodes and electrolyte solution. To reuse the structure of liquid-cooling microchannel, we need to consider the double functionality CCM for both heat transfer and electric capacitance. We propose to use the two opposite walls of a cooling microchannel as the current collectors for anode and cathode of a supercapacitor respectively. This structure (Fig. 1) will not lead to the interaction between functions of cooling and electric capacitor for two reasons: 1) the coolant flows along the microchannel while the electric field is imposed perpendicularly to the microchannel walls 2) the heat transfer has much larger time constant than that of the response time of an electric capacitor. The material of the CCM walls should have the properties of high thermal conductivity, high electric conductivity and tensile strength at the same time. The metal materials, such as aluminum, iron and copper are the natural choices which work for both cooling and electric conductivity. The electrode material needs to be a porous material having high specific surface area, high thermal conductivity, high electric conductivity. High specific surface area porous material means rough surfaces in two opposite walls of microchannel. Previous studies showed the improved liquid-solid heat conductivity caused by rough surface.



Fig. 1 Structure of proposed enhanced microchannel supercapacitor (top view, top, side view, bottom)

Carbon-based materials including activated carbon, carbon nanotubes, carbon nanofibers, carbon onions and graphene are desirable materials for pure electric-double-layer capacitor. While transition-metal based materials and polymer-based materials may activate the electrochemical pseudocapacitance of the supercapacitor but sacrifice the thermal conductivity a bit.

The electrolyte system needs to have both high specific heat capacity and be suitable for supercapacitors. Aqueous electrolyte, organic electrolyte and ionic liquid are three wellstudied electrolyte systems for supercapacitors. The aqueous electrolytes are solutions containing solvent water and salt ions; pure water is the most common coolant of liquidcooling microchannels. The previous studies show an improved liquid-soild heat tranfer by adding salts to water to create aqueous electrolyte system.

The dynamic behavior of supercapacitors is slightly different from commonly used linear dielectric capacitors. We are building a more accurate equivalent circuit of supercapacitors by considering the nonlinear behavior to study the effectiveness of voltage noise reduction when using supercapacitors. The equivalent circuit of a supercapacitor can be used to enhance the PDN simulator VoltSpot and become part of the MultiSpot tool.

To evaluate the proposed CCM, we are working on a thermalelectric simulator to investigate the effects of cooling and voltage noise reduction. The thermal part is being enhanced to incorporate the ability of simulating liquid-cooling microchannels for 3D IC as part of MultiSpot. The accuracy of the proposed thermal-electric simulator is being validated against a commercial multi-physics simulator.

### **3.2** Temporal energy storage for power-I/O pin switching using CCM

The switchable power-I/O pin is an emerging technology which switches a subset of the I/O pins to power pins in power-hungry phases of the program, and vice-versa, based on the opposite trends of power-hungry phases and I/Ohungry phases. However, in many scenarios, the powerhungry phases and I/O hungry phases overlap each other, therefore the program has to be slowed down due to either power bottleneck or I/O bottleneck. We plan to utilize the supercapacitor of CCM to power up the processor temporally with limited power supply to shift overlap of power-hungry and I/O-hungry phases.

#### 3.3 Hierarchical 3D power delivery via cooling layer

To minimize the contention between power delivery and I/O connections, we propose a 3D hierarchical power delivery network design. This design joins the power delivery and liquid cooling systems and leads to more compact and efficient cooling-power co-design. We propose two separate schemes: one to insert metal wires in the intermediate space between the cooling layers, another one directly adopts the conductive walls of the CCM as wires. In each scheme, for each cooling layer, we propose to have one or several power redistribution layers to connect to the corresponding silicon layer. And one or more vertical coarse-granularity power distribution layers are built vertically to connect the power from PCB board to the in-cooling-layer power wires. The proposed 3D hierarchical PDN is being evaluated and benchmarked against traditional 2D power delivery designs with real-world benchmark programs.

#### 3.4 Horizontal power delivery via cooling layer

The liquid-cooling microchannels need to be placed in parallel to the silicon die to maximize the heat transfer interface area, while the traditional PDN of 3D ICs distribute current laterally in package through C4 pads and then spread vertically within multi-layers via TSVs. As a natural sequence, the lateral microchannels and vertical TSVs can easily block each other. The spatial connection between microchannels and TSVs causes high design complexity and lowers down the cooling effect and the total number of TSV (both power TSV and I/O TSV). We propose a hierarchical 4level 3D power delivery topology. Herein, a PDN of the proposed topology partially spreads power laterally in package level with fat metal layers, then redistributes vertically with fat metal layers vertically, and then spreads laterally along the direction of microchannels in the cooling layer with fine metal, finally redistributes to silicon layers with very fine metal layers. This topology minimizes the number and occupied area of the vertical cross-layer power TSVs and therefore reduces the spatial conflict between lateral cooling microchannel and vertical TSVs and contention between power TSV and I/O TSVs.

#### 3.5 Cooling-power-capacitive microchannel

Combining the idea of hierarchical 3D power delivery and cooling-capacitive microchannel (CCM), we propose to use the walls (collectors) of CCM as lateral power distribution wires, called cooling-power-capacitive microchannel (CPCM). This design further reduces the spatial contention between power delivery and cooling to allow more microchannels. In addition, by incorporating the capacitance of CCM to the hierarchical 3D power delivery, further voltage noise reduction is expected.

#### 3.6 Cooling-power microchannel

Finally, as another method for dual use microchannels we propose to use high-conductivity, liquid metal, as the coolant for the liquid cooling system; therefore the micro-channels are capable of both cooling and power delivery.

The cooling-power-capacitive microchannel utilize the walls of microchannels for power delivery. We propose an alternative design which utilizes both the liquid and the walls of microchannel for power delivery, called cooling-power microchannel (CPM). The CPM design simply merges the liquid cooling system and the power distribution networks into one joint system and therefore makes the joint system more compact than the previous schemes. Electrolyte solution cannot provide enough conductivity to delivery power, therefore we switch to high electric-conductive liquid material – liquid metal. Because power delivery needs two isolated networks for VDD and GND, we consider two separate but equivalent cooling-power subsystems for VDD and GND respectively. As a competitive design, the CPM will compare with the CPCM.



Fig. 2 Structure of proposed enhanced microchannel liquid metal (top view, top, side view, bottom)

### 3.7 Liquid-cooling-power delivery co-designs for 3D memory architectures

Micron's hybrid memory cube (HMC) is the first commercial 3D IC device which provides more than 15X the performance, 70% less energy than traditional DDR3 technologies and 90% less space than today's RDIMMs. However the number of silicon layers is limited by power delivery and thermal constraints. Since the HMC is a 3D memory architecture, more I/O bandwidth but less power supply than those of processors are required. We intend to evaluate the proposed cooling-power co-design techniques: cooling-capacitive microchannel, cooling-power-capacitive microchannel and cooling-power microchannel to the HMC. New trade-offs between I/O, power supply and cooling will be studied to better utilize the proposed cooling-power co-design schemes.

### 4 Preliminary Results

For the enhanced microchannel work we have tried to derive some first order estimations of the expected improvements which show that indeed these ideas can provide tremendous benefits that enable future 3D-IC development.

### 4.1 Microchannel supercap for use during brownouts or to provide extra power during boost

According to [5], the electrodes are 230µm in width, 10mm in length, 200µm interspace and 0.312µm thinkness, which leads to  $11.074\mu$ F/mm<sup>2</sup>. Think about a cooling channel 230µm in width and 31.2µm in height. The capacitive channel design lead to  $1.1074\mu$ F/mm<sup>2</sup>. Given the reference 3D IC system described in [Zha15b], the chip has an area of 44.12 mm<sup>2</sup> which leads to 48.858mF per cooling layer. Given the case of 10% frequency boost, we have 9.20W per each silicon layer (7.6W on 1GHz). The extra power needed is 1.60W. The theoretical extra energy can provided by supercap is  $\frac{1}{2}$ \*[2.7<sup>2</sup>-1.1<sup>2</sup>)\*48.858mF = 0.14853J which can support 1.60W extra power for about 93ms.

### 4.2 Microchannel using liquid metal for cooling and power delivery

According to [6], Gallium is the best candidate of liquid metal cooling, whose thermal capacity and viscosity are very close to those of water by much better thermal conductivity. We assume a 3D-IC system but replace the coolant with Gallium. The total area of fluidic via is  $1 \text{mm}^2$  (1% die area). The total length is 150µm given die thickness is 50µm. The total resistance is 40.5µOhm. While if use power TSV, [7] shows (240.4mV-118.8mV)/100A = 1.216mOhm; thus the liquid metal cooling strategy cut the power delivery resistance to 1/3 of the power TSV solution. Since Gallium is highly corrosive it imposes constraints on the appropriate electrical contacts to the PDN, luckily Tungsten, already a common metal used in IC fabrication can serve this role.

#### 4.3 PDN and Thermal modeling

Our prior work on HotSpot and VoltSpot has served the research community well, yet there are also many aspects that MultiSpot enhances: the possibility of PDN/thermal codesign, extensions for heterogeneous systems, multiple cooling methods including microchannel cooling, multiple power delivery solutions, including CCM, multiple decap solutions including supercapacitors, etc.

### 4.4 Architecture level modeling of power delivery and heat removal for 3D-IC

In order to fully take advantage of the proposed solutions we need to take into account the implications at the architecture and system levels. We already have extensive experience with cross-layer issues from our work on the HotSpot thermal modeling tool and VoltSpot power delivery tool that include physical and circuit level considerations in an architecture modeling infrastructure. For the MultiSpot project we include 3D-IC aspects, including enhanced microchannel cooling and voltage stacking into a computer architecture infrastructure that will include GEM5 for functional simulation, McPAT for power modeling, and our MultiSpot for power delivery and thermal modeling. In order to reflect the 3D-IC details GEM5 is being augmented with a 3D-NOC and a 3D mesh manycore topology that will map NOC routers and processor cores according to the 3D-IC stack, McPAT is being enhanced by adding fluid power, voltage stacking and explicit switchedcapacitor regulator details in the power number calculations, VoltSpot is being enhanced by the addition of conductive microchannels, supercapacitor structures, TSVs and switched-capacitor regulation, while HotSpot, enhanced with 3D-IC microchannel cooling, is being used for self-consistent power and thermal simulations for a heterogeneous SoC or SoP.



Fig. 3 Current architecture tools for thermal/PDN. Multispot enhances and replaces VoltSpot/HotSpot

#### 5 Conclusions and future work

The described methods can have a significant impact on the semiconductor industry and on society as a whole. By breaking the power wall for 3D-IC, thus providing a practical path forward for Moore's law, future electronic systems can continue to become smaller, less costly, with higher functionality and with longer lasting batteries. As with our previous tools we plan to release MultiSpot for wide usage by the research community.

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SESSION 6

# **SESSION 6** Quantiheat Project / Nanoscale Thermal Investigations

### **QUANTIHEAT Project: Main progresses**

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#### Abstract

The development of increasingly complex and nanostructured materials and devices, for example thermoelectric materials, nanocomposite polymers or micro- and nanosystems (microelectronics systems, MEMS/NEMS), requires in many cases an accurate knowledge of the thermal properties of the materials at the nanoscale. Scanning Thermal Microscopy (SThM) is a key technique for such thermal measurements with a submicrometric spatial resolution. The European project QUANTIHEAT "Quantitative scanning probe microscopy techniques for heat transfer management in nanomaterials and nanodevices" aims at solving the problems of thermal metrology at the nanoscale by delivering accurate and traceable metrology tools (nanoscale thermal terminologies, calibration samples and guidelines, modeling, novel SThM probes) for enabling the thermal management and advancing the development of new generation nanomaterials. The purpose of this article is to provide an overview of its main results after 3 years of running.

#### 1 Introduction

The QUANTIHEAT project is a 4-year project (from 1st Dec.2013 to 30 Nov. 2017) aiming at addressing the problem of thermal metrology at the nano-scale and at delivering validated standards, methods and modeling tools for nanothermal design and measurements.

A key promising technique for thermophysical properties measurements at the nanoscale is Scanning Thermal Microscopy (SThM), but this technique remains highly nonquantitative. The need is for a complete thermal measurement and modeling technology for use at the nanoscale.

The main expected outputs of the project are to be useful as practical standards in the real world. Accordingly, the project includes applications where materials are modified at the nanoscale during manufacturing processes due to thermo-dependent effects or have to be thermally characterized and optimized. The applications include thermal and UV-nano-imprint lithography (NIL), novel nanostructured micro-particle based interconnects materials, atomic layer deposition (ALD) and novel generation of nanostructured thermoelectric and thermal interface materials.

The tasks of the first project step "Specification and methodology" (Fig. 1) were achieved in period P1 (from 1st Dec.2013 to 30 Nov. 2014), providing the basis for the other R&D activities.



Figure 1: (a) QUANTIHEAT Consortium.. (b) QUANTIHEAT work packages / WP (in Subproject / SP) overall strategy.

The industrial application oriented specimens to be studied and the requirements for new generations of nanomaterials and processes were defined in details. The thermal characterization techniques and methodologies available in consortium for multi-scale analysis of heat transport at different length scales were specified. This enabled the identification of measurement and modeling pathways linking thermophysical measurements with industry specified materials (Fig.2).

A review of definitions and terminology currently used in the micro and nano-scale measurement community was undertaken and recommendations were made for terms and definitions applicable to SThM measurements. Uncertainty budget analysis methodologies were developed by NMIs. The requirements for calibration, test and scientific samples to be developed for evaluating the SThM measurement were specified and the test plans for experimental research to be carried out were established.

On this basis, in Period (from 1st Dec.2014 to 31 May 2016), first passive calibration, test and scientific samples as well as first sets of industrial sample (NIL resist thin films, ALD, TE and TI materials) were fabricated and disseminated for their measurements using various characterization methods including SThM (Fig.2).



New probes & instruments to perform SThM in combination with other techniques & software

#### Figure 2: Project philosophy.

At this stage of the project characterization results have been mainly aimed at improving the first sets of passive test samples. In accordance with the test plans to be performed with the samples selected by consortium for thermal calibration and thermomechanical calibration of SThM techniques, inter-laboratory comparisons and SThM measurements were initiated. Study of the first sets of samples allowed refining the industrial thermal characterization techniques to be developed and/or to be applied to solve critical aspects related to manufacturing processes, materials and characterization. Material and manufacturing process were developed, supported by

characterization results for NIL resist, ALD and interface materials. The fabrication process for the first version of four categories of active devices was completed and devices were characterized through modeling and measurements for the development of temperature reference devices and heater devices for the calibration of the SThM tip temperature and for thin film characterization using the 3-omega method. Measurements following the test plans established for temperature measurements started.

Supporting modeling activity provided BTE-based simulations of the thermal distributions of thin films and confined geometries heated with localized heat source and

numerical codes for heat conduction issues in many classes of nanomaterials with varying levels of details. Based on an overview of the available probe-sample interaction modeling approaches methodologies for treatment of more complex tip-sample geometries were established. Fast modeling tools were developed and speedup for experimental data analysis and for building more complex models.

First SThM measurements with the new instruments developed were demonstrated. This includes new and evolved SThM probes, new SThM-based techniques combining SThM with Scanning Electron Microscopy and Infra-Red radiometry, a novel SThM technique calibrated in a liquid environment and a novel thermal-force imaging mode.

The evaluation of SThM methods was initiated with the establishment of a first draft of calibration protocols for the SThM measurement of (i) thermal conductance, (ii) surface temperature and, (iii) phase change temperatures and the assessment of measurement uncertainties.

This paper will focus on first results obtained on one of the test sample categories, topography-free samples, the demonstration of the non-negligible impact of sample roughness on SThM measurement and some new results regarding the development of new SThM instruments and tools. Focus on other specific results will be presented through other communications during the workshop.

#### 2 Focus on some results

# 2.1 Topography-free samples: what is measured through purely SThM thermal contrast in active mode?

For use in the investigation of SThM response in active mode (SThM probe heated and used as heat source and thermal sensor simultaneously) to spatial variation in thermal conductivity with minimal topographic artefacts topography-free samples with lithographically defined features exhibiting different thermal conductivity and minimal (< 5 nm) topography were fabricated.

#### 2.2.1 Sample description

A series of various topography-free samples were fabricated by Glasgow University. All test samples indicate a height difference between the pattern and background of < 5 nm. The fabrication and initial AFM/SThM scans have been published (see references [1] and [2] for details on and basic thermal analysis of the sample).

For their fabrication E-beam lithography folowed Au lift-off on a sacrificial substrate.  $Si_3N_4$  was then deposited and spin casting of epoxy was used for adhesion to borosilicate. The last step is the deletion of the sacrificial substrate. The two surface materials are then Au 20 nm thick (pattern) and  $Si_3N_4$  400 nm thick (background). The body and base of the sample (not exposed to the scanned surface) consist of borosilicate glass (rear side) and epoxy polymer - SU8 photoresist (sandwiched between the front and back surfaces). As shown in Fig. 3, patterns can consist of lines (width from 200 nm to 500 nm) connected or unconnected to large gold squares.



Figure 3: 20 nm thick gold wire connected or unconnected to  $5x5\mu m^2$  gold pads. Wire width: 200 -500 nm (from Glasgow University).

#### 2.2.2 Method and measurement principle

For thermal properties imaging, the SThM probe is heated by passing a current through its resistive element. The probe and is used as a thermistor since the electrical resistance of the wire depends on its temperature. When the probe is brought to contact with the sample surface, a part of the heat generated inside the tip flows into the sample, which modifies the probe temperature and then its electrical resistance. The thermal control unit (Fig. 3.a) can adjust the electrical current so that the probe electrical resistance returns to the set point. The bridge voltage is monitored while scanning the sample surface.

Three types of resistive probes were used to image the topography free samples:

1. Wollaston wire microprobe (Fig.4.b : the cantilever arms are made of a Wollaston wire of diameter 75  $\mu$ m that involves enclose a core of diameter 5  $\mu$ m made of platinum/10% rhodium. The wire is etched at the tip over a length of length 200  $\mu$ m, so that the liberated core constitutes the heat sensitive element of probe. It is obtained by electrochemically removing the outer silver layer of the Wollaston wire and bent bending to form a probe of suitable shape.

2. KNT nanoprobes: the cantilever is made of Silicon Nitride (Fig. 3.c). The cantilever length, width, thickness are 150  $\mu$ m, 60  $\mu$ m and 0.4  $\mu$ m respectively. Tip radius is lower than 100 nm. The tip height and thickness are respectively 10  $\mu$ m and 40 nm and its width varies between 1.5 and 6  $\mu$ m.

3. Si doped nanoprobes: The cantilever consists of two micrometric legs with high doping level and a low doped resistive element platform (Fig. 3.d). The tip of a nanometric radius curvature (10 - 30 nm) has a pyramidal shape is mounted on top of the resistive element. These Silicon-based probes are batch-fabricated.



Figure 3: example of resistance measurement circuit used in active mode (a.). SEM images of the Wollaston thermoresistive probe (b.), the standard Pd probe ((c.) these probes are commercialized by KelvinNanoTechnology, UK) and (d.) the Anasys Instruments microfabricated Si probes [3, 4].

#### 2.2.3 Some results

Fig. 4 gives the images we obtained for experiments performed under ambient air conditions for the thinnest lines of the samples presented in Section 2.2.1 with a Wollaston wire probe and a silicon doped nanoprobe.

As previously obtained with the KNT probe by Glasgow University [2] with a better thermospatial resolution in the case of the Wollaston wire probe the gold 200 nm width-line is detected when it is connected to the gold squares and this is not the case when the line is unconnected. This clearly illustrates that in SThM the contrast in a thermal image and the measurement correspond with thermal conductance measurements and demonstrates that SThM measurement strongly depends on the sample geometry. Local quantitative measurement cannot be direct \_a calibration of the system with bulk reference samples is not sufficient and requires the analysis/modeling of the thermal behavior of the whole system: probe, sample and environment [3]. We note that even if the boundary resistance locally changes when the line is not connected to the pads it is not detected. Experiments under vacuum have been planned to estimate the real contribution of this boundary resistance to the measurement. As previously shown for the presented results the main heat transfer mechanism to be considered between the Wollaston probe and the sample is the air conduction [3].

In the case of the silicon doped nanoprobe topography measurements (Fig. 4. e. and g.) are strongly disturbed by optical interferences also observable in the thermal contrast (Fig. 4. f. and h.). The heat transferred from the heated

cantilever to the sample through air leads to a deformation of the surface features. This kind of probe is clearly not adapted for thermal imaging under ambient air conditions and requires to be operated under vacuum conditions [5].



Figure 4: (from CNRS). Topography images (a., c., e., g.) and thermal contrast images (b., d., f., h.) of patterns consisting in a gold line of width 200 nm, connected (a., b., e., f.) and unconnected ((a., c., e., g.) to two  $5x5\mu m^2$  gold pads. Images (a., b., c., d.) were obtained with a Wollaston wire probe. The other with a silicon doped nanoprobe.

#### 2.2 New Instruments

The measurement environment and geometry within the QUANTIHEAT project include inter-laboratory comparison of SThM in air, dry gases and controlled humidity high vacuum environments. These have expanded beyond current state-of-the-art via increase of the heat flux sensitivity and spatial resolution in pioneering the development of nanoscale resolution immersion passive thermometry in liquid environment [6] and full liquid immersion active SThM probes [7]. In particular, the study of the sample topography and application roughness influence on the SThM [4, 8] and recently prototyped simultaneous shear force - thermal measurements transport mapping [9], should allow monitoring the contact area thus eliminating one of major uncertainties in nanoscale SThM measurements. This problem have been also addressed by the development of an combined SThM /SEM system [10] that offers advantages in terms of exact positioning of the tip with respect to the sample, live tip evaluation and observation of tip contamination during scanning. More precise study of the probe/sample interaction will be then possible.

The ability to utilize the wide variety of probes available have been facilitated by the development of a software system to suppress topographic artifacts arising during scanning. These differ substantially between different probe types and must be accounted for if the results obtained using different probes are to be comparable.

### 2.2.1 SThM in combination with SEM developed and tested

The combined SThM/Scanning Electron Microscopy (SEM) instrument that we developed is based on a home made Atomic Force Microscope (AFM). This AFM was designed to present a low profile and a reduced footprint. In such a way, we can keep all the positioning possibilities offered by the five degrees of freedom of our SEM (FEI Nova NanoSEM 450) stage. An optical fibber interferometer was preferred to a more commonly used optical beam deflection detection system (Fig. 5). This permits a more open architecture. The tip sample force contact is managed by using the optical signal delivered by the interferometer, giving the absolute displacement of the tip.

For combined SThM/SEM measurements, the SThM probe is integrated into the AFM instrument and connected to a home made thermal control unit, which can be used in passive and active modes of SThM, and in dc and ac regimes.



Figure 5: Electron image of a KNT probe scanning a NT-MDT calibration sample ©CNR.

We have demonstrated with this equipment that SThM measurements and imaging can be performed without perturbation linked to the electron beam.

Imaging was performed on various test samples. Fig. 6 gives topography and thermal contrast images obtained at the surface of a Si substrate covered by 100 nm of SiO<sub>2</sub> and locally by 80 nm of titanium. The interface between SiO<sub>2</sub> and Ti is studied. The voltage measured at the TCU output (representative of the electrical resistance of the tip and then of its temperature in that case) on Ti is lower than that for SiO<sub>2</sub> in the thermal image due to the largest heat loss from the probe to the metallic material.



Figure 6: Topography and thermal contrast (dc measurement with a KNT probe) images obtained with the combined SThM/SEM developed at CNRS at the interface between Ti and SiO<sub>2</sub>. The sample is here a Si substrate covered by 100 nm of SiO<sub>2</sub> and locally by 80 nm of Ti.

### 2.2.2 Development of software for real-time data processing

CMI have developed a Finite Difference Method solver for simulating whole SThM images. Fig. 7 gives an example of simulation of the thermal contrast linked to topographical artifact at the surface of a microchip.



Figure 7: (left) topography and (right) simulated thermal SThM image of a microchip surface ©CMI.

### 3 Conclusions

We are now two years into the QUANTIHEAT project and we are sailing at full speed. There has been a lot of work over the past year and partners have been working hard on both technical implementations as well as striving towards the best possible impact of the outcomes. After the set-up of the project during the first year, its technical implementation follows the original schedule. In 2016, we have seen important progress on the design and characterization of relevant samples using the various techniques available within the consortium. This article gives some examples of obtained results. We invite the readers to visit our Web site (http://www.quantiheat.eu/) to know better our works.
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### Calibration methodologies for scanning thermal microscopy

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#### Abstract

This work analyses the heat transfer between various scanning thermal microscopy (SThM) probes and samples. In order to perform quantitative measurements with SThM techniques, we have developed well-established and reproducible calibration methodologies. We present here two approaches of the SThM measurement: one to measure thermal conductivity of solid materials with a Wollaston SThM microprobe and a second one to evaluate phase transition temperatures of polymeric materials with a silicon low-doped nanoprobe. Based on the comparison of experimental data and modeling results, we have estimated the local resolution of the microprobe to be associated to a radius of 300 nm. Concerning the nanoprobe, we have demonstrated the strong dependence of measurement on sample topography and roughness.

#### 1 Introduction

Recent developments in the miniaturization of thermal analysis techniques - by combining scanning probe microscopy with thermal sensors (scanning thermal microscopy (SThM)) - offer interesting opportunities for the spatially-resolved thermal analyses of polymer and solid surfaces [1]. In the imaging mode, the topography and the thermal exchange with the surface can be visualised in the same time with expected good thermal and spatial resolutions. The lateral resolution is often expected to be sub-micrometric due to the small curvature radius of probe. Local thermal analysis (LTA) can also be performed on selected spots by following the response of the probe during a controlled fast heating while the tip remains in contact with the surface [1][2][3].

In the case of the Wollaston microwire SThM setup introduced about 20 years ago, the atomic force microscopy (AFM) probe is replaced by a resistive wire of a metallic alloy (platinum/10% rhodium). The thermal field in the probe is well-controlled since its moderate size does not lead in principle to small-scale effects. However, the spatial resolution stays micrometric, so that the technique does not provide a large improvement in comparison with Rayleighlimited optical techniques.

More recently-introduced nano-thermal analysis (nanoTA) involves a higher aspect-ratio AFM-like silicon probe on which the sensor is deposited at the back of the cantilever, so that the spatial resolution of the AFM is not degraded by the presence of a bulky thermal sensor. The topography resolution is clearly improved in comparison to Wollaston

probe-based SThM. Improvement in spatial resolution of the thermal signal has also been demonstrated, especially in vacuum [4].

While obtaining a qualitative thermal signal in SThM is quite simple, the key point to be quantitative is to develop well-established and reproducible calibration techniques [5][6][7][8], which are currently lacking. The aim of the present paper is to explain our recent calibration methodologies developed for the two SThM techniques aiming at measuring thermal conductivity and phase transition temperatures. The work is complementary to previous attempts [4][9] in the sense that it can tackle both solids and polymers in ambient conditions.

#### 2 Methodology and results

All measurements were performed under ambient conditions, i.e. at ambient pressure ( $\sim$ 1 bar) and temperature (T  $\sim$  298 K). The relative humidity was not controlled, but is usually in the range 40-60%.

### 2.1 Case of the Wollaston SThM microprobe: thermal conductivity calibration

#### Measurement principle:

The experiments with the Wollaston microprobe were performed on a Park Instrument CPR AFM combined with a home-made thermal control unit (TCU, figure 1). The Wollaston microprobe is one of the elements included in a Wheatstone bridge. When the microprobe is heated by a direct current (DC), the heat flows from the tip to the sample causing a decrease in the tip temperature and so a change in the tip electrical resistance  $(R_p)$ .

This decrease in temperature is directly related to the sample properties and induces a change in the output voltage ( $\Delta V$ ) in the Wheatstone bridge.



Figure 1: Schematic of the thermal control unit used for measurement with the Wollaston wire microprobe.

#### Main results:

Heat transfer between the probe and a sample occurs by different channels [1]: through the air, involving convection, diffusion and ballistic transport, through the tip-sample

Total number of elements	4761032	
Minimum element size	9.14 nm	
Tip mesh number of elements	2275301	
Air mesh number of elements	2108523	
Sample mesh number of	277208	
elements	377208	
Tip-sample distance	240 nm	
Maximum simulation time	15 min	



Figure 2: Finite-Element Method (FEM) simulation of heat conduction through air in the diffusive regime. Mesh characteristics for a tilted tip configuration. The colors indicate the mesh elements size distribution.

contact, involving constriction resistances and through possible meniscus due to capillary condensation of ambient humidity, and through thermal radiation.

The last mechanism is usually neglected or embedded in an effective way into the contribution of another mechanism, as it is expected to be small (and not to be modified depending on the conditions of the experiment).

The problem of the air heat transfer is that it is delocalized: it can spread over microns. In the case of the Wollaston microwire, we have verified that the associated length can be on the order of 10 microns [8]. In addition, we have demonstrated that the probe feels already the sample when it is retracted at 200 microns over it. By numerically reproducing the experiment when the tip is out of contact in a Finite-Element Method (FEM)-based framework (figure 2), we have demonstrated that heat convection can be neglected and that only heat diffusion takes place.



Figure 3: Difference between the experimental signal and the prediction by the FEM simulation: thermal transfer at the contact.

We showed that the angle between the axis of the V-shaped Wollaston probe and the sample can be determined out of contact. Such an analysis already provides some of the parameters required to calibrate the experiment. We have then shown that heat diffusion is not sufficient to reproduce the experimental signal in contact: while the numerical and experimental data match perfectly when the tip-sample distance is larger than 10 microns. There is a difference in contact. This difference is of course due to the other heat transfer mechanisms, but also to the deviation from the purely diffusive regime of air heat transfer important at the shortest tip-sample distances. We have therefore introduced a calibration curve, which depends on a series of wellknown materials with thermal conductivity in the range 0.2-10 W.m<sup>-1</sup>K<sup>-1</sup> (polyimide, SiO<sub>2</sub>, ZnS, ZrO<sub>2</sub>, CdSe) and allows determining precisely how to deal with the contribution close to contact and in contact. This method enables to split the contribution of the air, and the contributions of the other transfer mechanisms, which are more local (see figure 3).

The split is done by introducing  $\Delta(\Delta T)$ , a variation of temperature, and not a conductance: it therefore also directly includes possible contact conductances which are often difficult to determine. It is interesting because such a curve allows splitting the local transfer to the delocalized one which can be computed numerically if the geometry is known [10]. This method has allowed us to determine the radius associated to the lateral spatial resolution of the contact mechanisms, which is about 300 nm in the case of the Wollaston SThM microprobe [8]. Note that the technique is able to resolve temperature differences down to 0.05 K.

# 2.2 Case of the silicon NanoTA probe: temperature calibration

#### Measurement principle:

The experiments with the silicon nanoprobes were made with a NT-MDT -NTegra Aura AFM operating with the Anasys Instruments NanoTa module. For polymers, a thermomechanical method is used for the measurement of the phase transition temperatures: measurements are performed on selected spots of the sample surface by following the deflection of the cantilever supporting the nanoscale tip during a controlled fast electrical heating of tip while this tip remains in contact with the sample surface (figure 4).



Figure 4: Principle of the measurement in the NanoTa mode.

#### Main results:

We first note that the heater is made of a low-doped silicon area on the cantilever. While this constitution allows for a more compact design, it results also that a displacement of the laser spot location on the cantilever can strongly modify the probe electrical resistance because the charge carrier density depends on illumination (figure 5). Such phenomenon can induce erroneous calculation of the tip temperature. A method to ensure precise positioning of the laser spot on the lever, which is based on the measurement of the probe electrical resistance value (figure 1) and deflection signal while the tip is out of contact and in contact with a silicon sample was developed.



Figure 5: Silicon NanoTA probe electrical resistance variation depending on heating voltage and laser illumination.

#### Proposed calibration method:

Four polymeric samples (PCL, PE, POM, PET) with wellknown melting temperature (respectively 62 °C, 110 °C, 168 °C, 250°C) (measured by Differential Scanning Calorimetry (DSC) at the National Physical Laboratory) were used to calibrate the applied heating voltage into a temperature scale (figure 6). A special mode (power feedback) allowing the detection of the melting temperature close to ambient temperature was used and a ramp voltage of  $0.03 \text{ V.s}^{-1}$  was applied to the probe.



Figure 6: Calibration curves. Cantilever deflection for four polymer samples with well-known melting temperature (in blue) and corresponding temperature curve (in black).

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To check the relevance and the accuracy of the calibration, comparisons with melting temperature  $(T_m)$ DSC measurements for four LDPE (polyethylene) samples manufactured from the same raw material but with different cooling rates (60, 40, 20 and 5 °C.min<sup>-1</sup>) were first done. This has also allowed continuing our study of the influence of the polymer crystallinity on the melting temperature  $(T_m)$ . For a given  $T_m$  measurement method (SThM or DSC),  $T_m$ values measured appear to be similar across all four samples whatever the crystallinity: around  $94 \pm 2^{\circ}C$  for SThM and about 110°C using DSC. Unlike our previous works on semi-crystalline materials (IPP and PBT) of various crystallinity degrees the crystallinity does not impact the  $T_m$ . The influence of the polymer crystallinity on its  $T_m$  then depends on the material. Why a so large difference between the  $T_m$  values measured by the both used techniques?

We performed glass transition temperature  $(T_g)$  measurement on two PMMA samples with different surface states; one was prepared by means of microtomy showing a micrometric surface state and the other using ultramicrotomy shows a nanometric surface state (see figure 7).



Figure 7: Polymer PMMA a) prepared by microtomy (surface state with micrometric variations) and b) prepared by ultra-microtomy (surface state with nanometric variations).

We detected  $T_g$ , but the values were found to be strongly surface-state dependent. Values obtained on PMMA prepared by ultra-microtomy were found to be repeatable and showed small dispersion ( $T_g = 128 \pm 2^{\circ}$ C) whereas values obtained on PMMA prepared by microtomy varied more ( $T_g = 90 \pm 7^{\circ}$ C) (Figure 8).

This means that despite its strong sharpness the NanoTA tip still requires very flat samples: its height is too small (3-6  $\mu$ m) to be able to deal with variations of few micrometers on the surface sample, which impact strongly the thermal signal through air heat transfer. This could explain the difference in  $T_m$  values measured by SThM and DSC on LDPE samples and previously presented.



Figure 8: Deflection curves on PMMA prepared by microtomy and ultra-microtomy showing glass transition temperature.

#### 3 Conclusion

Scanning thermal microscopy (SThM) allows measuring either local thermal conductivity or local phase change temperature. For both applications, precise calibration method is required to be able to compare the different results and ensure their repeatability. It is known that the microprobe can deal with rough samples [11]. In contrast, we find that the nanoprobe depends strongly on the surface state of the sample. The microprobe heat exchange can be associated to a radius of 300 nm and the delocalized contribution can be separated from the local one. The thermal conductivity calibration requires a set of materials with varying thermal conductivities while phase change temperature measurements require a set of materials undergoing transitions. We introduced examples of possible calibration samples and showed that their qualities are key to the following measurements.

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### Thermal Analysis of Advanced Microelectronic Devices Using Thermoreflectance Thermography

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#### Abstract

Shrinking features and growing device complexity with today's advanced devices has led to increased challenges of gaining a full understanding of device thermal behavior. At the same time, with higher power densities having a full understanding of the device static and dynamic thermal behavior is essential for ensuring optimal tradeoffs between performance and device reliability. Thermal imaging based on the Thermoreflectance Principle can meet the challenges imposed by these advanced devices by providing sub-micron spatial resolution and temporal resolution in the picosecond range. This thermal imaging concept will be described in this paper and compared to traditional imaging techniques. Several case studies will be presented to further illustrate the advantages of the thermoreflectance technique for thermal imaging.

#### 1 Introduction

Detecting time-dependent thermal events on a submicron scale and identifying those that represent potential device defects that may lead to an early failure is a challenge in the thermal analysis of today's complex electronic devices. The scaling of device features results in a significant reduction in time response and an increased sensitivity to transient events. With today's complex devices, very small localized temperature 'hot spots' can occur due to an unintended functional anomaly in a circuit with a tight design margin or a timing perturbation resulting from a small change in capacitance or another parameter elsewhere in the circuit. As device features continue to shrink, so do the challenges of detecting circuit-induced thermal defects. While gaining a full understanding of the device thermal behavior is getting more difficult, extremely high power densities is increasing the importance of having this understanding. Clearly only knowing the average temperature behavior is not sufficient. It is necessary to have a clear understanding of temperature distributions with submicron resolution to detect local hotspots and nanosecond, and even picosecond, temporal resolution to observe time-dependent thermal events with today's high speed devices.

In this paper, an overview of the merits and demerits of various techniques for measuring device thermal behavior will be presented. A thermal imaging technique based the thermoreflectance principle will be described in detail and it will be shown how it can be used to thermally analyze today's advanced device structures. The Thermoreflectance Thermal Imaging (TTI) technique with illumination wavelengths in the visible range enables submicron spatial resolution and can be combined with temporal resolution in the nanosecond range to meet the requirements necessary to fully evaluate the thermal behavior of these advanced complex device structures. Several case studies will be described to illustrate the benefits of this approach.

#### 2 Thermoreflectance-based thermal imaging

As the temperature of a material changes, the refractive index, and therefore, the reflectivity of the material also changes. Thermoreflectance thermal imaging is dependent on the accurate measurement of the relative change in the surface reflectivity as a function of the material's temperature. The change in reflectivity is dependent on the Thermoreflectance Coefficient, a basic material property that is a function of the illumination wavelength, the material and its surface characteristics, and the ambient temperature. Fortunately for the range of ambient temperatures of interest the Thermoreflectance Coefficient,  $C_{\rm th}$ , can be considered constant. A first order relationship between the normalized change in illumination reflectivity and the change in material temperature can be approximated as:

$$\frac{\Delta R}{R} = \left(\frac{1}{R}\frac{\partial R}{\partial T}\right)\Delta T = C_{th}\,\Delta T$$

As  $C_{th}$  is quite small (~10<sup>-6</sup> to 10<sup>-3</sup>) [1], a lock-in technique is employed to enhance the signal to noise ratio (SNR) and with time averaging and pixel by pixel calibration over the region of interest, <0.1 °C temperature resolution can be achieved. With illumination wavelengths in the 400 nm to 900 nm range, TTI ensures sub-micron spatial resolution to meet the imaging requirements for today's advanced devices. In contrast, traditional infrared imaging has a resolution in the range of 3 to 5 microns. Figure 1 shows a schematic diagram of the TTI system and a photograph of the Microsanj TTI system used for this work.



Fig. 1: Schematic diagram of TTI system is shown on the left with photograph of equipment on the right.

#### 3 Transient Thermal Analysis with TTI

As suggested earlier, having a full understanding of timedependent thermal events can be extremely important with today's complex devices. Optimal trade-offs between electrical and thermal behavior can only be attained by knowing and understanding the device thermal behavior under normal operating conditions. Time-dependent thermal behavior with picosecond temporal resolution can detect thermal anomalies that would otherwise go undetected.

Fig. 2 shows the timing sequence to obtain the thermal transient behavior. The device excitation pulse is selected to be of sufficient duration for the device to reach maximum operating temperature and a relatively low duty cycle is employed to enable the device to cool prior to the next pulse. The LED illumination pulse is delayed from one cycle to the next to obtain a complete picture of the thermal response.



Fig. 2: Timing sequence for transient thermal analysis to determine time-dependent thermal behavior

#### 4 TTI calibration

As with any analysis technique, calibration is key to ensure thermal images that convey the information necessary to truly understand a device's thermal behavior. Determining the thermoreflectance coefficient,  $C_{th}$ , under static conditions for a specific region of interest is quite straightforward. Under dynamic conditions, however, accurate calibration for devices with sub-micron features is further complicated by the expansion and contraction that takes place when the device under test, DUT, is thermally cycled. Shifts in the x-y plane during the averaging period can lead to errors in calibration and expansion in the z-axis with high magnifications can lead to blurred images.

To address these complications our imaging approach includes a 3-axis piezo stage and controller [2]. With this approach, the errors between successive images is fed back to

the controller to reposition the stage to compensate for both the x-y shift and image defocusing. The results are illustrated in Figure 3 where the image on the left is without the 3-axis controller activated. The image on the right with the controller activated shows a more uniform  $C_{\rm th}$  calibration and a clearer view of the device features.



*Fig 3: High magnification image with (right) and without (left) x-y-z imaging stage/controller* 

#### 5 TTI versus infrared thermography

Both infrared thermography (IRT) and TTI are accurate methods of providing whole-field surface temperature distributions because they are non-contacting. However, TTI has some advantages over IRT because it has an order of magnitude much higher spatial resolution. With illumination wavelengths in the 300 nm to 900 nm range, TTI ensures submicron spatial resolution (0.3 to 0.5  $\mu$ m) to meet the imaging requirements for today's advanced devices. In contrast, traditional infrared imaging has a resolution in the range of 3 to 5 microns at best. Also, surfaces of devices often have very low emissivity which introduces greater inaccuracy in IRT. The above observations are illustrated in the following case studies.

The first case study [3] is the measurement of the gate temperature of a Power Amplifier (PA) Microwave Monolithic Integrated Circuit (MMIC) device which consisted of two gates of length 150 $\mu$ m. As illustrated in Fig. 4, the PA MMIC was soldered onto a Cu-Mo carrier with silver-epoxy adhesive and assembled inside an aluminium jig for thermal characterization using TTI and IRT. Finite element analyses (FEA) were carried out using the mesh shown in Fig. 4. The temperature measurements are shown in Fig. 5 and compared with results from FEA in Fig. 6. It can be seen that the agreement between TTI and FEA is much better than between IRT and FEA. The primary reason for the better agreement with FEA is the much better 0.3  $\mu$ m spatial resolution for TTI compared to 5  $\mu$ m for IRT.



Fig. 4: Three dimensional FEA thermal model of the PA MMIC package



(a) (b) Fig. 5: Temperature distribution of a Power AmplifierMMIC device obtained using (a) TTI, and (b) IRT



*Fig. 6: Comparison of MMIC gate temperatures measured using TTI and IRT with those calculated from FEA.* 

In a second case study, both TTI and IRT were used to image the temperature distribution of a  $120\mu$ m heater with 4 $\mu$ m lines that have been fabricated on top of a microcooler with an insulating oxide layer in-between [4]. The thermal images obtained are shown in Fig. 7 where it can be seen clearly that the better spatial resolution of the TTI system was able to provide a more differentiated temperature distribution compared to that from the IRT system.



Fig 7: A comparison of thermal images using TTI and IRT.

# 6 Analysis of thermal behavior of an integrated circuit

Transient thermal testing of integrated logic circuits can provide valuable information about defects and potential failure modes in complex microelectronic structures by detecting non-uniform temperature distributions and hot spot locations [5]. Using a lock-in transient thermal imaging technique as described in this paper, a heating sequence can be observed in a series of temperature maps over time as the device cycles through a complex startup process.

Figure 8 shows the optical image of an unencapsulated IC device with a  $1.6 \times 1.1 \times 0.5 \text{ mm}^3$  Si chip. The device is biased via gold wire-bonded connections. After the device is initialized, a V<sub>dd</sub> of 0 V – 5.4 V pulse signal is applied to operate the active area of interest under temporary extreme conditions. Under these conditions the current is latched until the bias supply is cycled off and then on again.



*Fig. 8: Optical image of an unencapsulated integrated circuit with the area of interest shown with 20X zoom* 

Fig. 9 shows the thermal intensity map sequentially in time from 0.5 ms to 3 ms. In the beginning of the sequence a portion of the circuit at the top left corner begins to heat up. After 1.0 ms, the temperature of that location declines and another portion of the circuit at the top center begins to heat up.



Fig. 9: Series of thermal intensity contour maps versus elapsed time after an applied bias. The brighter locations indicate higher temperatures. The temperature scale is the same for all of the images. Note that the right side top portion heats up relatively quickly after 1.0 milliseconds.

Fig. 10 shows the 3-dimensional intensity map at 1.2 ms. The vertical axis shows the temperature calibrated by the surface light reflectance coefficient of this IC for light of 470 nm wave length. Fig. 4 shows an overlay of the thermal intensity on an optical image of the IC device. In this particular device, a few logic sections, circled in the lower right, undergo latch-up, resulting in a 250 mA current through  $V_{dd}$  rather than the typical 10 mA. This high current causes the power path temperature to rise as shown in the thermal image. Additional measurements with an alternative power configuration confirmed that the bottom right is the location of the latch-up.



Fig. 10: 3D temperature contour map zoomed at the right side at 1.2 ms elapsed time after applied bias. The Z-axis and color scale show the temperature rise. Heating in the metal traces shows the current flow to the latch-up location.



Fig. 11: Thermal intensity map over-layed on optical image of the device at 20X as in Fig. 10. The latch-up location is circled at the lower right.

#### 7 Transient analysis of a power diode

It has been demonstrated that high-speed transient thermal imaging can provide the thermal response of small electronic devices with up to 800 ps temporal resolution [6]. Such thermal transient data can be used in conjunction with structure function analysis to obtain values of thermal resistance and capacitance of layers of different materials along the heat flow path. This is illustrated in the next case study where the device under test is a 100  $\mu$ m wide diode with top gold contacts. The thermal image and the intensity overlay on the optical image 1 ms after application of a 715 mA pulsed bias are shown in Figs 12 (a) and (b), respectively. Fig. 13 shows the mean temperature response, averaged over several repeating cycles, at the marked location of the left contact (anode).



Fig. 12: (a) Color scaled thermal contour and (b) Thermal intensity contour, both of which are over-layed on optical image of the power diode device.



Fig. 13: Time response of the relative reflectance change, which correlates linearly with the temperature change and shows the behavior of the transient thermal response of the power diode.

Thermal network analysis using network identification by deconvolution and the structure function method [7] is generally applicable for these relatively simple structures. Using T3SterTM [8], the acquired time series data is converted to the analog signal through a D/A converter and put into the T3Ster system to obtain the cumulative structure function shown in Fig. 14. The results of the analysis show that there are four major thermal resistances in the thermal network; the active device portion of the semiconductor, the interface to the electrode, the electrode pattern, and the thermal path through the substrate to the thermal ground. The

time response function for these microscale devices requires a time resolution ranging from 10 ns to 1  $\mu$ s (10<sup>-8</sup> to 10<sup>-6</sup> seconds). This is possible with the lock-in thermoreflectance technique, but not feasible with conventional IR thermography.



Fig. 14: Cumulative structure function, C<sub>th</sub> vs. R<sub>th</sub>

#### 8 Thermal analysis of flip chip packages

Fig. 15, shows the structure for an array of silicon lateral double-diffused metal oxide (LDMOS) transistors designed for high power operation. [9]. As can be seen in the figure, the top side of the device has multiple metallic contact layers and a passivation layer. The uneven surface with different materials having different thermoreflectance coefficients complicates imaging with visible light on the top side if the goal is to analyze the thermal characteristics of the transistor itself. The back side of the silicon however, is smooth and uniform and with Near-IR illumination provides a better solution for analyzing the junction thermal behavior.



Fig. 15: Cross sectional view of LDMOS transistor array

The topside and backside thermal images obtained with thermoreflectance are shown in Figure 16. The top side image shows the temperature distribution for the metal layer of the device while the backside image shows the thermal image for the transistor array observed with Near-IR illumination through the silicon substrate. Each short line on the backside image corresponds to a specific transistor in the array, clearly showing the temperature distribution between drain and source contacts.



Fig. 16: Topside metal surface thermal image and transistor thermal image obtained with NIR thru-the-substrate

#### 9 Conclusion

In this paper, the thermoreflectance thermal imaging (TTI) technique has been described and several examples of its successful use for thermal characterization of today's submicron devices have been presented. In particular, a few examples have shown that this technique is superior to infrared thermography as it has the submicron spatial resolution required for today's submicron devices. By using light in the Near-IR range to which silicon is transparent, TTI can be used to study the thermal behavior of transistors in flip chip packages. It also possesses good temporal resolution in the picosecond range which can enable it to be used effectively to study transient thermal behavior of devices.

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### Modelling and Measurement of the Thermal Conductivity of Composites with Silver Particles

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#### Abstract

The effective thermal conductivity of composites made up of silver micro-particles embedded in a resin matrix is modelled and measured. This is done for spherical and flake-like particles to analyse the effects of the particles geometry and concentration on the composite thermal performance. It is experimentally found that spherical particles yield a higher thermal conductivity than the one given by flakes, such that it takes the value of  $16 W m^{-1} K^{-1}$  for a 50% volume fraction of particles. Furthermore, this behaviour is well described by a simple and analytical model, which takes into account the particle-particle interactions through a crowding factor. The obtained results could be useful to optimize the design and manufacture of composites with metallic particles.

#### 1 Introduction

Thermal interface materials (TIMs) are critical for optimizing the thermal contacts between two surfaces and improving the heat dissipation across them. This is particularly important in electronic devices, whose performance, power, lifetime, and miniaturization rely on the effective dissipation of heat [1-5]. The thermal conductivity of TIMs represents the bottleneck for the heat flow through the mating surfaces, which are usually not smooth neither at the same temperature. Among the wide variety of TIMs (e.g. adhesives, solders, gels, pads, and pastes), those based on a metallic paste have become of great interest due to their relatively high thermal conductivity [4, 5]. A thermal paste consists of a matrix that is filled with a thermally conductive solid in the form of particles. The particle size is usually in the order of microand nanometers, which allows filling up the microscale valleys in the surfaces topography and keeping the squishability and spreadability of the paste. As the number of conductive particles increases, the thermal conductivity of the thermal paste increases, but its conformability decreases, and therefore the solid content should not be excessive[6]. The geometry and concentration of the particles drive the thermal performance of these composites, but their effects are not well quantified to date, especially for high particle concentrations [7-9]. A detailed modelling of this composite thermal conductivity is therefore required.

The objective of this work is to model and measure the effective thermal conductivity of composites made up of silver particles embedded in a resin matrix. Considering spherical and flat (flakes) particles, we analyze the effects of

the particles geometry and concentration on the thermal performance of these compounds, aimed at optimizing their design and manufacture, for applications as TIMs.

#### 2 Theoretical model

The modelling is analytically done for composites made up of metallic spheres and flakes embedded in a resin matrix, as shown in Fig. 1(a)-(b). The thermal conductivity of the particles and resin are  $k_p = 419 \text{ Wm}^{-1}\text{K}^{-1}$  and  $k_m = 0.3 \text{ Wm}^{-1}\text{K}^{-1}$ , respectively.



*Figure 1: (a) spherical and (b) flake-like particles embedded in a resin matrix.* 

As the particles concentration increases, the heat conduction through one of the particles inside the composite is strongly affected by the presence of its neighbours, which is usually not taken into account by classical models. The effect of this particle-particles interactions on the composite thermal conductivity k can be described by means of a crowding factor ( $\gamma$ ) defined as the effective volume fraction of particles [10]. This crowding factor model establishes that  $k = k_m \exp[Cf/(1 - \gamma f)]$ , where *C* is a constant determined by the behaviour of *k* at the dilute limit (*f*<<1), and *f* is the particles concentration. For particles with a random spatial distribution, the comparison of this expression in the dilute limit with Nan *et. al.* model [11], which is suitable for low particles concentrations, yield the following thermal conductivities  $k_{sphere}$  and  $k_{flake}$  for composites with spherical and flake-like particles, respectively:

$$\frac{k_{sphere}}{k_m} = \exp\left[\frac{3\lambda f}{1 - \lambda(1 + 0.89f)f}\right],\tag{1a}$$

$$\frac{k_{flake}}{k_m} = \exp\left[\frac{(2\beta_1 + \beta_2)f}{3 - \beta_2 f}\right],\tag{1b}$$

where

$$\lambda = \frac{1 - (k_m/k_p + a_K/a)}{1 + 2(k_m/k_p + a_K/a)},$$
(2a)

$$\beta_1 = k_p / k_m - 1, \tag{2b}$$

$$\beta_2 = 1 - (k_p/k_m + a_K/d),$$
 (2c)

and  $a_K = Rk_m$  is the Kapitza radius, whose effect strengthens as the average radius  $a = 5 \ \mu m$  (thickness  $d=1 \ \mu m$ ) of the spherical (flake-like) particles, reduces. Smaller particles are more sensitive to *R* and hence should yield lower *k*.

The interface thermal resistance  $R = R_{Ag-Ag} + R_{Ag-resin}$ accounts for the particle-particle ( $R_{Ag-Ag}$ ) and particle-resin ( $R_{Ag-resin}$ ) interface effects and was determined through the following formula

$$\frac{\Delta T}{q} = \frac{L}{k_p} + R,\tag{3}$$

where the average heat flux *q* is numerically determined using the finite element method [12], after imposing the temperature difference  $\Delta T$ , as shown in Fig. 2. The result thus obtained is  $R = 260 \text{ m}^2 \text{K/GW}$  ( $a_K = 78 \text{ nm}$ ).



Figure 2: Typical SEM image of the considered Ag/resin composites used to determine the interface thermal resistance between the silver particles and the resin matrix.

#### **3** Experimental procedures

#### **3.1** Samples preparation

Composites made up of silver micro-particles embedded in a resin matrix were provided by the Amepox company. Samples with different volume fractions of spherical and flake-like particles were considered to analyse the shape effect on the overall thermal performance of the composite. The dimensions of the solid samples were 25 mm x 9.75 mm x  $80 \mu \text{m}$  and two typical SEM images of them are shown in Figs. 3(a) and (b). Note that in both samples, the silver particles (in white color) have a random spatial distribution within the resin matrix (in black color), and therefore their shape and volume fraction are expected to drive the thermal



conductivity of the sample composites.

Figure 1: Typical SEM images of the samples with (a) spherical and (b) flake-like micro-particles embedded in a resin matrix.

#### 3.2 Thermal conductivity measurements

The thermal conductivity of the samples was measured by the Lateral Thermal Interface Material Analysis (LaTIMA)[13]. The working principle of this novel technique consists in setting a constant thermal current along a free standing thin film to measure the heat flux and the temperature gradient along the sample through thermocouples and an IR camera, as shown in Fig. 4, respectively. The sample thermal conductivity  $k_s$  is then determined by using the Fourier's law, as follows

$$k_s = \frac{QL_{IR}}{A_s \Delta T_{IR}},\tag{4}$$

where  $\Delta T_{IR}$  is the temperature difference along the sample length  $L_{IR}$  probed by the infrared (IR) camera,  $A_s$  is the sample cross-section, and Q is the heat flux through the sample, which is recorded by the metal-based heat flux sensors, calibrated according to the standard D5470 of the American Society for Testing Materials (ASTM) [14].



Figure 4: Scheme of the experimental setup of the LaTIMA technique.

The experimental setup was designed to minimize possible artifacts related to the sample materials and their geometry, as well as to ensure a measurement accuracy better than  $\pm$ 5%. This minimization was achieved by performing the experiments in vacuum, to get rid of the heat losses by convection, and by coating the heat flux sensors with a low emissivity layer of gold or nickel, which reduces the radiation losses and therefore increase the accuracy of our thermal conductivity measurements. These sizeable reductions of heat losses by convection and radiation were also confirmed by finite element simulations, as detailed in the literature [14, 15].

#### 4 Results and discussions

The predictions of Eqs. (1a) and (1b) in comparison with the experimental thermal conductivity k of Ag/resin composites with microparticles and flakes are shown in Fig. 5(a) and 5(b), respectively. The expected increase of k with f is, within the error bars, well described by the theoretical model, for both Ag fillers. For a given volume fraction, spherical particles yield a higher thermal conductivity than the one given by flakes. This is reasonable, given that the heat flux within randomly oriented flakes is highly dispersed in many directions, which reduces the overall thermal performance of the corresponding composite.



Figure 5: Comparison of the experimental and theoretical thermal conductivities of composites with (a) microparticles and (b) flakes of silver embedded in a resin matrix.

#### 5 Conclusions

We have experimentally shown that the thermal conductivity of solid composites made up of spherical silver microparticles embedded in resin is comparatively higher than the one obtained with randomly oriented silver flakes, such that it takes the value of  $16 \text{ Wm}^{-1}\text{K}^{-1}$  for a 50% volume fraction of particles. The increase of the thermal conductivity with the particles concentration has been well described by a simple and analytical model, which takes into account the particle-particle interactions through a crowding factor, for both the spherical and flake-like particles.

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### DPL Thermal Model of Test Microchip Structure without Cavity Dedicated to Estimation of Nanoelectronic Circuits Thermal Properties

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#### Abstract

This paper presents the comparison of the temperature distribution in the test structure chip obtained using Fourier-Kirchhoff and Dual-Phase-Lag heat transfer models. The investigated test structure consisting of two polysilicon resistors used as the heater and thermometer, which are located inside the silicon dioxide layer. The simulation results are compared with those which have been received using similar test structure containing two platinum resistors. Some numerical problems observed during the simulation of Dual-Phase-Lag heat transfer model have been also briefly presented.

#### 1 Introduction

Nowadays, one of the most important research areas is the analysis of the thermal problems occuring in modern electronic Integrated Circuits (ICs). This situation is caused by the meaningful structure size shrinkage and influential increase of their operation frequency. Due to the fact that electronic devices are getting smaller, the density of generated heat inside such structures is increasing. This phenomenon, in turn, contributes to occurrence of inappropriate operation of electronic appliances or even their permanent damages. Therefore, the electro-thermal analyses have become the integral part of the process of designing, developing and manufacturing of modernly produced electronic structures. The mentioned analyses are particularly crucial because most of malfunctions of electronic devices are caused by thermal reasons [1].

For almost 200 year thermal problems had been solving using approach established by J.B.J. Fourier [1], [2]. It is based on the Fourier law and the Fourier-Kirchhoff equation which are presented in equations (1) and (2):

$$-q(x, y, t) = k \cdot \nabla T(x, y, t)$$
(1)

$$\frac{\partial}{\partial t} \left( c_p \rho T(x, y, t) \right) = -\nabla \cdot \vec{q}(x, y, t) + q_{gen}(x, y, t) \quad (2)$$

where T(x,y,t) means the temperature distribution inside investigated ICs, q(x,y,t) represents the heat flux and k denotes the value of the thermal conductance of analyzed material,  $q_{gen}(x,y,t)$  means the density of internal generated heat,  $c_p$  represents the specific heat capacity and  $\rho$  is the material density.

However, the use of the Fourier-Kirchhoff (F-K) equation is associated with several unrealistic assumptions [3], [4].

Moreover, the development of the manufacturing technology of modern semicondutors and extreme reducing of their size implicate some other problems with applicability of the F-K equation [4], [6], [7]. Due to this fact, the new approach to the modelling of the heat conduction in nanosized structures is required. One of the solutions was proposed by Tzou who has established the Dual-Phase-Lag (DPL) model [8], which is described in the next section of this paper.

#### 2 Methodology

In this paper, the DPL model is taken into considerations. This model is based on the classical F-K model. However, it contains some significant improvements in relation to the classical heat transfer model. The DPL model can described using the system of differential equation presented in (3):

$$\begin{cases} c_{v} \frac{\partial T(x, y, t)}{\partial t} = -\nabla q(x, y, t) \\ q_{gen}(x, y, t) + \tau_{q} \frac{\partial q(x, y, t)}{\partial t} = \\ = -k \nabla T(x, y, t) - k \tau_{T} \frac{\partial}{\partial t} \nabla T(x, y, t) \end{cases}$$
(3)

Two new constants  $\tau_T$  and  $\tau_q$ , which appear in the DPL model, are the temperature time lag and the heat flux time lag, respectively. Appearance of these two time lag constants explains the name of the investigated model. The DPL model is suitable for the parabolic F-K model as well as hyperbolic models. Moreover, it can be useful for modelling of heat conduction in nanosized electronic structures which will be analyzed in this paper.





Figure 1. The cross-sectional view of the vertical structure with the air chamber filling

In the Figure 2, the cross-sectional view of the investigated structure is presented. Using DPL model together with radiation model and material parameters of the investigated structure, the heat distribution will be yielded. The value of the parameter  $B = \tau_T/(2 \cdot \tau_q)$  for the silicon and the silicon dioxide, the platinum and the aluminium is assumed to 20, 36 and ca. 100, respectively [9]. The values of other material parameters are taken from the specialist literature presented in [10] and they are shown in Table 1. Moreover, the following DPL heat transfer equation is employed:

$$\frac{1}{\alpha} \cdot \frac{\partial T(x, y, t)}{\partial t} + \frac{\tau_{q}}{\alpha} \cdot \frac{\partial^{2} T(x, y, t)}{\partial t^{2}} =$$

$$= \Delta T(x, y, t) + \tau_{T} \cdot \frac{\partial \Delta T(x, y, t)}{\partial t} + q_{gen}$$
(4)

where the constant  $\alpha$  is the thermal diffusivity. It is assumend that the value of the heat density  $q_{gen}$  is equal to  $2 \cdot 10^{15} \text{ W/m}^2$ .

In further research, the structure consisting of three main layers. The bottom one is made of the silicon which thickness is 400 nm. The middle one is the 500 nm thick layer of silicon dioxide or silicon nitride. The top part is the passivation layer made of silicon dioxide. Between two lower layers the aluminium heater is placed. Its thickness is 30 nm. Inside the structure the cavity of the 5  $\mu$ m length filled with the air is located. Over the cavity, in the top layer, the platinum nanothermometer is put. Described structure is presented in Figure 1.

#### **3** Simulation Results

The thermal simulation has been carried out based on the assumed material parameters of investigated structure for the polysilicon resistors which thicknesses are equal to 50 nm. The temperature distribution was modelled using both the Fourier-Kirchhoff and the Dual-Phase-Lag models in Mathematica ver. 11 environment. Moreover, the results have been obtained using Finite Element Methods for 3528 triangles and the mass matrix method for the reformulation of the equation.

Figure 2. The cross-sectional view of the nanosized horizontal structure consisting of polysilicon resistors

The temperature distribution around the polysilicon resistors (in regions where the heat is generated and where the thermometer is placed) obtained using F-K and DPL models for 10 µs are presented in Figure 3. As it can be seen, the temperature distribution obtained using both models has the similar behaviour, however temperature rises in F-K model are significantly greater than in the case of the DPL model. On the other hand, the average temperature rise in the heat generation region and in the place, where the thermometer is located, is presented in Figure 4. Unfortunately, in spite of the correct determination of the temperature distribution presented in Figure 3, the convergence of the received results for DPL numerical model seems to be insufficient, what is shown in Figure 4, case b. The obtained results, which are demonstrated in Figure 4, case b and in Figure 5, case b, are quite similar to the previous one yielded in [11] for platinum (Pt) resistors (see Figure 2) and presented in Figure 5, case a.

The undertaken consideration shows that DPL model is numerically ill-conditioned for FEM as well as FDM methods. Therefore, the solution should be confirmed using another approach. For this purpose, the Multiresolution Battle-Lemarie as well as cylindrical wavelets approximation will be used. The final results will be presented during the Therminic 2016 conference.

Table 1 MATERIAL PROPERTIES OF INVESTIGATED STRUCTURE

	Material			
Material properties	Silicon Si	Platinum Pt	Silicon dioxide SiO2	Silicon nitride Si <sub>3</sub> N4
Density ρ [kg/m <sup>3</sup> ]	2330	21450	2220	2400
Specific heat c <sub>p</sub> [J/(kg·K)]	712	133	745	691
Thermal conductivity k [W/(m·K)]	148	71.6	1.38	16
Thermal diffusivity $\alpha \cdot 10^6 \text{ [m^2/s]}$	89.2	25.1	0.834	9.65



Figure 3. The final steady state solution for F-K model and DPL model;  $t=10 \ \mu s$ ,  $q_{gen}=2 \cdot 10^{15} \ W/m^2$ , poly-Si resistors, thickness 50 nm



Figure 4. The average temperature rises in heat generation and thermometer regions obtained for F-K and DPL models;  $t=0-10 \ \mu s, \ q_{gen}=2\cdot 10^{15} \ W/m^2$ , poly-Si resistors, thickness 50 nm







Figure 5 The comparison of the temperature rise in the heat source and in the thermometer obtained using both the F-K and the DPL models for a) Pt resistors, thickness 30 nm,  $q_{gen}=1.10^{15}$  W/m<sup>2</sup> and b) poly-Si resistors, thickness 50nm,  $q_{gen}=2.10^{15}$  W/m<sup>2</sup>

#### 4 Conclusions

This paper demonstrates the application of F-K and DPL thermal model for real testing structure. The considerations presented in this paper are the first step in the modern chip designing process. The obtained results will allow carrying out the experiment which will revalidate the applicability of DPL model to nanoelectronics and air chamber as well as the estimation of the thermal parameters of materials in the investigated nanoelectronic structures.

Unfortunately, the convergence of FEM approximation for DPL model is not sufficient, therefore the Multiresolution Battle-Lemarie as well as cylindrical wavelets approximation will be used in further investigations.

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**SESSION 7** 

# **SESSION 7** Power Electronics 2: Testing

### **Extracting Structure Functions of Power Devices in Induction Motor Drives**

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#### Abstract

This paper proposes the extraction of structure function from power devices on-board induction motor drives. It puts forward the issues and methodology related to on-board measurement of the cooling curve and derivation of the structure function during idle times in induction motor drives for maintenance purposes. The structure function uses the thermal resistances and capacitances in the Cauer form to identify changes in the device structure. The advantage of the structure function is that it does not only reveal the value but also the location of the thermal resistance and capacitance in the heat flow path. The novelty in this work is the methodology used to achieve the measurement of the cooling curve and the derivation of the structure function despite issues related to freewheeling current due to energy stored as a result of motor inductance.

#### 1 Introduction

Power Semiconductors are central to a number of key societal infrastructures. They are the basic building blocks of power (electrical) conversion applications. From Figure 1, the various silicon based semiconductor devices can be observed to be used for a wide range of power levels. Also the various possible applications for the semiconductor devices have been illustrated. Most of these applications are integral to daily life. In fact, according to [1], electric motors and the systems they drive are the single largest electrical end-use, consuming more than twice as much as lighting, the next largest end-use. It is estimated that electric motor driven systems account for between 43% and 46% of all global electricity consumption. Over 90 % of this is represented by induction motors. About 25-30% of induction motor drives are driven by power switched converters. This number is growing in motor drive applications, automotive, renewable and other applications.



Figure 1: Power Semiconductor Devices and Applications[2]

Power converters that use insulated gate bipolar transistors (IGBT) modules are becoming more common in automotive, rail-traction, aerospace, renewable energy and several other applications where the combination of environmental and load-derived thermal cycling can result in large and unpredictable fluctuations in junction temperature [3]. The power module is made up of different

layers and several materials. This is designed to provide mechanical stability, electrical insulation and thermal conductivity[4]. The conventional power module is usually made up of eight layers as seen in Figure 2. The numbers indicate the different layers and the colors are indicative of the materials used. Table 1 enumerates some of the different materials used and the coefficients (CTE) of thermal expansion. The CTE indicates change of a component's size with a change in temperature.



Figure 2: Conventional Power Module Cross Section

*Table 1: Power Module Materials and CTE* 

Material	CTE ppm/°C
Aluminium	~22
Silicon (Die)	~3
Ceramic (Al <sub>2</sub> O <sub>3</sub> )	~7
Copper (Cu)	~17

The different values of CTE will make the different materials expand and contract at different rates which will lead to mechanical stresses resulting in various failure mechanisms, such as wire-bond lift off and cracking, solder delamination and aluminium reconstruction [4]. Wire-bond lift off and solder delamination are shown in Figure 3. The failure mechanisms need to be detected in order to prevent abrupt destruction of the devices. Therefore to detect the impending failure, cursor/cursors of detecting the failure mechanisms need to be defined. Some parameters related the device or device structure will be related to the failure mechanisms. The thermal response function (cooling or heating curve) as a result of power step excitation contains information of structure of the device. Hence by measuring the thermal response function a change in the structure can be detected. The junction temperature then is an important parameter to monitor degradation; the power modules are enclosed and provide no opportunity for a direct measurement of the junction temperature.



Figure 3: Failure mechanisms (a) wire-bond lift-off (b) solder delamination[5]

A common method to detect the temperature in enclosed devices with no direct contact is with temperature sensitive electric parameter (TSEP). TSEPs are electrical parameters like collector-emitter voltage ( $V_{ce}$ ) [6-9] which have a mathematical relationship to temperature.  $V_{ce}$  is chosen in this work based on the fact that the aim is to measure the dynamic temperature of the device. Therefore a continuous measurement of the temperature is needed. This eliminates the use of the threshold voltage, turn-off time as regular switching is needed in order to obtain the temperature. The  $V_{ce}$  as presented in [10], exhibits the favourable characteristics such as a high repeatability, linearity.

#### **1.1 Measuring Thermal Transients**

The basic concept for measuring the cooling temperature curve by using temperature sensitive electrical parameters is shown in Figure 4(a). A high current (red) is passed through the device under test to heat up the device using a high current source; the temperature profile (blue) of the device heating and cooling can be observed. A basic set-up to obtain the aforementioned temperature profile can be seen in Figure 4 (b). A control switch is placed in the high current path to turn on and off the high current during heating and measurement respectively. The device under test (DUT) is left on, so during the measurement the low current passes through the DUT to create a voltage drop proportional to temperature. The relationship between the voltage and temperature is obtained from the device calibration. The calibration process is carried out by heating the device to a certain temperature and applying the low current (measurement current) and measuring the corresponding voltage. By measuring at different temperatures a relationship between the temperature and the voltage can be established.

The aim of this paper is to present the challenges and methodology used to extract the cooling curve and derive the structure function (from cooling curve) of the power devices in a 2-level 3-phase inverter as seen in Figure 5 without dismounting or changing the connections [8]. As seen from the basic measurement in Figure 4(b) a current source is provided in order to heat up the DUT. However in the inverter setup, the current (constant) has to be taken from the DC voltage supply without exceeding the current ratings of the devices.



Figure 4: (a) Junction Temperature & Heating Current Pulse (b) Basic Concept of Junction Temperature Measurement Using vce



Figure 5: 2- Level 3-Phase Inverter with an Induction Motor Load

As opposed to the real-time monitoring solutions, which take measurements of the TSEP of the device during operation of the inverter, in the methodology proposed here, measurements are taken when the system is not operation in order to measure the cooling curve. In [11, 12] real-time monitoring is presented, which compares physical measurement with a model estimate to accurately track the junction temperature of the device under consideration. The limitations of this method are that the collector emitter voltage is noisy and intermittent due to the non-linearity of the I-V characteristic of the IGBT, low temperature sensitivity and the variable phase current in an inverter. A quasi real-time method was also proposed in [13] which uses the RMS collector emitter voltage and current to detect fault just before start in vehicles.

The in-situ method in [14] works by injecting external currents into the power unit during idle times. Both high currents (heating) and low currents (measuring) are injected externally. Moreover, in [14] a set of relays need to be inserted to select which device undergoes test, with severe limitation of the applicability of such solution and considerable complication of the testing methodology. The method [15], mainly made reference to in this work introduces the use of vector control to heat up the power devices making use of the DC voltage supply as opposed to [14] which uses external high current source. An original approach in this paper is extraction of structure function (onboard) which can be carried out between operational phases of the equipment, such as in trains once a week/month in the depot for maintenance routines.

#### 2 Structure Function

The structure function uses the thermal resistances and capacitances in the cauer form (because Cauer networks have a link with the physical structure) to identify changes in the devices structure. The structure functions are obtained by direct mathematical transformations from the heating or cooling curves [16]. These curves may be obtained either from measurements or from the simulations of the detailed structural model of the heat flow path. In both cases a unit step function powering has be applied on the structure, and the resulting increase (or decrease, in case of switching off) in the temperature at the same location has to be measured in time, following the switching on[17].

The advantage of the structure function is that it does not only reveal the value but also the location of the thermal resistance and capacitance in the heat flow path. There are two types of structure function, differential and cumulative. The cumulative structure function is also known as the Protonotarios-Wing function[18]. This is a function that presents a graphical representation of the structure of the device by using the thermal capacitance and thermal resistance. The cumulative structure function is sum of the thermal capacitances  $C\Sigma$  (cumulative thermal capacitance) in the function of the sum of the thermal resistances  $R\Sigma$ (cumulative thermal resistance) of the thermal system, measured from the point of excitation towards the ambient. In [17], the differential structure function is defined as the derivative of the cumulative thermal capacitance with respect to the cumulative thermal resistance, by

$$K(R_{\Sigma}) = \frac{d C_{\Sigma}}{d R_{\Sigma}} \tag{1}$$

From Figure 6, considering a dx wide slice of a single matter of cross section A, we can calculate this value. Since for this case  $dC\Sigma = cAdx$ , and the resistance is  $dR\Sigma = dx/\lambda A$ , where c is the volumetric heat capacitance,  $\lambda$  is the thermal conductivity and A is the cross sectional area of the heat flow, the K value of the differential structure function is



Figure 6: One Dimensional Heat Flow Model

$$K(R_{\Sigma}) = \frac{cAdx}{\frac{dx}{\lambda A}} = c\lambda A^2$$
(2)

This value is proportional to the *c* and  $\lambda$  material parameters, and to the square of the cross sectional area of the heat flow, consequently it is related to the structure of the system. In other words: this function provides a map of the square of the heat-flow cross section area as a function of the cumulative resistance. The differential function is shown in Figure 7, the local peaks indicate reaching new surfaces (materials) in the heat flow path, and their distance on the horizontal axis gives the partial thermal resistances between these surfaces. More precisely the peaks point usually to the middle of any new region where both the areas, perpendicular to the heat flow and the material are uniform



Figure 7: Differential Structure Function

#### 3 Extracting Structure Function On-Board

One of the challenges of extracting the structure function from the inverter is heating the devices with constant current. A control technique called vector control is introduced to heat up the devices and at the same time keeps the induction motor stationary, as test is to be carried out during maintenance routines. Vector control is used because it provides the opportunity to control the torque current ( $I_{sq}$ ) and field current  $I_{sd}$  which analogous to the armature current and the field current in DC motors respectively. By making the torque current ( $I_{sq}$ ) 0 and giving the required current as the field ( $I_{sd}$ ) reference, current flows in the devices hence heating the devices up without moving the rotor. These conditions make it suitable for maintenance routine. The details of this process are presented in [15]. The resulting phase currents during heating can be seen in Figure 8. From the phase currents it is evident that the motor will be stationary due to absence of rotating fields.



Figure 8: Three Phase Currents During Heating

The next step after heating is measuring the  $V_{ce}$ , which has to be carried out on the inverter in the presence of high voltages. The measurement circuitry is based on the work in [6]. Two diodes D1 and D2 shown in Figure 9 are connected in series and a current source forward-biases them during the IGBT on time. When the IGBT is off, the D1 diode is blocking the  $V_{ce}$  voltage, protecting the measurement circuitry from damage. Assuming the two diodes are identical ( $V_{D1} = V_{D2}$ ), the  $V_{ce}$  voltage may be measured by subtracting the voltage drop on diode D2 from the  $V_b$ potential. This mathematical function can be realized using the circuit shown in Figure 9.



Figure 9:Schematic of measurement circuit [6]

The circuit in Figure 9 makes it possible to implement the equation above. The first op-amp (highlighted in red) does the mathematical function of producing  $2V_b$  in (3). The second part (highlighted in green) of the circuit completes the mathematic function using a differential amplifier to obtain  $V_{ce}$  ( $2V_b$ - $V_a$ ). Extra stages have been added to the measurement circuit, such as conditioning the signal to utilize the full range of the FPGA and increase resolution. An isolation stage has also been added to protect the control board. The measurement circuit and the isolation can be seen in Figure 10.

The measurement is carried out by passing the low current used to calibrate the device. This is carried out by switching on only S1 in Figure 5 and switching off S2-S6, in order to prevent high current paths. Due to the energy stored in the motor inductance current free wheels through the device switched on for measurement and the top 2 diodes in the 2 other phases as shown in Figure 11. This means that the low current measurement cannot be carried out during the free-wheeling period due to high current flowing in the device. A voltage (collector-emitter) and current measurement of the device was carried out at this stage and it can be seen in Figure 12 that the current decays slowly.



Figure 10: Measurement Circuit and Isolation Board



Figure 11: Inverter during Measurement Phase



Figure 12: Current and Voltage (collector-emitter) of DUT

The magnetising inductance of the motor is considerable; it takes time for the current to decay to the measurement current used for calibration. This means that by this time, a lot of information is lost in the cooling curve which means information on the structure of the device is lost. From Figure 12, it can be observed that it takes 0.793s for the current to reach the level of the measurement current. If the measurement is to start at 0.793s most information of the structure of the device solder and substrate faster time constants. The data sheet gives information about the junction to case thermal resistance of the device (Magna Chip MPMB75B120RH) which is typically 0.2 °C/W. By matching this information to the derived normalized temperature (divided by the power dissipation) shown in Figure 13. The approximate time

constant from the junction to the case can be obtained. In this case the obtained time constant from the graph is 0.2512s. This means that any measurement that starts past this time constant is measuring the heat sink. Therefore any degradation present in the device will not be recorded



Figure 13: Normalized Temperature Curve

To solve this problem, the methodology will be outlined. Since the current stored in the inductor flows through the device and the voltage is always measured. The collector current against the collector emitter voltage (I-V curves) at different temperatures can be used to measure the temperature by creating a look-up table. In Figure 14, the maroon line is the measured voltage and current passing through the device. However this curve passes through a point on the IV curves where there is no difference in voltage and current for all the temperatures. This means that it is impossible to measure at this point (Inflexion Point). But above the and below this point the sensitivity (to noise) gradually decreases. The highlighted area in Figure 14 below the Inflexion point has a lower sensitivity (to noise) of about 2mV/°C and the highlighted area above this region has a higher sensitivity(to noise) of 0.9mV/°C This methodology exploits the point below the inflexion point. One of the reasons for this is that the region has a lower sensitivity (to noise) and also it is known that there is negligible self-heating in this region as the current is low.



Figure 14: I-V Curves and Measured Device current and Voltage

#### 4 Results

The methodology is to use the controller (vector control) used to heat the devices to force the current to a low value so that the region in the IV curves will be of a low sensitivity. It can be seen in Figure 15 that the reference changes from 7A to a low value (0.2 amps in this case). The current changes faster (from 7Amps to 0.2 A in 2ms) than in the previous case. This means that the self-heating is negligible, faster time constants will be recorded. In this case the measurement starts when the current falls below 1A. As it can be seen from figure 6, the sensitivity(to noise) of the IV curves reduces as the current approaches zero therefore less error in the measurement.



*Figure 15: Current and Voltage During Measurement Using Vector Control.* 

The Junction Temperature measurements taken in this case are shown in Figure 16. An averaging technique was used to derive the two averaged curves (Blue and Orange). The two curves are presented here to show that this process is repeatable. This is important because the process is carried out to check for degradation in power modules; making sure changes are due to degradation not measurement. The differential structure function of the temperature curves can be seen Figure 17 also showing repeatability.



Figure 16: Junction Temperature Curves



Figure 17: Differential Structure Function

#### 5 Conclusion

This work has shown a method of extracting the junction temperature and structure function of power modules for health monitoring purposes. It introduces the use current controller to measure junction temperature. It also shows how to avoid the stored energy in the induction motor that disrupts temperature measurement. Experimental results of junction temperature and the structure function have been provided. The system is carried without additional components or changes to the inverter system except the analog measurement circuitry. Future work will entail cycling of devices to induce degradation so the difference can be identified by a measurement carried out at time 0 using the structure function.

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### **Characterization of Thermal Interface Materials for IGBT Inverter Applications**

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#### Abstract

Power electronics applications require an accurate thermal management design. In this sense, one of the most important elements are thermal interface materials (TIMs) placed between the power devices and heatsinks in order to provide good thermal contact and (eventually) electrical isolation. To predict accurate thermal performances of the final assemblies, direct thermal tests are practically unavoidable, as the final thermal behaviour of TIMs depends on many parameters, such as mounting pressure, surface roughness, etc. and datasheets are often incomplete. Such thermal tests could be complex in final industrial systems and for this reason we propose a simple TIM evaluation setup for predicting the final thermal behaviour of IGBT-based inverters using such materials. The results obtained from two thermal pad TIMs and silicone grease are compared showing a good agreement with those obtained in test vehicles using functional IGBTs.

#### 1 Introduction

Power electronics applications require an accurate thermal management design process. Inside the power converter circuits, power semiconductor devices switch high voltage and current values and generate considerable conduction and switching losses that must be dissipated to the ambient or cooling fluid. A suitable heat extraction path between the semiconductor dice and such ambient is required in order to keep the device temperatures below their maximum allowed values under nominal operation conditions. In this scenario, one of the most important elements of the cooling path is the thermal interface material (TIM) placed between the power devices (either, in discrete or module package form) and heatsinks [1] [2] [3]. Their main role is to improve the thermal interface contact between the device package and the heatsink, although very often they must also provide electrical isolation between both elements. In order to predict accurate thermal performances of final IGBT + TIM + heat sink assemblies, direct thermal tests are practically unavoidable, as the final thermal behaviour of TIMs depends on many parameters, such as mounting pressure, surface roughness, etc. In addition, thermal parameters provided in datasheets are sometimes incomplete and obtained in conditions away from the application. Such thermal tests could be complex in final industrial systems such as the full-bridge inverter considered in this work (see Figure 1). For example, the cross heating effects between neighbour devices difficult to interpret the correct contribution of the TIM layer, temperature measurements can be also hindered by the final converter topology and the application of suitable electrical test signals could be incompatible with the final control circuitry. For this reasons we have investigated a simple TIM evaluation setup allowing the estimation of the final thermal behaviour of IGBT-based inverters using different materials.

The main objective of this work is to validate the suitability of the proposed off-site thermal evaluation setup. Consequently, Section 2 describes this setup and the results obtained for three different TIMs. As the main interest of the study focuses on the assessment of "gap-pad" TIM solutions, in order to avoid the complexity related with the extraction of absolute thermal parameters [4] such as thermal conductivity or contact resistances (influenced by the contribution of surface roughness, ambient conditions, etc.) the analysis has been raised in comparison with a silicone grease (the best analysed solution). Section 3 describes the test vehicles developed with functional IGBTs and the thermal impedance extraction method used for them. This parameter clearly shows the influence of each TIM on the power devices in a very similar environment than in the final converters. The agreement between both evaluation methods is also analysed.



Figure 1: Picture of the inverter showing 4 RC-IGBTs fixed to the heat sink with a TIM film. On the left side, a bridge rectifier is also fixed with silicone grease used as TIM.

#### 2 Direct Characterization of TIM materials

This work was mainly addressed to characterize TIMs in thin film format (also known as "gap pads" or "thermal pads") because in the considered full-bridge inverter application, electrical isolation between the TO-247 package of the IGBTs and the heat sink is mandatory (see Figure 1). Such TIMs are based on elastomer-like materials reinforced with a carrier fabric (typically fiberglass) although their precise composition is usually unknown for final users. In particular, two TIMs of different cost range and nominal performances (denoted as TIM1 and TIM2) have been characterized. Nevertheless, the typical silicone grease solution (denoted as SG) has been also considered for two reasons: silicone grease is used in a rectifier bridge of the converter where electrical isolation is not required (see Figure 1) and silicone grease provides the best thermal contact among the available TIMs, becoming a reference material for comparison purposes. The silicone grease used in our study is based on silicone oil with a suspension of metallic oxide particles of unknown size. As the main interest of the study focuses on the assessment of "gap pad" solutions, the analysis has been raised in terms of determining the thermal resistance ratios respect to the silicone grease, avoiding the problems related with the extraction of absolute thermal parameters such as thermal conductivity (strongly influenced by the contribution of the test conditions, material composition, etc.). Table 1 summarizes the main nominal (datasheet) parameters for the 3 analyzed TIMs. As it can be observed, direct comparison of different technologies such as thermal pads and greases from datasheets is difficult (provided parameters are not the same, different test conditions, etc.). It is also interesting to observe that although TIM1 is thinner than TIM2 it provides higher thermal resistance values for a TO-220 package. This fact is explained by the higher thermal conductivity of TIM2 but probably also by a better gap filling behavior and optimized reinforcement carrier fabric.

	Nominal Parameters			
Material Thickness (µm)	Thermal conductivity	Breakdown voltage	<i>R<sub>TH</sub></i> for TO- 220 @ 1.4MPa	
	(µm)	(W/m.K)	(Vac)	(K/W)
TIM1	125	1.6	1700	1.74
TIM2	200	1.8	3000	1.46
SG	-	0.65	-	-

Table 1: Nominal (datasheet) values for the analyzed TIMs

In order to analyze the thermal behavior of the given TIMs, we have used a setup developed some years ago for the thermal conductivity extraction of power substrate materials [5] [6]. Figure 2.a shows a schematic view of the main mechanical elements while Figure 2.b shows a picture of the whole setup. It consists of a heat source (a MOSFET power transistor) that injects a given heat flux to the TIM sample under test (cut in 15 mm x 20 mm pieces) through a Cu heat spreader. The dissipated power P is regulated with a specific closed-loop controller [7]. The heating element, the spreader and the material under test are fixed with a clamping system consisting on two vertical rods, a transversal clamping beam (made of insulating material) and two nuts for tightening the assembly. All these elements are placed in a vacuum enclosure to avoid convection. Two precision Pt temperature

sensors measure the temperature at two points: in the middle of the heat spreader ( $T_S$ ) and on the heat-sink surface where the TIM sample is placed ( $T_{HS}$ ). The mounting pressure can be controlled with a dynamometric wrench when tightening the top nuts (see Figure 2.a). The characterization system is completed with a Keithley 2420 power supply and with a Keithley 2700 for temperature measurement.

A thermal resistance  $R_{TH}$  associated with each TIM material is evaluated as:

$$R_{TH} = \frac{T_s - T_{HS}}{P} \tag{1}$$

This thermal resistance includes the contribution of the TIM, the interfaces TIM/spreader and TIM/heatsink and a fraction of these two elements (spreader and heat sink). As the TIM evaluation process will be performed in comparison with silicone grease, for each test the setup will be kept unchanged except for the material under test and, consequently, the measured  $R_{TH}$  will reflect mainly the TIM contribution.

One of the critical aspects of the described characterization process is that the thermal response of the TIM depends on the pressure applied when assembling it  $(P_S)$  [8]. Consequently, this parameter must be known when performing the tests.



Figure 2: a) Scheme of the test setup showing its main mechanical elements. b) Picture of the complete test setup, including the electrical equipment.

The pressure is computed as the force applied by the clamping system, F, divided by the TIM area, being the total force two times the force applied by one of the fixing nuts

(see Figure 2.a). Consequently, the mounting pressure can be computed as:

$$P_{S} = \frac{N}{COF \times D \times A} T_{q} \tag{2}$$

Where N is the number of fixing nuts (2 in our case),  $T_q$  is the mounting torque applied to the nuts, D is the diameter of the rods (6 mm in our case), A is the TIM area in contact with the spreader and the heat sink (15 mm x 20 mm in all our study) and COF is the coefficient of friction, a parameter depending on the nut and screw characteristics (materials, lubrication, etc.). This parameter has a strong influence on the final force applied by the nuts for a given torque, as it can be observed in the curves of Figure 3, computed for three typical COF values in the range between 0.18 and 0.36. For determining the appropriate value in our system, a test was performed replacing the TIM under test by a compression load cell (FC23 from Measurement Specialties). This experiment allowed a direct measurement of the force applied by the clamping system for a given torque and from this data a COF of 0.22 was determined. It is worth pointing out that the influence of lubricating oil between nut and rod was also analyzed and its effect can be neglected in our setup.



Figure 3: Computed curves showing the pressure exerted by the clamping system as a function of the mounting torque for three different COF values.

For obtaining the experimental  $R_{TH}$  values, a given constant power is applied in the previous setup (approximately 48 W) and the data for applying expression (1) is taken only when complete stabilization (steady state) is reached (in the range of 1 to 2 hours). The pressure applied during the tests is computed from expression (2). The results obtained for the 3 tested materials in the pressure range from 0.75 to 4.25 MPa are shown in Figure 4. It is worth pointing out that, according to expression (2), the pressure exerted by a TO-247 package fixed with a M3 screw at a typical mounting torque of 0.75 NM is around 4 MPa and, consequently, following the described methodology the TIMs are characterized under real operating conditions. The plots in Figure 4 show not only that TIM1 presents a higher thermal resistance than TIM2 in all the pressure range (as expected from the last column in Table 1), but that the  $R_{TH}$  dependence with pressure is also higher for TIM1 (33% variation in front of 7% in the analysed pressure range). This information is relevant as it allows predicting, for example, eventual IGBT overheating due to abnormal lower mounting torques during the fabrication process. Silicone grease provides by far the best thermal interface, but without electrical isolation and the variation of its  $R_{TH}$  value with pressure is even lower than for TIM2.



Figure 4: Thermal resistance values measured off-site with the proposed setup for the 3 analyzed TIMs, as a function of typical mounting pressures (0.75 to 4.25 MPa).

#### **3** Evaluation of TIM materials in test vehicles

In parallel with the off-site thermal characterization of the TIMs, the test vehicles depicted in Figure 5.a were developed for evaluating the thermal response associated with the IGBTs and their corresponding TIMs. The thermal impedance from device junction to baseplate ( $Z_{TH(j-REF)}$ ) of these test vehicles describes the conduction phenomena present in the inverter with the IGBTs assembled on the heatsink. As the devices used in our tests are in fact RC-IGBTs, only a Si die is found inside the package as the IGBT and the freewheeling diode are monolithically integrated. The IGBT packages (TO-247) are screwed into a 3 mm thick Cu baseplate with M3 screws, the recommended (datasheet) mounting torque (0.75 Nm) and the TIM material placed between them.

For measuring their thermal impedance, the test vehicles are assembled in the heatsink of a specific test setup already used for this kind of tests [9]. The forward voltage drop of the freewheeling diode is used as a thermo-sensitive parameter (TSP) for  $T_j$  estimation and a reference temperature ( $T_{REF}$ ) is directly measured on the baseplate backside with a spring-loaded K-type thermocouple (see Figure 5.a. The transient cooling curves are recorded after a long (steady state) heating period where the freewheeling diode dissipates a constant power in the range of 14 to 20 W. In particular,  $T_{REF}$  is directly measured from an instrumentation amplifier and  $T_j$  is derived from the forward voltage drop of the freewheel diode,  $V_F$ , biased at a low current level ( $I_M = 10$  mA). A previous calibration of the forward voltage drop at 10 mA with temperature is also used in this process. The circuit shown in Figure 5.b implements the described measurement approach. Defining the junction and reference temperature variations ( $\Delta T_j$  and  $\Delta T_{REF}$ respectively) as the variation of such variables respect their initial values during the cooling process, the junction to reference (baseplate backside) thermal impedance is finally computed as:

$$Z_{TH(j-REF)} = \frac{\Delta T_j - \Delta T_{REF}}{P}$$
(3)



Figure 5: a) Schematic drawing of the developed test vehicles including the RC-IGBT package, the TIM and a baseplate. b) Schematic of the circuitry used for evaluating the thermal impedance of the test vehicles.

Figure 6 shows the thermal impedances obtained for the three analysed TIMs. As it can be observed, the device heating is practically the same for heating times up to 0.1 s. From this point, the influence of the TIM layer becomes relevant, although the curves for TIM1 and TIM2 are practically the same up to 0.5 s and then, diverge. The thermal resistances of the test vehicles, derived from the thermal impedance values at 100 s, show again that the best thermal behaviour is found for the silicone grease (lower  $R_{TH}$ ) while the higher  $R_{TH}$  corresponds to TIM1. Table 2 summarises the thermal resistance ratios found among the different TIMs for both measurement approaches proposed in this work: off-site direct TIM characterization ("Direct test") and test vehicle characterization with a functional IGBT device (" $Z_{TH}$  test"). The results are in a reasonable good agreement for the purposes of this study: comparison and selection of TIMs. The deviations observed between both test methods are probably associated to slightly

different surface roughness of the involved elements but also due to the errors for applying a precise pressure in the " $Z_{TH}$  test" case.

Table 2: Experimental thermal resistance relationships among the different TIM-based solutions derived from Direct Tests) and from test-vehicles  $Z_{TH}$  tests.

R <sub>TH</sub> ratios	$Z_{TH}$ test	Direct test
TIM1/SG	2.2	2.8
TIM2/SG	1.8	1.87
TIM1/TIM2	1.24	1.5



*Figure 6: Thermal impedance curves of test vehicles for the 3 analyzed TIMs. IGBTs screwed at 0.75 Nm (4.1 MPa).* 

In this sense, Figure 7 shows the thermal impedances measured for the TIM1 test vehicle at different mounting torques, i.e., at different pressures. The effect of the increasing pressure can be clearly appreciated in all the measurement range but the two central curves for 4.1 and 5.4 MPa overlap, indicating a wrong estimated pressure in one of these two tests.



Figure 7: Thermal impedance curves of the test vehicle with TIM1 assembled at 4 different pressures (from top to bottom: 2.7 - 4.1 - 5.4 - 8.1 MPa).

#### 4 Conclusions

Thermal evaluation, comparison and selection of TIM materials for power converter applications must be often performed by direct measurement as datasheet parameters are not always complete and elaborated under the same conditions. Nevertheless, thermal tests in final converter circuits could be difficult to implement. In this work we have proposed a simple direct measurement method for TIMs, under the same conditions found in practical power converters. The results obtained with this approach are in good agreement with those performed on test vehicles including functional discrete IGBT devices in TO-247 package. These test vehicles are representative of the real operation conditions of the power devices in real full-bridge converters. The results confirm that the proposed simple direct test method allows predicting the behavior of a TIM in a final application, in terms of thermal resistance increase or decrease from another known material. Present works are addressed to improve the accuracy of the method and to validate the estimation of the pressure influence on the TIM's thermal response.

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### Difficulties in characterizing transient thermal resistance of SiC MOSFETs

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#### Abstract

Thermal design is important for safety and reliable operation of power electronics system to cope with emerging loss accompanied by power conversion operation. This paper point outs the difficulties in evaluating transient thermal resistance of power module with SiC MOSFET. The static mode thermal test method to extract structure function of power device utilises K factor of power device to estimate junction temperature. The knee voltage of body diode and threshold gate voltage are utilized as K factor for MOSFET. The estimated junction temperature of SiC MOSFET through the use of K factor gives inappropriate temperature behaviour especially at the onset of thermal test measurement. The anomalous results are observed for different measurement setup type for MOSFET. The dynamic instability of threshold gate voltage occurring in SiC MOSFET violates the estimation of junction temperature with K factor. The larger temperature variation for measurement is effective in mitigating temperature estimation error.

#### 1 Introduction

Power electronics is the key technology to achieve energy saving and renewable energy utilization, whose application is emanating significantly [1]. The less power conversion loss, reduction of size and weight for power electronics system is required. But, the performance improvement of power conversion circuit with conventional Si power device have been approaching the limit. The loss reduction requires low conduction and switching loss in power device, and the miniaturization and weight saving of power conversion circuit requires higher density integration of components and higher temperature operation with smaller heat sink. Then, novel wide band gap semiconductor device, which has superior material property than conventional Si, e.g. SiC and GaN, is expected to break through the performance limit of power electronics system especially high voltage and high power application [2]. The electrical design and thermal design of power conversion circuit must be considered simultaneously to realize the function and to secure the reliability of the system. The thermal design targets on high level realization of balancing heat generation in circuit operation and heat dissipation by cooling. To this end, precise modelling and evaluation of thermal characteristics for component in the circuit is necessary. The characterization of thermal behaviour is especially important for highly integrated SiC power module, whose heat density results in significantly high. The thermal resistance of power module represents the thermal characteristics. There are two methods to evaluate transient thermal resistance of a packaged power device, and the static mode thermal test method is standardized as JEDEC JESD51-1 [3]. This method utilizes K factor of power device as temperature sensitive parameter to estimate junction temperature in transient condition. This paper studies junction temperature estimation for SiC power device with their K factor. SiC MOSFET are evaluated as the power device. The influence of instability in threshold gate

voltage of SiC MOSFET on junction temperature estimation is especially investigated for static mode thermal test measurement.

# 2 Measurement setup types of thermal test in static mode method for MOSFET

The thermal response of SiC MOSFET is evaluated in static mode. The studied power MOSFET has vertical structure, then it has intrinsic body diode. There are two junction temperature estimation methods in static mode thermal test for MOSFET. The one method is to use gate voltage as the temperature sensitive parameter to estimate junction temperature, which is slightly higher than threshold gate voltage to flow sense current in saturation region operation. The other method is to use knee voltage of body diode as the temperature sensitive parameter to estimate junction temperature. MOSFET can flow current in bi-direction. Then, the measurement current direction is also used as a parameter. SiC MOSFET has difficulties of threshold gate voltage fluctuation for the applied gate bias voltage [4] and deterioration of forward voltage drop of body diode by conduction current [5]. Then, this paper evaluates the influence of characteristics change in SiC MOSFET on junction temperature estimation for following 4 measurement setup types.

### 2.1 Type 1: Vgs (Vds) measurement for forward channel conduction current (GD short)

The gate and drain terminal is directly connected as shown in Fig. 1(a), which results in Vgs=Vds. The power supply flows current in forward direction. The voltage drop across gate and source flows drain current in saturation region, which becomes high for large heating current. The gate-source voltage is measured to estimate junction temperature in cooling mode with flowing small forward current. The gate-source voltage results in slightly higher than threshold gate voltage.

# 2.2 Type 2: Vds measurement for body diode conduction current (GD short)

The gate and drain terminal are directly connected as shown in Fig. 1(b), which is same as type 1 measurement. This results in Vgs=Vds. The power supply forces current in reverse direction. The forward voltage drop by reverse conduction current induces negative Vgs, then the MOSFET channel opens. The current flows through body diode. The knee voltage of body diode in SiC MOSFET is higher than Si MOSFET. Then, the channel of SiC MOSFET is steadily opened. Also, the expanded depletion region under gate electrode by negative Vgs expands depletion region and may influence on conduction characteristics of body diode.

# 2.3 Type 3: Vds measurement for body diode conduction current (GS short)

The gate and source terminal are directly connected as shown in Fig. 1(c). This results in Vgs=0, and the MOSFET channel is open. The current is forced in reverse direction and it flows through body diode. The voltage drop by conduction current does not influence on Vgs. Therefore, the influence of electrical state change from heating operation to cooling operation expected to be small on the MOS gate condition.

# 2.4 Type 4: Vds measurement for body diode conduction current (forced negative gate bias)

The series connected voltage source between gate and source terminal applies negative gate bias voltage as shown in Fig.1(d). This results in Vgs<0. Then, the MOSFET channel is open, and reverse conduction current flows through body diode. The negative gate voltage deeply expands depletion region under the gate. The expanded depletion region under gate electrode by negative Vgs expands depletion region and may influence on conduction characteristics of body diode. The power supply flows reverse current in reverse direction through body diode.



Figure 1: Setup of thermal test for MOSFET

# **3** Evaluation of estimated junction temperature in static mode thermal test for SiC MOSFET

This subsection evaluates the estimated junction temperature response of SiC MOSFET for static mode thermal measurement to identify the structure function of the packaged device. The temperature is estimated with K factor, which is extracted in advance for stationary state and the experiment is performed with T3Ster (Mentor Graphics). The time for heat up with force current and the time for cooling to measure thermal response with small current and K factor are both set 30sec. The small current for junction temperature estimation is set 10mA. Two different SiC MOSFETs are experimented, and a Si MOSFET is also experimented as a reference. The specification of the studied MOSFETs are summarized in Table. 1.

	SPW20N60S5	CMF20120D	SCT2080KE
Manufacturer	Infineon	Cree	ROHM
Туре	Si SJ MOFET	SiC MOSFET	SiC MOSFET
Vds	600 V	1200 V	1200 V
Id	20 A	42 A	35 A
Rds(on)	0.19 Ω	80 m Ω	80 m Ω
Vth	4.5 V	2.65 V	$1.5-4.0 \; \mathrm{V}$
Vsd	1 V	3.1 V	4.6 V
Package	TO-247	TO-247	TO-247

Table 1: Specifications of studied MOSFETs



Figure 2: Vgs-Ids characteristics for MOSFET (Vds=10V)



Figure 3: Reverse conduction characteristics for body diode

Figure 2 shows the Vgs-Ids characteristics of the experimented MOSFETs to the applied drain voltage Vds=10 V. The threshold gate voltage for SiC MOSFETs are less than Si MOSFET as shown in Fig. 2(a), and also the slope of transconductance for SiC MOSFETs are shallower than Si MOSFET. This means the activity of carrier in channel of SiC MOSFET is lower than Si MOSFET. The temperature dependency of the threshold gate voltage for CMF20120D is shown in Fig. 2(b). The threshold gate voltage decreases with the rise of temperature, and the K factor is extracted for Ids=10 mA. The extracted K factor is utilized in type 1 measurement.

Figure 3 shows the Ids-Vds characteristics in reverse current conduction for MOSFETs. The conventional Si MOSFET shows low knee voltage in body diode conduction, which is shown by Vgs=0V in Fig. 3(a). The applied gate bias voltage higher than threshold voltage conducts channel and vanishes knee voltage. The Ids-Vds characteristics for SiC MOSFET in Fig. 3 (b) and (c) shows higher knee voltage than Si MOSFET, which stems from wide band gap property of SiC. The reverse conduction characteristics gradually changes with lowering gate voltage. The K factor is estimated from their temperature dependency.

#### 3.1 Type 1 measurement (GD short)

The estimated junction temperature response, which is based on the K factor, for cooling operation in static mode thermal measurement type 1 is shown as semi-log plot in Fig. 4. Where, the heating current amplitude is denoted in legend of the plot. The junction temperature for Si MOSFET SPW20N60S5 monotonically decreases with time just after shut off heating current, because the heat injection by measurement current 10mA is negligible. This thermal behaviour corresponds with physical phenomenon. However, SiC MOSFET of both CMF20120D and SCT2080KE show junction temperature rise up for approximately 1msec after shut off heat current. There is no heat injection and heat dissipation with higher thermal conductivity of SiC semiconductor material than Si should show decrease in junction temperature. That is, the estimated junction temperature response based on K factor for SiC MOSFET is inconsistent with physical phenomenon for short duration after switching the operation mode from heating to cooling. The gate voltage of MOSFET largely changes with the operation between heating and cooling operation in this measurement type. The positive gate bias voltage is applied to flow heating current in forward direction of MOSFET, which is higher than threshold gate voltage. But, it decreases to almost threshold gate voltage in cooling operation. The threshold gate voltage shift to positive is expected to be induced in heating operation, and this shift is relaxed for approximately 1 msec.



Figure 4: Junction temperature behavior in cooling mode operation for type 1 measurement

The time response in 1 msec contains thermal behaviour from junction of the device to die attach, which is major concern in evaluating transient thermal resistance of packaged device. Therefore, following subsection evaluates the estimated dynamic junction temperature behaviour with another measurement type, which has less gate voltage change in the measurement operation.

#### 3.2 Type 2 measurement (GD short)

Figure 5 shows the estimated junction temperature response for type 2 thermal test measurement. The heating current amplitude is denoted in legend of the plot. The voltage drop in body diode for Si MOSFET is quite smaller than SiC MOSFET as shown in Fig. 3. Then, the amount of rise in temperature for Si MOSFET results in much smaller than SiC MOSFET. The estimated junction temperature for Si MOSFET monotonically decreases after shut off heating current, which well corresponds with physical behaviour. SiC MOSFET does not show junction temperature rise after shutoff heating current, but the temperature hardly changes for SCT2080KE or slightly decreases for CMF20120D approximately in between 1 msec. This phenomenon differ with the thermal response of Si MOSFET, which does not show inflection of temperature around 1 msec.

The bias voltage imposed on the gate stemming from voltage drop by reverse conduction current in body diode has negative polarity. This negative gate voltage lessen the current conduction as shown in Fig. 3(b) and (c). This bias gate voltage polarity give adverse effect of type 1 measurement. In this sense, the estimated temperature should largely drop after changing the operation mode from heating to cooling. The effect of threshold gate voltage fluctuation is mitigated for this type of measurement.



Figure 5: Junction temperature behavior in cooling mode operation for type 2 measurement

#### 3.3 Type 3 measurement (GS short)

Figure 6 shows the estimated junction temperature response for type 3 thermal test measurement. The reverse direction current flows while maintaining gate voltage Vgs=0 V by directly connecting gate terminal to source terminal.

The voltage drop across drain-source for Si MOSFET is lower than SiC MOSFET, then the temperature rise results in smaller. The junction temperature of Si MOSFET monotonically decreases just after shut off heating current as shown in Fig. 6, which corresponds with physical phenomena. However, the estimated temperature of SiC MOSFET SCT2080KE slightly rises up approximately for 1msec, and then drops. The estimated junction temperature for SiC MOSFET CMF20120D does not rise up, but the rate of temperature deceleration is low. These estimated thermal behaviour of SiC MOSFET does not correspond with physical phenomenon. The gate voltage is clamped with 0 V. Therefore, the gate threshold voltage instability for SiC MOSFETs are expected to be induced exogenously.



Figure 6: Junction temperature behavior in cooling mode operation for type 3 measurement

#### 3.4 Type 4 measurement (gate bias)

Figure 7 shows the estimated junction temperature response for type 4 thermal test measurement. The gate voltage is biased by Vgs=-5 V with series connected dc voltage source. Junction temperature at the onset of cooling operation for type 4 measurement correspond with type 3 for Si MOSFET. Because, reverse conduction character for Si MOSFET does not differ between Vgs=0 V and -5 V as suspected from Fig. 3(a). However, voltage drop across source and drain of SiC MOSFET for heating by reverse conduction current largely increases for Vgs=-5 V. It results in larger loss and the initial junction temperature becomes higher.

The junction temperature of Si MOSFET monotonically decreases as shown in Fig. 7. The junction temperature of SiC MOSFETs also monotonically decrease, but inflection occurs around 1msec. The influence of threshold gate voltage instability is mitigated, but it still has influence on the accuracy in identifying structure function.
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Figure 7: Junction temperature behavior in cooling mode operation for type 4 measurement

#### 3.5 Discussion

K factor for knee voltage of body diode and threshold gate voltage in Si MOSFET can adequately estimate junction temperature in transient condition. However, K factor of SiC MOSFET shows inadequate temperature estimation at the onset of conduction state change. That is, the estimated temperature rises or unnaturally slowly drops by K factor for SiC MOSFET. The threshold gate voltage of MOSFET affects on the conduction characteristics in forward and reverse direction. The forward voltage drop in body diode conduction for SiC MOSFET is larger than Si MOSFET. Then, the influence of threshold gate voltage instability is severe for SiC MOSFET. The static threshold gate voltage shift to the applied bias voltage has been reported and been applicably improved for SiC MOSFET. However, the presented results indicates that the instability of threshold gate voltage for SiC MOSFET is not completely resolved, but still there is unresolved difficulty in dynamic gate threshold voltage instablitiy [6].

Figure 8 shows the estimated junction temperature response in type 3 measurement with the parameter of heating current. The low heating current give low temperature rise. 5A heating current results in 32 K and 15 K temperature rise as initial condition for CMF20120D and SCT2080KE respectively. The estimated junction temperature with K factor shows temperature rise in short period after shut off heating current for both SiC MOSFET. The larger heating current gives higher temperature rise, which obscures inadequate temperature response estimation by K factor at the onset of conduction state change from heating to cooling. The higher temperature change gives larger gate threshold voltage lowering in accordance with the junction temperature. Type 3 and 4 measurement basically utilizes body diode conduction with fixing gate bias voltage. Then the impact of bias voltage on the threshold gate voltage is expected to be small. But, the junction temperature estimation error is inferable to the applied drain-source voltage drop in body diode from heating to cooling condition.



Figure 8: Estimated junction temperature for type 3 measurement with different heating current

#### 4 Conclusion

This paper studied the applicability of junction temperature estimation by K factor in static mode thermal test measurement for SiC power MOSFET to evaluate transient thermal resistance of packaging with identifying structure function. The junction temperature of Si MOSFET can be adequately evaluated with K factor of device. However, the junction temperature of SiC MOSFET estimated with K factor gives incorrect response in thermal test measurement. That is, the estimated junction temperature rises up or drops slowly in cooling operation of power device, which conflicts physical phenomenon. This phenomenon lasts the approximately 1 ms, which disturbs to evaluate transient thermal resistance adjacent to junction of device. This defect is attributed to the dynamic instability of gate threshold voltage in SiC MOSFET, which stems from trapped charge in the gate dielectric and the interface of channel. It can be mitigated with increasing the heating current and raising initial temperature in the cooling operation. But, it does not fundamentally eliminates the cause. The improvement of SiC MOSFET performance is indispensable for fundamental solution to exact junction temperature estimation by K factor.

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**SESSION 8** 

# **SESSION 8** Thermal Design with CFD Simulation

# A Novel Approach to Heatsink Mass Minimisation

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# Abstract

Typical Heatsink design includes deciding base and fin thickness, fin height, and fin gap optimization. In situations where material cost or mass of the heat sink are also a design priority, further optimization with respect to mass removal can be significant. This paper discusses a 'Subtractive Design' method to further evolve the heat sink topology by the systematic removal of heat sink mass where the Thermal BottleNeck (BN) Number [1] was found to be lowest. The aim is to identify topologies that optimise the use of material but do not unduly affect thermal performance.

**Keywords:** Subtractive Design, Heatsink Design, Heatsink Thermal Resistance, BottleNeck Number, CFD

# Nomenclature

- $R_{th}$  Thermal Resistance (K/W) = ( $T_j T_a$ ) / P
- T<sub>j</sub> Junction Temperature (K)
- T<sub>a</sub> Ambient temperature (K)
- P Dissipated power (W)

BN – Thermal BottleNeck Number

# 1. Introduction

Typical heat sink design involves balancing trade-offs between parameters such as heat spreading, heat sink mass, airflow bypass, pressure drop, and manufacturability. A typical optimization would include varying a small number of dimensional parameters of the heat sink and a temperature rise used as the objective cost function. A Computational Fluid Dynamics (CFD) simulation offers the opportunity to consider the spatial distribution of heat transfer effectiveness and, based on that, changes made to the geometry topology with the intention of further improving the design. Previous studies have considered elements of this approach [1].

An earlier study [2] explored an additive methodology to heatsink design. In that study the heatsink fins were allowed to grow where the surface temperature was the highest, as part of an iterative design process. The heatsink topology evolved over a number of cycles until no further performance gains were achieved. It was observed that the heatsink grew as a tree-like structure from the center of the heat source. This process was also applied to grow the heatsink where the Thermal BottleNeck was largest [3], producing slightly improved behaviour compared to using surface temperature to drive the additive design process.

Thermal BottleNeck distribution was also used to directly modify fin thickness of a pre-optimized heatsink [4]. The Thermal BottleNeck values in each fin were noted and the fin thicknesses modified in an attempt to equalize the BN in each fin, leading to a marked improvement in thermal performance. The subtractive approach was first applied to an extruded plate fin heatsink under both forced and natural convection cooled conditions [5]. A single, centrally located, heat source was cooled. The study investigated two mass removal strategies: Removing geometry from any lowest BN location, which resulted in holes and gaps in the geometry that might only be manufacturable using 3D printing approaches. Geometry removal that was restricted to the top of the fins only, resulting in geometries that could be milled from an initial extrusion.

The work presented here continues to explore the use of the Thermal BottleNeck as the indicator of where to effectively modify heatsink geometry, focusing on modifications to the methodology to reduce the overall time required to perform it. Removing geometry at not just a single lowest BN location, but at a number of lowest BN locations.

A description of the Thermal BottleNeck Number can be found in Annex A and [3].

# 2. Subtractive Design Methodology

The approach consists of removing a small piece of geometry, of a predetermined volume, from the point where it is found to make the smallest contribution to increasing the thermal resistance. This process is repeated to construct a graph relating total heatsink mass reduction to change in heatsink thermal resistance.

The initial heatsink consists of a previously optimized plate fin extrusion with respect to base thickness, number of fins and fin height. Such a subtractive approach could be applied to any area extending geometry, whether additively designed or optimized using more classic parametric approaches.

The initial heatsink is simulated in the environment used for optimization and the Thermal BottleNecks calculated for each material volume in the heatsink. These material volumes are considered as small tessellated portions of the geometry. The 'N' material volumes with the lowest BN numbers are then removed, a new simulation conducted, and the process repeated. Note that the approach of removing the lowest 'N' material volumes is intended to accelerate the process, compared to removing only one at a time. Two values of N will

#### Bornoff, A Novel Approach to Heatsink Mass Minimisation

be investigated, 4 and 15, to determine their sensitivity to resulting mass reduced topologies.

Removal of the heatsink mass, and related convective surface area, will eventually lead to much higher heatsink thermal resistance. However the intention of this study is to attempt to identify if there are opportunities to remove heatsink mass without unduly increasing thermal resistance. The design iterations could be continued until no heatsink mass remained. In practice the design analysis would stop when the thermal resistance matched the performance requirement or was otherwise considered optimized.

# **3.** Application to a Natural Convection Cooling Environment

A sealed 5mm thick Magnesium alloy enclosure housing 3 surface mount TO263 power amplifiers that are mounted onto an internal surface of the enclosure (Figure 1). That face of the enclosure has external extruded type heatsink fins whose height, number, and thickness have each been optimised using a classical parametric gradient based optimisation method so as to minimise the maximum thermal resistance of the system. The junction temperature of the higher powered (8W) component is used to determine the system thermal resistance. The unit is vertically orientated in a natural convection environment at an ambient temperature of 35 DegC.



Figure 1: Sealed Enclosure with 3 Power Amplifiers



The resulting non-uniform temperature distribution is shown in Figure 2.

Figure 2: Surface Temperature Distribution Bornoff, A Novel Approach to Heatsink Mass Minimisation

The fin geometry was discretised into 3850 material volumes, shown in Figure 3 for one of the fins.



Figure 3: Discretised Fin Volume (single fin shown for clarity)

The sequential removal of the lowest 4 BN material volumes is conducted until such time as all fin volume has been removed. A resulting graph relating the increase in system thermal resistance, from 0% increase to 100% increase when all fins are removed, is plotted against the % reduction in fin mass (Figure 4).



Figure 4: Increase in System Thermal Resistance vs. Reduction in Heatsink Fin Mass (fins coloured for clarity)

Removal of more material volumes at each stage will reduce the overall time taken for the subtractive design process to complete but would in theory alter the resulting heatsink topology sequence. Figure 5 compares removing 4 and 15 material volumes at a time.

22nd Therminic Workshop



**Figure 5:** Increase in System Thermal Resistance (log Scale) vs. Reduction in Heatsink Fin Mass Comparing 4 and 15 Material Volume Removals at a Time

The full subtractive process when removing 15 material volumes at a time was 3.5 times faster than when removing 4 at a time (25 vs. 86 hours) and with only minor degraded performance during the initial mass reduction stages.

#### 4. Discussion and Conclusions

This approach can be considered valuable if it demonstrates that a large amount of heatsink fin mass can be removed without incurring a correspondingly large increase in thermal resistance. In fact 50% of the fin mass can be removed (Figure 6) with only a 5% increase in thermal resistance (compared to the thermal resistance with no removal of fin mass).



**Figure 6:** Heatsink Geometry at 50% mass removal, 5% increase in Thermal Resistance, 4 Material Volumes Removed at a Time

Despite the initial topology having plate fins, the removal process identifies a hybrid type design with plate and pin type fins (Figure 7):

- Single plate fin over the over the highest power component
- Pin type fins over the larger area hotspot from the lower powered components
- A much reduced density of pins and fins over the cooler areas of the enclosure, where they are not required



Figure 7: Surface Temperature Distribution at 50% Mass Reduction

Having employed the subtractive design method to determine a mass efficient heatsink topology, it could be parameterized and a more classical gradient-based or response surface optimisation be used to fine tune the design.

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Bornoff, A Novel Approach to Heatsink Mass Minimisation

#### Annex A

Heat flow can be defined in terms of a heat flow through a given cross section area. This measure is known as a heat flux. The presence of a heat flux vector will always result in a temperature gradient vector. The temperature gradient field is taken to be an indicator of conductive thermal resistance as, for a given heat flux, the greater the temperature gradient is the larger the thermal resistance will be.

The dimensionalized Thermal BN Number is the dot product of the above 2 vector quantities. At each point where there exists a heat flux vector and temperature gradient vector:



The BN scalar at that point is calculated as:

Heat Flux magnitude (i.e. length of the heat flux vector arrow) x Temperature Gradient magnitude (i.e. length of the temperature gradient arrow) x |Cos(Theta)|

Note that |Cos(Theta)| is always positive. If the angle between the two properties is zero, i.e. the heat flux is aligned with the temperature gradient as it would be for conductive heat flow in a homogenous thermally isotropic material, then the BN number is the product of the vector magnitudes (i.e., |Cos(Theta)| = 1). If the temperature gradient is orthogonal to the heat flux then the Thermal BN Number is zero.

SI units for such a dot product are degC W/m<sup>3</sup>.

Regions of the analysis that exhibit large values of Thermal BN, will have three qualities:

- A large value for heat flux, i.e., it will be on an existing heat transfer path of significance.
- A large value of temperature gradient, i.e., there will be significant thermal resistance at that point.
- The heat flux and temperature gradient vectors will be aligned

Therefore, areas that are thermal bottlenecks, i.e., are on an existing heat transfer path and experience significant resistance to heat transfer, will result in large values of the Thermal BN Number. Once these bottleneck areas have been 'designed out', heat will leave the model more 'easily' thus reducing all 'upstream' temperature rises, all the way back to the heat source.

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#### Bornoff, A Novel Approach to Heatsink Mass Minimisation

# Flexible CFD Simulation Model of a Thin Vapor Chamber for Mobile Applications

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# Abstract

Heat loads produced by electronics in mobile devices affect the external temperature distribution, which users perceive. During the design phase of a product, these distributions have to be taken into account. Simulation provides a way to try different design approaches quickly. Vapor chambers are thin heat spreaders that offer very high spreading capabilities without adding too much thickness to a low profile device. The heat spreading makes the external temperature more uniform. To simulate a vapor chamber fully would require simulation of phase changes and rapid mass flows in a very thin volume. This kind of detailed simulation is cumbersome in a system level model. Therefore, a simpler model would be useful. A few of these exist but the goal in this work was to develop a behavioral approach which would model the vapor chamber as a single object in the system model.

# 1 Introduction

Thin vapor chambers can spread heat very evenly without adding too much thickness to a low profile system like a phone or a tablet. During the design phase it is crucial to be able to make quick simulations to see how well heat is handled in the device. This requires a simulation model that doesn't take a long time to solve. Simulating the two phase flow in a vapor chamber can prohibitively increase the total complexity of a system level CFD model. The most common way to simplify the model is to exclude phase changes and mass flows inside the vapor chamber and model only the aggregate behavior of the vapor chamber. This can be done with knowledge that the biggest resistance is created by the wick and that the conductivity of the vapor space is much larger than every other component in the vapor chamber. This means that the vapor chamber can be modelled with at most three cuboids. However, even a simplified model requires knowledge of the vapor chamber internal details. Such details are usually not shared by the vendor. Also, multiple very thin layers pose an even greater modeling challenge than the one posed by the thin dimension of the vapor chamber.

Note that the heat pipe modelling capability built into the commercial software is meant as a conductive element only. It assumes that only a small percentage of the heat is lost along the length of the pipe. [1] This assumption is unsuitable to the present application, where heat loss is evenly distributed over the surface.

To minimize the number of required cuboids, an even simpler model using only one cuboid is studied in this paper. The goal is to develop a method to create a behavioral model of a vapor chamber to represent its spreading ability. Ideally the model would scale and adapt to changes like size, thickness and heat input. A second objective is to develop a modelling method which can characterize the behavior of the vapor chamber easily over the range of likely application parameters.

# 2 Background

Vapor chambers are two phase heat spreading devices similar to heat pipes. They share the same working principle, and the same basic theory can be applied to both. The main difference is that while heat pipes typically are long pipes, vapor chambers are more like plates. Whereas heat pipes commonly are used to transfer heat from one narrow location to another, vapor chambers are used to spread heat over a wide area. The wider area gives better thermal dissipation performance and temperature uniformity to a system. This helps to better transfer heat to a heat sink, or in case of a mobile device, to spread the heat over the cover of the device. In passively cooled devices, uniform heat distribution is essential to achieve better user experience and better performance without thermal throttling, and also to increase the dissipation capability of the device while maintaining user comfort temperature limits on the cover.

Both heat pipe and vapor chamber work through a phase change process which is driven by heat. They have the same components: wall, evaporator, wick, working fluid, vapor space, condenser. The wall is thermally connected to a heat source. Heat is conducted through the wall to the wick and then to the working fluid. In the evaporator region, the fluid evaporates from the wick to the vapor space. This vapor space is typically below atmospheric pressure. The vapor travels from near the heat source to a cooler area in the spreading device and condenses back to liquid. The wick absorbs liquid, and capillary action draws it back to the evaporator. Because the vapor condensation area can be anywhere that the temperature is low enough to condense the vapor, the temperature differences are minimized. This is further

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amplified by the fact that higher power drives vapor farther from the heat source as it expands farther into the cooler region. With these processes, the vapor chamber can achieve an order of magnitude or greater effective conductivity than copper. [2]

The governing equations for heat conduction show that the temperature gradient scales linearly as the power. This model is unsuitable to model vapor chamber behavior, as the temperature gradient tends to be constant while the power varies. The experimental data in Figure 1 shows these opposing trends. For low power, the copper spreader outperforms the vapor chamber although it is much thicker, and not a practical thermal solution for mobile devices. As expected, the temperature gradient increases with power for the copper. The vapor chamber (VC) maximum temperature gradient is approximately constant over the tested range of power. The same trends have been found before. [3]



Figure 1: Temperature gradients in 3 mm thick copper vs 0.6 mm thick vapor chamber spreaders.

Modeling the vapor chamber using conductive elements has been addressed before. [4] The vapor space, being the biggest contributor to heat transfer, is modeled as a solid with very high thermal conductivity. To account for conduction into the vapor space, a known thickness of copper represents the shell, and another, lower thermal conductivity solid models the wick regions. This method generates very thin grid cells. It also requires some knowledge of the construction of the vapor chamber, which is not available in every instance.

# 3 Approach

Experimental data was used as the basis for developing the model. First, data using a copper spreader was used to calibrate the model, using a best-fit technique to arrive at model unknowns. This calibration model is explained further below.

Next, for each power level, runs of the model were made using the calibration values and several values of conductivity in the thin vapor chamber. Comparing these results with experimental data gave a normalized error value that varied with the conductivity. The conductivity that resulted in the least error varied with power level. Since the spreader temperature varied with power, the conductivity can be considered to vary with spreader temperature, as long as ambient and physical geometry are fixed.

Finally, to validate the model, the resulting temperaturedependent thermal conductivity was used to model another, unrelated data set to verify its usefulness and accuracy.

# 3.1 Physical experiments

Experimental heat spreading performance measurements were done with a thermal test vehicle (TTV). It has a heater element that mimics the chip and can accurately produce wanted heat load to the system. Measurements were done with six power settings (1, 3, 5, 7, 8, 9 W), and two different types of spreaders with various thicknesses were used. A painted copper spreader with thickness of 3 mm was used as calibration sample. The spreader was oriented vertically with respect to gravity to simulate the intended handheld device use condition. The experiments were carried out in a still-air chamber controlled at 25 °C. To minimize the heater temperature, a clamp was used together with a thermal interface material between the heater and the spreader, and the load kept at a consistent value using a load cell. An acrylic block on each side minimized heat leakage into the clamp. A picture of the setup is shown in Figure 2.



# Figure 2: Experimental setup

Thermocouples used in experiments were first tested to ensure that they give consistent values. For this all 14 thermocouples were attached to a vapor chamber with adhesive tape. The setup was in a controlled environment with temperature at 35 °C. There was no additional heat in the system. Measurement ran 218 minutes, and data points were recorded every 2 seconds. Then an average value for each time was calculated, and each data point was compared to the average. Last, the average deviation value was calculated for each thermocouple. Overall, the maximum deviation from average was 0.125 °C.

Thermocouples were attached to both front and back surfaces of the heat spreader with thermal grease and adhesive tape. On the outward facing surface they were placed near the extreme corners and along the center line. This way the temperature distribution could be captured over the surface of the heat spreader. Thermocouple locations are shown in Figure 3. Locations 1-6 are on the outward facing side of the spreader. An additional thermocouple is on the inward facing side of the spreader, directly adjacent to the heat source contact area and opposite thermocouple 6.

# 3.2 Calibration model

Commercial CFD code was used for the simulations. The model included the test board and heater chip, test spreader and interface material. The acrylic block was also included as well as a simplified representation of the test fixture's acrylic panel surrounding the test board. Boundary conditions matched the experimental setup for orientation, quiescent environment and stable surrounding temperature. Figure 4 shows an isometric view of the model. Figure 5 shows the cross sectional view of the heater assembly. The heater is at the center. To the left is the main heat spreading path with a layer of thermal interface material (TIM), the copper spreader, and an acrylic pressure block. The heat leakage path to the right includes the test vehicle solder balls, board, and acrylic pressure block. The load cell and clamp were not included in the model.





Figure 3: Temperature sensor locations

Figure 4: Model geometry overview. The spreader area is about  $6000 \text{ mm}^2$ .



Figure 5: Experimental stackup components

The model was calibrated with experimental data from a 3 mm thick painted copper spreader at 7 W heater power. Copper has well known thermal properties so it may be used to solve unknown parameters. These were emissivity of the paint covering the spreader, test vehicle PCB conductivity, thermal interface material conductivity and surface thermal resistivity. Multilinear fitting and error minimization provided values for the unknowns that resulted in best fit to the measurements. A total of 98 different designs, which were created by using design experiments tools, were used in this calculation. Optimized values are shown in Table 1.

Table 1: Calibration values for best fit

Unknown	Value
Emissivity	0.89
Board conductivity (W/(m K))	40
TIM conductivity (W/(m K))	6
TIM surface resistivity ((K m2)/W)	5e-06

# 3.3 Thermal conductivity models

After calibration, a 0.6 mm thick painted vapor chamber was modelled. To find the best conductivity value for each power setting, a range of thermal conductivity was used. Each conductivity value yielded a set of temperatures that were compared to the corresponding experiment. RMS error was calculated for each pair, and this set was used to form the behavioral model by minimizing the RMS error. The range of thermal conductivity to use was chosen based on the online calculator for spreading resistance in the case of isotropic circular-disk heat spreaders with convective cooling by the Microelectronics Heat Transfer Laboratory at the University of Waterloo. [3] The trend, shown in Figure 6, is that the spreading resistance is very sensitive to the value of thermal conductivity when the conductivity is low, but once the thermal conductivity is high, further increases in conductivity produce minimal reduction in spreading resistance.



Figure 6: Thermal resistance as a function of thermal conductivity, theoretical result

# 3.4 Validation model

To validate the resulting thermal conductivity approach, a separate set of data was used that had different spreader geometry, orientation, and physical implementation. The spreader was horizontal and was resting on thermal insulation, so that heat could dissipate primarily from the top surface. Two power levels were used, 5 W and 10 W, where 10 W required extrapolation beyond the originally tested power range.

# 4 Results

# 4.1 Thermal conductivity results

Results from simulations were normalized to the minimum error for each power setting to obtain the thermal conductivity value that provided the best fit. The normalized errors are shown as a function of the conductivity in Figure 7. In this figure it is evident that the best-fit thermal conductivity increases as the power setting increases.





Figure 7: Normalized error as a function of conductivity for various power levels

#### 4.2 Temperature dependent thermal conductivity

Plotting the best-fit thermal conductivity as a function of power as in Figure 8 shows the trend.



Figure 8: Best-fit thermal conductivity as a function of heater power

The same trend appears when the average spreader temperature is substituted as a proxy for the power. Power as a rule is a boundary condition, rather than a property of a grid cell. Thus, for the thermal conductivity to vary, it must be a function of the temperature as in Figure 9.



Figure 9: Best-fit thermal conductivity as a function of spreader temperature

The variable conductivity algorithm built into the CFD software uses a reference temperature and conductivity, and a slope to infer conductivity when the temperature deviates from the reference temperature. Thus, to use the algorithm a linear approximation must be made. Since the low power cases are not thermally challenging, and high power cases will drive high temperature and therefore high conductivity, an intermediate range of slope is most useful.

### 4.3 Validation results

The results were verified with a model which was based on the vendor's test setup. This setup differed from the previous test configuration in size and orientation as well as boundary conditions. The experiments were done with 5 and 10 W power. As with the previous data, the model was calibrated with results from the experiment done with the copper spreader. The calibrations were then applied to the vapor chamber model. Simulations done with the behavioral model showed good agreement with experimental results for both power settings, see Figure 10. A constant-conductivity model over-predicts the temperature at the outer edges of the spreader, whereas the variable conductivity model shows very good agreement. Location 7 does not show good agreement in any of the cases, most likely because it was mounted directly on the heater, and also because the approach ignores dominant resistance from the wick in the throughplane direction.

For the 10 W case, the spreader temperature is above 80 °C, leading to a variable conductivity of around 10000. For the 5 W case, the spreader temperature is around 55 °C, or a variable conductivity around 5000 – very close to the assumed constant conductivity. This explains why the 5 W

validation results are insensitive to the type of model. The 10 W results show an appreciable difference.



*Figure 10: Validation results. Constant conductivity value is* 5170 W/mK

It is known that this model is not valid in transient situations, or for heat fluxes approaching dry out limits. Therefore startup and dry out conditions cannot be predicted, and these have to be modelled with different means. Also it is expected that the model would need to be changed for different ambient temperature by adjusting the reference temperature.

# 5 Conclusions

By tuning a behavioral simulation model of a vapor chamber to match experiments, a robust, simple model can be achieved. The model will be more flexible than models with constant conductivity as it will react to temperature changes as a real vapor chamber would.

Results show that even without detailed knowledge about the construction of the vapor chamber that is modelled, a behavioral model can be created by comparing measurement data to simulation data. RMS minimization shows how the vapor chamber reacts to power and temperature changes.

Simulating a vapor chamber simply by using thermal conductivity as a function of temperature (which is a proxy for the power) is a useful way to include the spreading behavior of the vapor chamber in a complex system model with more accurate results than can be achieved by a constant-conductivity model.

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# Heat Transfer Enhancement in Micro-Scale Air Flows

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# Abstract

The aim of the present study is to extend air-cooling capabilities. A method of generating an unsteady vortical flow within small annular channels is introduced and studied numerically. The addition of an orifice at the entrance to the channel generates a propagating train of vortex rings that induces the continuous eruption of hot air from the wall region into the core flow. The overall effect is significant transverse convection even in laminar flows and enhancement of heat transfer. The effect of the orifice diameter is studied in detail. The method is very appealing for extending cooling capabilities of heat-sinks based on air, but it works similarly well for single phase flow of liquid. An increase of almost two-fold in the heat dissipation relative to a standard microchannel can be obtained. Heat dissipation of 8watt/cm<sup>2</sup> per contact area can be anticipated using a single layer of the proposed air-based orificed-microchannel.

# 1 Introduction

Several approaches are being used to meet the high cooling demands of power devices together with their miniaturization. The use of mini- and microchannels are among the most promising methodologies, [1-7]. Minichannels refer usually to channels with a hydraulic diameter less than 3mm but larger than 200µm. Microchannels have even smaller diameters. In the following, we shall use the term microchannel to channels of a hydraulic diameter less than 1mm.The low Reynolds number flows associated with the small size of microchannels might have detrimental effects on the cooling capabilities if air is used as the coolant. Therefore, liquids are common together with the use of long channels  $(L/D > 10^3$ , where L and D are the length and the hydraulic diameter of the channel). Heat fluxes as high as 10<sup>3</sup>watt/cm<sup>2</sup> can be dissipated by microchannels heat-sinks using water. Nevertheless, air is preferred in electronic devices if the desired cooling can be achieved. Naturally, it is orders-of-magnitude less than in the case of liquids. Studies of gas flow in microchannels are scarce relative to liquid flows. The survey of [2] found that less than 19% of the studies up to 2011 were devoted to air or gas flow. Since then, the ratio seemed to decrease even more. Presently, a maximum of less than 3watt/cm<sup>2</sup> (of contact area) can be dissipated by microchannels using air as the coolant. The maximal heat transfer coefficient obtained in these cases is 350 watt/m<sup>2</sup>/°C, [1].

In the present study, we seek to extend air-cooling capabilities using annular microchannels by manipulating the flow field. The low Reynolds flow in microchannels result in many cases laminar flow with small transverse convection and hence unfavourable heat transfer properties for both liquid and gas flows. In the case of liquids, the low convection is compensated by their large heat capacity and the use of long channels  $(L/D \gg 1)$ . The key for enhancing heat transfer is increasing transverse convection in laminar flows as well. Several such enhancement methods have been suggested for water based microchannels, see review of [8]. In most cases, the improved cooling relies on increasing contact area and/or on generating flow features absent in standard channels, such as developing or vortical flows. In the first category, one can mention corrugated channels [9, 10], while in the second category one can list segmented flows or flow interrupting designs [11] that generate developing flows in the case of long channels as well. Recently, various vortex promoters gained popularity. They include offset-strip geometries and ribs [12], pillars [13], various shapes of micro-fins [9] or micro-pins [5, 14-15] placed inside the channel. Other vortexgenerating methods include shaped-walls, such as sinusoidal walls [16], or nature-inspired shapes [17]. A few of these techniques were optimized using CFD, yielding a two-fold increase of Nusselt number at the cost of significant increase of the pressure drop.

Vortex promoters create a vortical flow fields that enhance heat transfer through the mixing generated by the vortices. However, due to the low Reynolds, the flow field and the vortices are in most cases stationary, except if the blockage ratio and the Reynolds number are large enough to promote von-Karman vortex shedding with the associated increase in pressure drop, [14]. Moreover, the intricacies and the high fabrication cost of such microchannels make these enhancement methods less applicable.

In the present study, we suggest a heat transfer enhancement method that overcomes some of the aforementioned issues. Without the need of adding micro-structures, an unsteady vortical flow field can be established within annular microchannels. It is achieved by passing the fluid through an orifice before entering the microchannel. This simple geometry and the required short channels (L/D < 4) make this option very appealing. It effectively increases heat dissipation for both liquids and gases, but it is more attractive for air since the enhancement can extent present air-cooling capabilities. Results of a numerical investigation of the heat transfer performance of orificed-channels using air as the coolant are presented in this paper.

# 2 Methods

The axisymmetric domain of simulation is shown in Fig. 1. An inlet reservoir with open boundaries is defined upstream of the channel. The microchannel has a circular cross-section with a constant diameter of D = 0.45mm and a length of L = 4mm. At the upstream part, a circular vertical wall exists with a concentric orifice of diameter  $D_{orf}$  that varies from a small value of 0.15mm to a fully open channel. The latter case will be also referred to as the *standard microchannel* (SMC). The orifice diameter ratio is defined as  $D^* = D_{orf}/D$ . The case of  $D^* = 0.8$  is referred to as the *Base Case*. The case of  $D^* = 1$  is the SMC case. The axial coordinate *x* has the origin at the orifice.



Figure 1: The computational domain

The typical sizes involved allow the assumption of continuity. The unsteady, laminar compressible Navier-Stokes equations have been employed to simulate numerically the flow of air within the orificed-microchannels. In the SMC case and in the case of the largest orifice ( $D^* = 0.89$ ), the larger flow rate increases the Reynolds number to  $Re \approx 2700$  and therefore the unsteady Reynolds-Averaged Navier-Stokes equations were solved in these cases employing the transition k-kl- $\omega$  turbulence model. The flow is compressible since the air flow rate needed to obtain significant cooling is large, yielding high velocities in the microchannel with Mach numbers well over M > 0.3. The air is assumed to be a perfect gas.

At the upstream boundary, the inlet gauge stagnation pressure  $(P_T)$  is specified; in the results to be presented  $P_T$ =10kpa. The stagnation pressure is a measure of the mechanical power of the inflow and therefore it may serve as a reasonable condition for comparing the performance of the various orifice size cases. The orifice size determines the volume flow rate; the larger the diameter of the orifice is, the larger is the volume flow rate for the given stagnation pressure. On the walls zero velocity is imposed, while at the outlet, zero gauge pressure is specified. To model the open boundary upstream of the orifice wall, symmetry conditions are given. The inlet stagnation temperature was specified to be  $T_T = 30^{\circ}$ C and the microchannel wall is assumed to have a uniform temperature of  $T_w = 70^{\circ}$ C.

The Ansys Fluent CFD package has been employed. A quadrilateral mesh of 130,000 nodes has been selected following a mesh-independence test. Mesh nodes are clustered near the walls, in the orifice region and in the shear layer downstream of the orifice. Second-order spatial and temporal schemes have been used together with the PISO approach. The solution is advanced in time until a time-periodic solution is obtained. This was achieved after not less than a time of  $t^* = Ut/D > O(10^3)$ , where U is the average axial velocity in the channel and t is time.

# **3** Results and discussion

Figure 2 presents the evolution of the non-dimensional vorticity field for one shedding cycle of the Base Case. The vorticity is non-dimesionalized by U/D. The vortex shedding cycle has a period of  $T_{per} \approx 11 \mu s$ . The shear layer generated at the orifice circumference rolls up into a vortex ring that is eventually disconnected from the feeding shear layer and is shed downstream. The formation time [18] in the present case is  $F^* = UT_{per}/D_{orf} = 3$ . It is smaller than obtained for vortex-rings generated in an unbounded flow ( $F^* = 3.8$ , [18]). The proximity of the wall induces counter-rotating vorticity (the leftmost blue region in Fig. 2) that is dragged away from the wall by the forming vortex ring. That countervorticity facilitates in the premature disconnection of the vortex ring through vorticity cancellation. In each cycle, a vortex ring is generated. The vortex rings propagate downstream, generating a moving train of vortices. This propagating train of vortex rings drags counter-rotating vortices away from the wall of the channel. The overall effect is the generation of an unsteady flow field with large transverse (radial) motion, augmenting heat transfer.



Figure 2 The vorticity evolution in a single shedding cycle of the Base Case

The instantaneous Mach number, non-dimensional vorticity and temperature fields are shown in Fig. 3 for  $t/T_{per} = 0$ (Fig. 2). The temperature is non-dimensionalized by  $T' = (T - T_{in})/T_w - T_{in}$ ), where  $T_{in}$  is the static temperature at the inlet. Regions of Mach number as high as 0.6 are found in the vicinity of the vortices, justifying the assumption of compressible flow. The increase of the Mach number downstream of the orifice decreases the static temperature by about 13°C (T' = 0.3, Fig. 3c), increasing further heat transfer. The temperature field reveals significant mixing and similarity with the vorticity field. Hot air eruptions from the wall region coincide with the eruptions of counter-vorticity.

The variation of the heat flux from the channel's wall at the same instant is depicted in Fig. 3d. Peaks of heat flux are found on the downstream side of the vortex rings where cold air is dragged away from the core flow into the wall vicinity, increasing the temperature gradient. Hot air is ejected into the core flow at the upstream part of the vortex rings. The vortex rings decay downstream decreasing the heat flux. The heat transfer efficiency seems to decrease significantly downstream of x/D > 3.



Figure 3: The instantaneous (a) Mach number, (b) vorticity, (c) temperature fields and (d) the wall heat flux [watt/cm<sup>2</sup>] at  $t/T_{per} = 0$  of the Base Case

The enhanced mixing has a paramount effect on the mean properties, Fig. 4, where the mean temperature field of the *Base Case* is compared with the steady temperature field of the SMC case. The higher average temperature of the air is noticeable in the case of the orificed-channel, indicating the larger heat dissipated from the wall. Whereas in the SMC the temperature of the core flow is unchanged, in the orificed-channel the temperature increases in the core as well. No significant axial variations of the temperature field are found for x/D > 3, indicating that heat transfer is less effective in the downstream part of the microchannel.



Base Case with (b) the SMC case

The heat transfer coefficient h(x) and the total heat dissipated Q(x) along the microchannel wall of the *Base* 

Case are compared with the SMC case in Fig. 5. The heat transfer coefficient is defined as  $h(x) = q(x)/(T_w - t_w)$  $T_m(x)$ ). The bulk temperature at a cross section x is defined by  $T_m(x) = \int \rho u T dA / \int \rho u dA$ , where  $\rho$  is the density, u is the axial velocity and dA is a cross-section area differential. The total heat dissipated is calculated from the start of the channel up to x/D. The orificed-channel has a significant advantage up to  $x/D \approx 3$ . Downstream of this location, the heat transfer coefficients are almost identical. At large distances x, it approaches the value of 350 watt/m<sup>2</sup>/°C, cited by [1] as the maximal heat transfer coefficient of existing (very long) microchannels. The larger heat flux at the upstream portion of the channel generates an excess of 0.05 watt in the total heat dissipated up to x/D = 3. This translates into doubling the dissipated heat by the orificedmicrochannel relative to the SMC for such short channels.



Figure 5: Comparison of (a) the heat transfer coefficient and (b) the total heat dissipated of the Base (blue solid line) and the SMC (black dashed line) cases.

The distribution of the heat transfer coefficient, the total heat dissipated and the average Nusselt numbers for several orifice diameter ratios are plotted in Fig. 6. The average Nu number is calculated from:  $\overline{Nu}(x) = \frac{1}{x} \int_0^x Nu(x') dx'$  where the local Nusselt number is defined as Nu(x) = h(x)D/k, ;k is the thermal diffusivity. For  $D^* > 0.5$ , the heat transfer coefficient has a maximum downstream of the orifice with the largest value for  $D^* = 0.8$ . This orifice diameter ratio seems to be optimal in the sense that the wall is far enough to generate strong vortex rings but it is also close enough to yield strong interaction between the vortex rings and the wall to promote the eruption of hot fluid from the wall. The location of the maximal heat transfer coefficient moves downstream with the decrease of the orifice diameter due to

the shadowing effect of the orifice wall that reduces velocity and hence decreases heat transfer. The maximal heat transfer coefficient for  $D^* = 0.8, 0.73$  and 0.67 is found at x/D =1.4, 1.6 and 2, respectively. Again, it is observed that for L/D > 4, the heat transfer is less effective and it approaches the values of a SMC. Small diameter orifices of  $D^* < 0.6$ , yield very low heat transfer rates, even lower than for SMC as a consequence of both the decrease in flow rate and the too large distance of the wall that inhibits any interaction with the wall. Moreover, due to the small diameter of the orifice in these cases, the air is almost stagnant near the wall.



Figure 6: Variation of the (a) heat transfer coefficient, (b) total heat dissipated and (c) average Nusselt number for various  $D^*$ 

The magnitude of Q(x) along the channel in the case of  $D^* = 0.8$  (the *Base Case*) is only marginally higher than for  $D^* = 0.73$ . Decreasing more the orifice diameter results in degradation of the total heat dissipated, but still it is larger than for the SMC, especially for shorter channels (L/D < 4). The total heat dissipated for the largest orifice diameter ratio of  $D^* = 0.89$  is only slightly higher than from the SMC.

However, it is achieved by using 6% less volume flow rate. The large diameter orifice case is similar to a single rib case [12].

The variation of the average Nusselt numbers along the channel for the various  $D^*$  (Figs. 6c) re-iterate the previous findings that the orificed-channels remove heat effectively only in the upstream part of the channel. The average Nusselt number is maximal for even shorter channels of  $L/D \approx 1.5$  and 2.5 for  $D^* = 0.8$  and 0.67, respectively. Converting it to dimensional quantities, a microchannel of diameter 0.45mm and a length of 0.7 or 1.1mm for orifice diameters of 0.36 and 0.3mm, respectively, can remove 0.07 watt. A SMC of the same diameter and lengths can remove (using air) 0.028 and 0.044 watt only. To dissipate 0.07 watt, the SMC should be 1.8mm long.

So far, only heat dissipation has been considered. However, other performance criteria can be of interest as well, such as the Coefficient-Of-Performance (*COP*) that is defined as the ratio between the heat dissipation rate and the pumping power needed to drive the flow, i.e. COP(x) = Q(x)/W(x), where  $W(x) = \int_{x}^{inlet} P_T u dA$ . In most other studies, the pumping power is approximated by  $W(X) \approx \dot{V}\Delta P(x)$ , where  $\dot{V}$  is the volume flow rate and  $\Delta P(x)$  is the static pressure drop. This approximation assumes minor variations in the kinetic power. In the present high velocity cases, this approximation cannot be done.



Figure 7: The variation of the COP for various D<sup>\*</sup>

Figure 7 presents the variation of the *COP* as a function of  $D^*$ . Among the configurations tested, the SMC has the best *COP*. Still, it is 1-2 orders of magnitude smaller than conventional solutions based on fan and fin-based heat-sinks. This decrease of the *COP* is typical to microchannels and need to be paid for the compactness of the design. For long enough channels (L/D > 4), the larger diameter orifices ( $D^* = 0.80$  or 0.73), have a *COP* only slightly lower than for the SMC (but remove more heat, see Fig. 6b). Independent of the orifice size, a minimum is found in the *COP* at  $x/D \approx 1.5$ , mainly as a result of the large pressure drop through the orifice. Further downstream, the *COP* improves due to pressure recovery and the relatively low power needed to drive the flow in these sections of small pressure drop.

Figure 8 presents for a channel 1.5mm long (L/D < 3.3), the dependence on  $D^*$  of the gain relative to a SMC of the heat dissipation and the *COP*. Either small or large  $D^*$  are unattractive (small heat dissipation rate and small *COP*). However in the range of  $0.85 > D^* > 0.65$ , significant gain is obtained at the expense of only a small decrease in *COP*. An increase of 90% in the heat transfer rate can be obtained with a penalty of only 20% decrease in the *COP*.



Figure 8: The gain in the heat dissipated (blue solid line) and in COP (red dashed line) relative to the SMC for a channel of length L/D = 3.3 (L = 1.5mm)

In addition to the COP, other performance criteria are being used, such as the heat dissipated per contact area or per volume of the heat-sink. A possible design may include a single row of orificed-microchannels with  $D^* = 0.8$ , channel diameter of D = 0.45mm and a length of L = 1.5mm. Taking the distance between adjacent channels and the height to be 2D (0.9mm) results in a heat dissipation per area and per volume of  $Q/A_{HS} = 8$ watt/cm<sup>2</sup> and  $Q/V_{HS} = 90$ watt/ cm<sup>3</sup>. The index HS refers to the heat-sink contact area or total volume. The value of  $Q/A_{HS}$  can be further increased by adding layers of tubes. For example, taking into account conduction loses,  $Q/A_{HS} > 16 \text{ watt/cm}^2$  can be obtained using three layers of orificed-microchannels using air. This is far better than can be obtained using conventional fan and fin heat-sinks that obtain at best  $Q/A_{HS} < 2.5 \text{watt/cm}^2$  and  $Q/V_{HS} < 0.5 \text{watt/cm}^3$ .

# 4 Concluding remarks

A method of generating an unsteady vortical flow within mini and micro annular channels is introduced and studied numerically. The addition of an orifice at the entrance to the channel generates under favorable conditions a propagating train of vortex rings that induce continuous eruption of counter-rotating vortices and hot air from the wall region into the core flow. The overall effect is a significant enhancement of mixing in general and heat transfer in particular even in the case of laminar flow. An increase of almost two-fold in the heat dissipation relative to a standard microchannel can be expected for constant temperature boundary conditions, while keeping very compact size of the heat-sink. Similar gains can be obtained by using micro-structures within the microchannel, such as micro-pins or fins, [5, 9, 14-15]. However, in the present case, the heat transfer enhancement is obtained by employing very simple geometry. The method is very appealing for extending the cooling capabilities of heat-sinks based on air, but it works similarly well for single phase flow of liquids as well, including water. In the case of air, compressibility is not negligible. It does increase heat transfer from the wall next to the downstream due to the larger temperature difference in the regions of flow expansion.

The heat transfer properties are very effective in short microchannels, L/D < 4. This is in contrary to standard microchannels that use very long channels,  $L/D > O(10^2) - O(10^3)$  and most of the flow field is fully developed. The very short channels allow compact designs of heat-sinks based orificed-microchannels. However, such devices pose a challenge in the design of the supply and evacuation system.

The compactness of the heat-sink and effective heat dissipation have a price in the form of elevated pressure drop. However, the cost in terms of *COP* is comparable to standard microchannels because the resulting flow rate decreases. Lower pressure drops and higher *COP* can be achieved by increasing the size of the channel and the orifice at the expense of compactness.

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# **Detailed Analysis of IC Packages Using Thermal Transient Testing and CFD Modelling for Communication Device Applications**

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# Abstract

Due to the increased functionality and increasing power load capabilities, the thermal design of communication device applications is becoming more and more crucial in today's handheld device industry. Based on the thermal transient measurement principle, a series of thermal tests can be taken to help thermal engineers better understand the thermal impedance characteristics of high -performance multi-core SoC chips and their packages widely used in communication device applications.

The main topic of this article is to share an effective test method for multi-core SoC chip embedded with capacitors in a PoP package. Beside the experimental results the detailed numerical model of the dedicated chips and packages is created in FloTHERM and calibrated against the measurement results.

# 1 Introduction

In the current, increasingly high computing power mobile and communication device industry, the packaging of the high-performance multi-core devices are the key challenges which enable system level integration. Traditionally side by side SiP-s were used to extend the technological boundaries, however recently stacking has become the most commonly used technology to improve the package performance. Such multi heat-source packages however require very careful thermal design, the designers have to make sure that each chip in the package and even each core can keep its temperature below a maximum allowable operating limit in any possible powering scenario. The main design tools to ensure proper solutions are thermal transient testing and CFD based thermal simulations.

Physical tests are important as they allow direct temperature measurement on the semiconductor die's surface as well as by measuring the step response function, structure functions can be created, which give idea of partial thermal resistances in the heat flow path, and also help to reveal any physical defects in the design and manufacturing phase [1,2]. Measuring the real physical behavior, one can also create a reference to the simulation environment and make sure that the simulation results of a certain package can be the same as the real physical behavior [3].

The answer to these challenges may lie in a combined measurement and simulation approach. Measurements yield a structure description of materials having different conductivities; simulation gives the clue as to what certain sections in the measured structure correspond to. TIM materials are very difficult to model, as neither their conductivity nor their thickness can be determined with high accuracy even by the designer of a given package. Well planned thermal measurements are suitable tools to measure the in-situ resistance of these materials so that they can be later on used for accurate model creation [4].

Having an accurate model is a must if the designer would like to analyze the thermal behavior of the package mounted into a communication device.

# 1.1 Experimental overview

In order to create a procedure for package level characterization, we will follow the thread explained below for the package level characterization:

IC packages with different core arrangements are characterized by thermal transient measurements. The goal of this phase is to measure the effect of the chip design (floor planning) on the thermal properties of the IC and validate the design expectations.

The chips are packaged and mounted on test boards which follow JEDEC JESD51-9 standard requirements [5], so that we can easily determine at which thermal resistance value the package ends and the heat enters the PCB.

The first step is to find a temperature sensitive parameter (TSP) in each core, normally we use the forward Voltage of a substrate diode. The second step is to calibrate the TSP for the desired temperature range. This step requires some further considerations in case of embedded capacitors in a core or IC.

As a final step we measure the step response function of each core and generate structure functions based on the measured data. In this phase, detailed/calibrated numerical device model can be created and calibrated against the system characteristic test data.

# 1.2 Generic test procedure

For thermal transient measurement of real chips in this paper the substrate diode of a CMOS circuit will be used. Reverse-biasing the Vdd and the ground pins the substrate diode will be used as heater and sensor. [6]



Figure 1: CMOS inverter, cross section

The heating current will be applied first to the substrate diode (chain of p and n doped regions between the Vdd and ground pins) until thermal equilibrium is reached, then the heating current will be switched off, and thermal transient response will be recorded under sensor current applied to the substrate diode.

This procedure works in general for every possible CMOS circuit. Some cores are however embedded with capacitors, to suppress supply noise. In such cases sensor current needs to be selected carefully. For sensor current selection, transient time of voltage signals caused by capacitors must be less than initial electrical transient time to ensure no impact on thermal transient response.

# 2 Sample description and measurement results

The SoC sample created by Huawei has three cores, 'Core 1 to 3' embedded onto one silicon die. Core 2 also contains an embedded capacitance which requires us to select to corresponding sensor current carefully.



Figure 2: Tested core arrangement

To find a suitable sensor current value we performed thermal transient measurement on Core 2 with different sensor current values, starting from 5mA and going up to 100mA. The heating current was 2A in each case. The goal of the experiment was to monitor the dependence of the initial electrical transient response after the switching (non-thermal, parasitic signal) on the sensor current level.



Figure 3: Effect of the sensor current on the length of the electric transient response in case of embedded capacitor

As the devices were not calibrated at this stage, the magnitude of the temperature rise looks different in each case which is a normal phenomenon. The length of the initial electric transient can be seen however clearly in the graphs. In case of the lowest sensor current, 5mA, the electric transient is the longest, it lasts up to app. 180 microseconds, while if the sensor current is increased up to 200mA, the electric transient ends below 20 microseconds, which is a significant gain.

Based on this data we selected 200mA sensor current for the measurements, and performed a calibration between 25 °C and 85 °C in 5 °C steps.



Figure 4: K-factor calibration curve corresponding to Core 2

The resulting curve is non-linear due to the capacitance, however it is highly repeatable, so this core also works perfectly as a temperature sensor. In order to make sure that the temperature calculations will be correct, a 3<sup>rd</sup> order polynomial fit was applied on the measured point instead of a linear approximation.

The k-factor values corresponding to the other two cores were linear on a wider range as normally expected from Si

devices, and 100mA sensor current was used only as we did not take into consideration the effect of the embedded capacitor.

# 2.1 Transient measurement data on each core

After successful calibration of each core, thermal transient tests were performed, two tests on each core. In the first test the package was mounted on a 'high conductance' board and in the second test it was mounted on a 'low conductance' board in order to get the junction-to-board thermal resistance for each scenario.

Due to the longer time constants of the test 'low conductance board' test case, the measurement time was set to 600seconds and each test was performed in a still-air chamber environment.

The raw transient data corresponding to Core 1 can be seen in Figure 5. transient



Figure 5: Raw data measured on the Core 1

As Figure 5. indicates, the electrical transient ends before 30 microseconds, from where the curve continues as a clear thermal signal. In order to correct the initial electrical transient we have used a square-root type fit to the beginning of the curve from 260 microseconds, resulting in a good match with the measured data.

Figure 6 shows the structure functions corresponding to each test case performed on the Core 1 fitted on the top of each other.



Figure 6: Core 1, test on high and low conductance boards

The initial part of the two structure functions match well, indicating that the heat flows in the same structure in both cases in a similar package first, before it enters the two different PCB-s. From the point of view of the Core 1 the Rth<sub>JB</sub> is 2.95 K/W. As the initial heat source size of the three cores is different, the Rth<sub>JB</sub> from the point of view of the three individual heat sources will be different, too:



Figure 7:  $Rth_{\ensuremath{\text{JB}}}$  values from the point of view of the different cores

As Figure 7 clearly indicates, depending on the heat source area both the initial thermal capacitance resolved by the structure functions, and the calculated  $Rth_{JB}$  values will be different. The obtained values and the corresponding areas are summarized in Table 1.

Table 1: Rth<sub>JB</sub> values of the different cores

	Summary of each core's characteristics	
	Area [mm <sup>2</sup> ]	Rth <sub>JB</sub> [K/W]
Core 1	21	2.95
Core 2	15.5	3.53
Core 3	9.5	6.26

In order to make sure that the measurements were correct, one can fit the measured curves at the PCB region and, and a good fit will be obtained, which is independent on the initial heatflow area, as Figure 8 suggest. This proves that the calibrations were all correct.



Figure 8: Each measurement from the different cores fitted in the ambient

# 3 Model calibration

### 3.1 Numerical Model

The experimental configuration was modeled using the FloTHERM simulation software. The internal construction of the package was known in details before the characterization, however some sizes and material parameters were not certain. Best guess assumptions were made regarding the thermal conductivity of the substrate beneath the chip, the solder mask layer, the conductivity of the solder bumps and underfill among the bumps.



Figure 9: Overview of SoC device construction

The transient simulation duration was 600s, sufficient to allow the model to thermally transition from the two powered states. 10 time steps were defined per decade, starting from 0s to 1e-6s, increasing in size so as to achieve a smooth transition of time step size between the decades.

Whereas the experimental approach was to set the power to zero after steady state was achieved, the numerical approach was to set the power to 1.799W at time = 0s, this was to aid the ease by which the numerical simulations were conducted. It was confirmed that the resulting SF was identical to the power down numerical equivalent.

The resulting thermal impedance was calculated from the temperature rise in time of the central point of the active layer of the die.

The initial simulation result was quite different from the measured result, the comparison was done in the form of structure functions, as shown below [7,8]:



Figure 10: Initial simulated curve vs. measured data

#### 3.2 Numerical model optimization

As according to Figure 10. the measurement based structure function and the simulation based structure functions were very different from each other, we have decided to use the thermal model calibration feature in FloTHERM to do an optimization. In case of the simulation optimization the Core 1 was heated and compared to the corresponding test data.

The measurement time required for the  $Rth_{JB}$  test was 600 seconds, however it is not efficient to use this entire time span for the model calibration, hence we have checked in the Zth curve the approximate heating time of the package only. In order to reach over the 2.94 K/W surface

(4 K/W was used to have a safety margin), it takes the heat trajectory 0.15 seconds to spread. For this reason, the optimization was carried out up to 0.15 seconds as well.



Figure 11: Region for the optimization, Rth < 4 K/W

The optimization requires a list of the uncertain parameters, and a possible range of the corresponding thermal conductivity values. Based on these scenarios a list of simulation experiments can be created automatically, and each will be solved until convergence. The best fit with the reference measured curve will then be selected by FloTHERM. The benefit of such optimization procedure is that the resulting calibrated thermal model will behave exactly the same way as the real physical device would work for any arbitrary input powering. This gives confidence to the appliance design group that any thermal simulation they make with the calibrated package will result in reliable data.

Table 2: Most important parameter ranges used forcalibration

	Calibrated parameters	
	Minimum [W/mK]	Maximum [W/mK]
Bumps	40	70
Underfill	0.2	0.7
Substrate	10	20
Solder mask	0.5	3

The uncertainty of the parameters does not only come from the thermal conductivity of a given layer itself, the interfacial thermal resistances also play an important role. As we did not model the interfacial thermal resistances individually, the optimized conductivity values are not bulk, but effective conductivity values, characteristic to this package arrangement and technology.



Figure 12: Calibration results in the structure function space (truncated functions based on a 0.15 sec transient)

Figure 12. shows the final calibration result, which is a good match with the measured data until the  $Rth_{JB}$  thermal resistance.

# Summary

In this paper we have shown a methodology to characterize high performance multi-core SoC devices for communication device applications. Thermal transient measurements are capable of obtaining the  $R_{thJB}$  thermal resistance of a package from the point of view of each core separately. This is still true if there is an embedded capacitance in any of the cores, with the selection of a proper sensor current its effect can be eliminated and the electrical transient response can be limited to an acceptable level.

As a second step we have built a simulation model also which was calibrated against the measured data. The thermal parameters of each layer were optimized and as a result of the optimization we got a model which will behave properly for any varying power input. Such model can be later used to for system level thermal analysis of the communication device with high confidence.

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# Methodology to Achieve the Thermal Management of a 6U Conduction-Cooled Board With 130W Power Dissipation and an Operating Temperature of 85°C

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# Abstract

We are presenting a methodology to optimize the design of a thermally challenging Single Board Computer (SBC) in order to achieve ambitious thermal management goals at reasonable cost. The case study presented describes the design of a conduction cooled SBC in 6U-VPX [1] form factor, dissipating up to 130 W (2 high performance CPUs) and presenting a high density of components (ca 4500 on 640cm<sup>2</sup>). In order to achieve high reliability (low MTBF), all components must be operated at least 5°C below their maximum rating, while the board's thermal interface, i.e. the upper and lower board edges, are kept at 85°C. Any "active" cooling (including heat pipes) is prohibited. This puts tight constraints on the allowable temperature gradients between the board edges and any of the thermally critical components. It turns out that a heat frame design based on advanced composite materials (aluminium, copper and graphite) can meet these constraints even in the presence of layout constraints that impose a less-than-optimal placement of thermally critical components.

# **1** Presentation of the case of study

The following briefly explains the main requirements of the project:

- Conduction-cooled means passive cooling, the board is equipped with a heatsink providing a thermal path from components to outer edges of the module
- 6U VPX form-factor [1] determines the allowable surface and a 0.85" pitch limits the allowable height, i.e. the maximum thickness of the heat frame
- Several functions inducing a high quantity of components about 4500
- Final mass lower than 1.2 kilograms
- High processing power (2 Intel® processors and their memories) leading to a high power density
- An edge temperature (also defined as cold temperature) of 85°C
- 5°C of minimum temperature margin for all components

Both last points are very constraining. For example, if we consider one CPU embedded with a maximum temperature rated of  $105^{\circ}$ C and a dissipation power of 37 Watts that means the temperature difference allowed between CPU case and board edge is  $15^{\circ}$ C. So the total thermal resistance allowable in this path must be less than 0.40 °C/W.

# 2 Hypotheses of design

In order to avoid the disastrous consequence of a late redesign, the thermal management of an electronic board must start at the very beginning of a project in parallel with electronics, mechanics and layout. The first task to think about is a model of the board. To keep the complexity of the model within manageable limits, we need to take some simplifying hypotheses.

The board is "conduction-cooled". To simplify simulation the following hypotheses will be taken and validated later:

• No natural convection considered

This hypothesis implies that calculated values will be higher than expected in real test which is acceptable in view of conservative design. The difference will be quantified later by tests. However the time saved will be significant due to the time necessary to solve the Navier-Stokes equations in several numerical tools.

• No radiation

The time saved with this hypothesis is important. Moreover an implicit rule of thermal designer says that below 100°C of temperature difference the radiation part can be neglected without any major impact on the relative uncertainty.

• 2 cases of study, 1 "worst" and 1 "typical"

The "worst case" is defined by using all components dissipation powers at their maximum which, in reality, is never the case.

The "typical case" tries to be closer to reality by reducing the power. For the present study we will consider "typical case" as 70% of the "worst case". • Conduction through the heatsink only

This hypothesis concerns only the components managed by the heatsink. This hypothesis is taken considering the difficulty to have a stackup definition, i.e. the detailed design of the printed circuit board (PCB), available at the beginning of the design phase.

# **3** Specifications of thermal constraints

Thermal engineering provides a list of thermal constraints as inputs of the design process. Below there is a list of constraints applicable to the current project.

- The most critical components shall be as close as possible from edges which are the coldest points of the board. Given that only a relatively fraction of the surface is close to these 2 edges, priorities must be assigned.
- The heatsink will have a gradient of temperature due to the conduction resistance through it. That means the center will be the hottest place and critical components shall be avoided there.
- There are 2 "cold" edges so the power budget shall be distributed on both sides of the board.



The picture above represents the thermally critical components (red rectangles and squares). Both blue transparent surfaces represent privileged place for them, close to the edges so close to the "cold" source. The red transparent surface represent place to avoid, too far from the edges so in front of the highest temperature of the heatsink.

- The distance between two critical components shall be as large as possible to avoid one affecting the other through the heatsink.
- Thermally managed components shall be placed on the PCB's top side where the allowable height is significantly larger than on the bottom side.

Contrary to the "simple wall" model [2] commonly used in the thermal engineering, in this case the cold source is not directly opposite to the hot source but on its side. That means the thickness of the heatsink directly above the component shall be sufficient to allow the complete spreading of the heat. For example, with this board, the pitch requested is 0.85" so the height allowable on top is 14.7 millimetres compared to the height allowable on bottom which is 4 millimetres. As 4mm is more risky than 14.7 millimetres for a good spreading, we shall avoid thermal critical components on bottom.

• The heatsink shall have the highest possible thermal conductivity

There are not a lot of parameters in the Fourier's Law and the thermal conductivity is one the most important. The higher it is, the better will be the conduction performance, it is as simple as that. Below you can find a table compiling the thermal conductivity of different materials commonly used in the industry.

Table 1: List of common isotropic materials for a heatsink[3]

Aluminium 6061-T6	167 W/m.K
Aluminium 6063-T6	200 W/m.K
Aluminium 6101-T6	218 W/m.K
Pure Aluminium	235 W/m.K
Copper Alloy	333 W/m.K
Pure Copper	386 W/m.K

Selection of components and their packaging is also critical to a successful thermal management.

- Every critical component shall be checked by thermal engineering before approval to be used in the design. A bad package may make the thermal management impossible.
- The Thermal Interface Material (TIM) shall be selected carefully. The temperature drop due to it is generally the highest of all the resistance chain. For the present study a thermal pad extremely compressible will be considered.

# 4 Calculations and simulations of the thermal performance during the design phase

Both methods, analytical calculations and finite element simulation (FEM), allow evaluating the impact of conflicting design constraints on the thermal management. For example a thermal constraint, requiring that components shall stay close to edges, and an electric constraint, requiring the opposite, cannot be applied both. Below we describe a typical example of numerical simulations and analytical calculations applied to help solving this kind of issue.

### 4.1 Thermal resistances modelling

Following the hypotheses from section 2, the thermal resistance model for a "thermally-managed-by-the-heatsink-component" is defined below:

With:

$$R_{gt} = R_{jc} + R_{tim} + R_{hs}$$

- R<sub>st</sub> : global thermal resistance
- R<sub>ic</sub> : junction-to-case resistance
- R<sub>tim</sub> : TIM resistance
- R<sub>hs</sub> : conduction resistance through heatsink

We will apply this using one of the two CPUs on our board and will focus on the heatsink study:

- the "junction-to-case" resistance of the processor is below than 0.10°C/W following the datasheet
- power used for the CPU will be 37W in "worst" and 26W in "typical"
- the required global thermal resistance, defined in section 1, is 0.40°C/W in "worst-case" and 0.55°C/W in "typical case"
- the TIM used could provide a thermal resistance of 0.15 °C/W

$$R_{hs} = R_{gt} - R_{jc} - R_{tim}$$

Worst:	Typical:
$R_{\rm hs} = 0.40 - 0.10 - 0.15$	$R_{\rm hs} = 0.55 - 0.10 - 0.15$
$R_{hs} = 0.15 [^{\circ}C/W]$	$R_{hs} = 0.30 [^{\circ}C/W]$

The values above give the resistance allowed for the heatsink in both cases of study. This resistance is difficult to calculate with simple analytical model so FEM will be necessary.

#### 4.2 Simulation and preliminary design of the heatsink

Considering the hypotheses presented in section 2 the thermal performance of the heatsink depends only on the following criteria:

• Power distribution

The power distribution, i.e. the amount of heat injected into the heatsink at any point, depends only on components positioning and results in an update of the heatsink for each iterations.

• Surface available for the heat recovery

This contact surface available for the heat transfer is only determined by component characteristics and shall be the biggest possible to decrease the power density. This is essentially managed during the package selection of components. • Enough thickness for a good spreading

Insufficient thickness could affect significantly the performance. Note the minimum working thickness depends on the material selected.

• Material

It seems obvious, but the thermal conductivity impacts considerably the conduction performance of the heatsink. Firstly isotropic solutions will be considered until they reach their limits. Then new solutions could be applied like hybrid copper/aluminium or graphite/aluminium.

# 5 Comparison between theoretical and practical design of the board

The picture below represents the real positioning of components. The final placement shows significant derivations from the initial proposal, which was motivated by thermal considerations only.



These differences are due to the mitigation work. Numerous thermal constraints were conflicting with others constraints (electrical, mechanical or others). Below we give a list of constraints (mainly electrical) which counteract thermal optimization but are quite common in the electronic industry:

- CPUs, chipset and memories (all critical components) are already grouped in an existing block, type "pick and place", making it impossible to increase the distance between them
- This existing block comes with its stack up preventing to place CPUs on the edges of the board due to the difficulty to route all the wires
- In order to minimize the track length between some critical components and the VPX connectors, these components have been moved closer to the board center.

• The large number of components in the memory block, considered as critical components, makes it impossible to place them only on the PCB top surface.

# 6 Design of the heatsink

As seen in section 4.1, there are thermal resistance values that the heatsink shall reach in order to make the board working. Using this methodology, the main axis of improvement to make the heatsink working, and considering the final design, is to increase its thermal conductivity. Some runs of simulations gave the following results:

- Monolithic aluminium alloy part gives a resulting thermal resistance of 0.80 °C/W
- Monolithic copper alloy is about 0.68 °C/W

In both cases the plain thermal conductivity is not enough to present an acceptable temperature on top of processors due to their positioning close to the centre.

A new solution of heatsink has been simulated and approved. This solution is based on 3 materials: aluminium, copper and graphite.

- Graphite is used to increase the conductivity in the x/y plane up to 1100 W/m.K
- Copper is used as "thermal vias" to boost the thermal conductivity in z-direction
- Aluminium covers everything to bring mechanical coherency

The following picture illustrates the new design.



With this build for all components, except CPUs, the working temperature is significantly lower than the max rated temperature.

Concerning the CPUs the thermal resistance achieved by the heatsink is 0.24 °C/W which is acceptable in "typical case" and not acceptable in "worst case". However this solution has been selected for reasons explained in the next section.

# 7 Comparison between calculated/simulated values and test values for several projects

The methodology has been tested and approved by comparing the calculated values and the measured values.

It shows that "worst case" is really conservative with every values overestimated. However the "typical case" seems to be very close to the reality.



The plot above compares temperatures at selected heat sink locations. Green bars correspond to measured "typical" values, orange bars represent "worst case" values and blue bars represent "typical case".

#### 8 Criticism about the methodology

The methodology has the purpose to simplify the study by developing a model of the complete board focusing purposely on the heatsink.

By considering firstly the "worst case" we try to define a design case very conservative based on "can do more can do less". However this case could lead to oversize the heatsink and it is not going in sense of optimization.

The "typical case" tries to be as close as possible to reality but the deduction selected, i.e. 70%, needs to be validated later by thermal tests. Moreover it is possible to calculate operating power dissipation of numerous components.

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**SESSION 9** 

# **SESSION 9** DELPHI4LED Special Session

# Delphi4LED - From Measurements to Standardized Multi-Domain Compact Models of LED: a new European R&D project for predictive and efficient multi-domain modeling and simulation of LEDs at all integration levels along the SSL supply chain

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#### Abstract

There are a few bottlenecks hampering efficient design of products on different integration levels of the SSL supply chain. One major issue is that data sheet information provided about packaged LEDs is usually insufficient and inconsistent among different LED vendors. Many data such as temperature sensitivity of different light output properties are provided to a limited extent only and usually by means of plots. Also, reported light output properties are typically rated for a junction temperature of 25 °C, which is obviously much below the junction temperature expected under real operating conditions. Even if "hot lumens" measured at a junction temperature of 85 °C this is not the actual operating temperature and there is little information about how such "hot lumen" tests are performed. The gap between and reported LED test data and actual operating conditions can be bridged by proper simulation models of LEDs and their environments. Such models should be accurate, hence capable of proper prediction of LED operation but simple enough to assure fast numerical simulations. However, LED integration do not get access to detailed LED information to perform those simulation at system level, thus perform reverse engineering which is time and cost consuming.

A bridge, in the form of standardization, has to be established between the semiconductor industry and the LED component integrators. In order to achieve this, the following tools have to be provided:

- Generic, multi-domain model of LED chips
- Compact thermal model of the LED chips' environment (including the package and module assembly)

• Modeling interface towards the luminaire

The goal of the project is to develop a standardized method to create multi-domain LED compact models from testing data.

#### Keywords

Electro-thermal-optical characterization, LED compact model, Thermal Transient Measurement, computer simulations

# 1 Introduction

The lighting industry faces a couple of key challenges due to the introduction of LED: faster pace of development, quality performance safety net, growth of the LED industry, commoditization of LED component, to name a few. Technically, the key challenge is linked to the current structure of the value chain and resulting relation between LED supplier and luminaire makers.

Although LEDs are very efficient, and therefore dissipate much less heat than conventional light sources such as incandescent, halogen or high-intensity discharge lamps, their efficiency is dependent on the LED temperature. This temperature depends on how effectively the LED dissipates its power to the surrounding environment, the amount of heat dissipated by the device and the effectiveness of the heat transfer paths inside the LED component. Thermaloptical-electrical parameters are inter-related but incomplete or even erroneous in datasheets of LED suppliers. At luminaire developers, this results in considerable reverse engineering effort to get the proper product information about packaged LED. Ways to do this include material analysis, cross-section analysis, computer simulation and measurements. All these reverse engineering techniques combined lead to reasonable results but result in long development time and waste of money. For example the exact package dimensions and materials properties – properties of the LED chip and phosphors - are unfortunately proprietary information of LED suppliers and cannot be expected to be publicly shared.



Figure 1 - Value chain of LED lighting products

# 2 Value chain and key stakeholders

**Error! Reference source not found.Error! Reference source not found.** shows the typical elements of the value chain in solid-state lighting. It is split into different levels from L1 to L6 where L1 is the LED<sup>1</sup>. (packaged LED chip) and L6 is a complete system, e.g. in a building or in an outdoor application like street-lighting. The value chain belongs to two different industries: to the semiconductor industry (L1) and to the lighting industry (L2-L6). Those two industries are working separately; and exchange of information today is in the form of a paper datasheet, which in many cases is insufficient for the design of a reliable and performant LED system.

# 3 Delphi4LED baseline and beyond state of the art

In order to achieve a good design of LED systems, a modular, multi-physics based modelling approach is needed, including LED package/module thermal models which are boundary condition independent – this way allowing the

freedom for LED luminaire manufacturers to use such models in any kind of luminaire designs.

The multi-physics model couples the thermal, electrical and optical domain.

Over two decades ago, work has been done for such an approach in the conventional semiconductor world, resulting in thermal measurement solutions, thermal modelling and simulation solutions, most of which got standardized. As in digital electronics device operation is less influenced by the actual chip temperature, the need of multi-domain simulation was less pronounced than in case of today's LEDs. Therefore, simply following the pattern from compact thermal modelling approaches determined two decades ago is not sufficient. A new multi-disciplinary approach is required focusing on multi-domain thermaloptical-electrical operation as well as to related reliability issues. The approach is extending the original concepts developed, with multi-domain and multi heat-source aspects.

#### A. Delphi4LED Objectives

The specific technical and exploitation objectives of Delphi4LED are:

	Specific technical objective
1	Define the appropriate characterisation procedures and tools required for generation of compact models of LED components
2	Define the extraction methods of generic, multi- domain models of LEDs (both for colour and phosphor converted white LEDs) from measurements which allows for simultaneous simulation of the LED behaviour in all operating domains, within a single software tool, providing electrical and light output characteristics as well as the dissipation and the junction temperature and other key parts in a consistent way.
3	Offer a standardized data format for exchanging the measurement data and model parameters
4	Integrate the multi-domain models into software for computer aided design, finite element modelling, and computational fluid dynamics based thermal simulators to be used in the development processes.
5	Reduce the physical prototype and experimental effort and cost in the value chain to the absolute minimum.
	Specific exploitation objective
1	Make a proposal for a standardized data format to exchange LED component measuring data and compact models and drive further standardisation in the relevant committees e.g. in JEDEC or in Division 2 of CIE.
2	Implement Delphi4LED methods, models and tools within consortium partners to harvest the benefits in the internal development processes and to ripple on other business sectors
3	Develop extra software tools for model generation and implementation in FEM and CFD packages.
4	Explore new, long-term business opportunities based on cloud services and data analytics e.g. investigate the possibility for a central, cloud-based data storage of LED data and commercialization of it.

Table 1 - Technical and Exploitation objectives of Delphi4LED

<sup>&</sup>lt;sup>1</sup> According to the latest LED product terminology standardized by CIE (see the CIE FDIS 024/E:2015 document) a so called level 0 device, a packaged LED chip is called *LED package*. In the context of the present paper this term would be ambiguous as it would hamper the clear distinction between the actual device level enclosure ("the package") of the light emitting chip ("the LED") and the entire level 0 LED device. In this paper term "LED" means the entire packaged LED chip and the term "package" or "LED package" is used to refer to the level 1 device enclosure of the LED chip.

The vision of the Delphi4LED project is that the above goals will lead to new standards in the solid-state lighting industry: develop a standardized method to create multidomain LED compact models from thermal-opticalelectrical performance data where test data are reported in standardized e-datasheet format, compact models are published in a standard compact model file format. Delphi4LED provides standardized interfaces for information exchange at the different levels of the flow. (Figure 2)

In addition, tooling for design and simulations are to be developed which will be prepared for integration in reliability prediction tools and digital manufacturing environments.



Figure 2 - - Foreseen standard links between LED device suppliers and lighting development engineers

# B. Approach and Methodology

A multi-disciplinary approach is chosen by Delphi4LED to guarantee the uptake by the market of its outcome.

Contrary to the historical approach, the approach chosen by Delphi4LED is to create compact model based on measurement data. The original approach was considering simulations but this requires the geometrical and material detailed information, which in case of LED is not available due to proprietary information.

Today at most SSL companies thermal, optical and electrical measurements are treated in an isolated manner since the practice of different testing teams and labs is not yet adapted to the business changes of the solid-state lighting industry. Though there exists a combined thermal and radiometric/photometric testing solution for LEDs, this is mostly used in the traditional manner, mainly by LED thermal testing teams, due to the lack of appropriate standardized multi-domain testing protocols accepted by the lighting community as well. Measurement based characterizations are completed with computer simulations.

The methodology will be completed by end-user validation at luminaire level. The methodology adopted is devoid of all LED confidential information. The following disciplines and knowledge areas are involved:

Disciplines	Knowledge Area
1. Laboratory testing	Optical
2. In-line testing,	Electrical
3. Simulations,	Thermal metrology
4. Statistical analysis and	Lighting systems
mathematics,	
5. Data reporting,	
6. Computer simulation and	
Engineering.	

#### C. Methodology per key disciplines

#### Ad 1: Laboratory testing

Testing of thermal properties of LED packages initially followed the thermal testing procedures used in the conventional semiconductor industry. About a decade ago it was recognized that neglecting the emitted optical power in the calculation of thermal resistance results in ambiguity [1]. Thermal resistance calculated without considering light emission is smaller than with considering the emitted optical power. As long as the energy conversion efficiency of LEDs was small, the difference was negligible and did not cause much confusion either in market competition or in thermal design. For modern high power and high brightness LEDs the problem had to be solved. In 2012 this lead to the publication of JEDEC's LED thermal testing standards (the JESD51-5x series of documents[2],[3],[4],[5]) in which clear distinction is made between the real thermal resistance of LED packages (where the emitted optical power is considered) and the "electrical only" thermal resistance, calculated solely from the junction temperature rise and the supplied electrical power (which in case of the traditional semiconductor devices is equal to the dissipated power).

Besides the firm definition of the real thermal resistance of LED packages a test procedure was also defined to measure it. Unfortunately these standards still do not require how and to what value the junction temperature of the LED under test should be set during the measurement of the real thermal resistance; only recommendations were given how to identify this temperature value from the test rest results. Using a combined thermal and radiometric (and possibly also photometric) test setup was recommended only, but using a tight coupling was not required by these LED thermal testing standards.

# Ad 2: In-line testing

Thermal testing and precise photometric measurements of LEDs are performed off-line, in dedicated testing labs. Electrical properties along with quick measurements of the light output properties however are performed in production lines. Unfortunately in LED in-line testing so far little attention has been paid to thermal aspects. This problem affects both the measured electrical and photometric properties. From an end-user point of view a major problem of in-line testing is that test results are rated typically to an assumed LED junction temperature of 25 °C which is clearly not the junction temperature that LEDs are operated at under real application conditions. Recently a few LED vendors started publishing "hot lumens" on their datasheets, said to be valid to a junction temperature of 85 °C. There are still problems with these reported "hot lumens":

- It is not known publicly how the junction temperature was set to the rated value during testing
- and the operating junction temperature of an LED could be anything during operation under real application conditions.

These problems seem to be remedied by the publication of the technical reports of the CIE TC2-63 and TC2-64 technical committees which are expected in late 2016 or early 2017. These expected new recommendations regarding optical testing of high power / high brightness LEDs combined with the JESD51-5x series of standards of JEDEC are expected to solve the problem of separately measuring the operating parameters of LEDs.

#### Ad 3: Simulations: Model order reduction and Statistical analysis methods

The approach consists of the following steps: investigate current knowledge and analysis of available data, choose appropriate class of models, set-up and analysis of efficient (lifetime) experiments, derive compact models, verification of outcomes related to multi-domain operation, integrate models, draw conclusions.

# Model order reduction

We envisage a new kind of hierarchical modelling procedure that will augment compact models of the basic (active and passive) devices with connections that will allow interaction with and representation of their environment. Parts of the environment require that local data is computed such that simulation and measurements results must be inserted. In addition, we foresee the need to include new effects that were deemed inconsequential so far but will play a definite role in determining the behaviour of the structures that we intend to model. If we have the compact models with connections, we will subsequently determine the coupling among these elements, and after that, we will message the resulting equivalent models into another model, which is still accurate enough but much simpler.

To reduce the size of the huge systems to be solved, Model Order Reduction methods for coupled problems (cMOR) will be employed. To this end, accurate low rank approximations of the coupling blocks will be made. The size is a problem, in addition to keeping enough sparsity, allowing communication via ports or via equations. Furthermore, the reduced order models will be coupled to each other or to remaining sub-systems within monolithic time iteration in a co-simulation approach. For combining the individual ROMs, it is necessary to include coupling variables and other parameters as symbolic quantities such that the evaluation of the combined ROMs for variations of the parameters (i.e., changing values of the field and possibly also material variables) is made possible at low computational cost. This motivates another focus of the project on the need for methods for parameterized MOR (pMOR), where the preservation of parameters as symbolic quantities in the ROM is essential. And, finally, MOR will have to be able to deal with nonlinear couplings.

We will employ MOR methods that are based both on simulations and on measurements.

# Ad 4: Statistical analysis and mathematics

If measurements are subject to statistical variations, we can interpret the challenge of estimating LED parameters as one of finding the most likely value, e.g. the expected value (to reduce mean square error) or the value with the highest a posteriori probability (to handle ambiguity), conditioned on the measured noisy observations. Mostly we have (forward) models for the measurement imperfections (given a certain parameter value, how is the spread in the measurement), while the above problem is an inverse one. For instance thermal properties such as heat conduction can be calculated from measured junction and other temperatures, but inverting these may lead to "noise enhancement", or amplification of measurement errors. Similarly, electrical properties can be estimated from measured voltages and current at a limited number of places, and calculation of resistances and capacitances or diode properties may be numerically instable. Statistical signal processing provides tools for this. Depending on the number of parameters, and how (combinations of) these can be observed, efficient characterization of LED types, production batches and individual samples can be evaluated, possibly not only in the dedicated labs but also in production lines, each with their own limitations in measurement accuracy.

# Ad 5: Data reporting

Even if characterization of LEDs can be done by LED vendors in a correct and consistent way, there are no recommendations how and what properties of LEDs need to be reported on LED datasheets in an unambiguous, consistent way such, that the published data would allow LED application designers to perform the design work without the need of (partially) re-characterizing the LEDs they want to use and without the need of building different physical prototypes of their final products during the product design and development process. CIE already made their first steps by creating a new technical committee in March 2016 (TC 2-84). Delphi4LED will actively support the work in this new technical committee.

# Ad 6: Computer simulation and Engineering

The present separation of LED testing by operating domain described above is even more characteristic to the design. Thermal, electrical and optical design are also separated, basically because of the lack of the ability of the applied design tools of using a common library of appropriate, consistent, multi-domain simulation models of LEDs. The steps A-C below explain how each of these domains are addressed, step D explains how the three domains are combined.

# A. Thermal: LED package thermal models

It is known that when an exact mechanical-thermal model of the LED with detailed geometry and appropriate materials properties is available, a full finite element model (FEM) of the LED can be created. This model describes the LED thermal behaviour under various thermal boundary conditions and renders a boundary independent representation of the component, which can be integrated in system level calculations. This way the experimental effort for a good system characterization can be considerably reduced, because physical experiments can be to a large extent replaced by computer simulations. The FEM models are unfortunately rather complex and the calibration of e.g. a FEM model is a time and cost intensive effort requiring specific knowledge on the package architecture.

At present, the component characterization therefore happens at two levels of the supply chain, at component suppliers and at component integrators, that wastes both time and money. Besides offering off-the self LEDs, component suppliers are frequently confronted with different customers specifications for their components, because their customers lack a common approach and definition of the relevant key parameters. This also causes a lot of time-consuming and unnecessary alignment efforts. Finally, though detailed FEM models are in principle boundary condition independent, they have normally a lot of degrees of freedom and have huge number nodes. Thus, despite the advances in computer power the number of LED component FEM models, which can be integrated into FEM and CFD based system (luminaire) level simulation is limited.

The story would end here, if it was not known that model order reduction (MOR) techniques enable the compression of large FEM models. Instead of thousands or more nodes, normally a set of 10 - 50 parameters is sufficient to, for instance, describe accurately even the thermal transient behaviour of an LED component. Another beneficial effect of MOR is, that the originally detailed geometric and materials information in the FEM model is encrypted. Likewise, for thermal simulation purposes, the thermal compact models, comprised of a small set of thermal RC network elements are also used. It is not possible to get the full model back from such reduced order models or compact models and in this way it can be guaranteed that no confidential information is lost.

As LED packages need to offer both good heat removal as well as efficient light extraction from LED chips, cooling options are somewhat different from what are used in case of conventional semiconductor devices. Therefore compact modelling methods standard in electronics cooling cannot be directly implemented for LED package compact modelling.

Besides the need for new compact thermal package model concepts, another challenge for Delphi4LED is to investigate whether it is possible to generate the compact models without a detailed mechanical-thermal FEM model.

# B. Electrical: Power dissipation

In thermal only simulations the dissipated power is usually a fixed value associated with the detailed geometry model or a fixed parameter value attached to the thermal compact package model. In case of LEDs the total electrical power consumption can be measured easily, but the light output has to be subtracted from that in order to get the power dissipation. As the junction temperature changes, this heating power would also change. But the junction temperature is calculated from the thermal impedance/resistance and the heating power. To bypass this power dissipation also has to be modelled, consistently with the temperature dependent electrical properties and the light output (emitted optical power).

By using an appropriate thermal-electrical-optical model of the device, the power dissipation and light output can be calculated as a function of the device temperature. This multi-physics nature of the LED operation is depicted in **Error! Reference source not found.**.

As seen in Figure 3, this multi-physics nature has to be modelled for the LED chip only. If such models are available, these models can be further used in module and system level simulations. When combined with the proper thermal model of the LED package and the complete environment of the LED device, thermal calculations on levels along the supply chain will be also correct.



Figure 3 - Multi-domain operation of LEDs and the scope of the project

#### C. Optical: Hot lumens calculations

When a luminaire is designed it has to be assured that it will meet the lighting design specifications under any environmental conditions that it is rated for. At present thermal simulation, luminaire level optical design and final application level lighting design are de-coupled.

To meet the illumination levels required by lighting standards for different application scenarios (such as lighting of roads belonging to different road categories) luminaires are often over-designed. This can be avoided, if in luminaire level design supported by computer simulation, multi-domain LED models are used. This way the actual total luminous flux emitted by each LED of the luminaire at their own, specific junction temperatures is known ("hot lumens") and can be propagated to lighting level design.

# D. Co-simulation of LEDs with their electrical environments

LEDs' electrical operating point is also defined by embedding electrical environment. If the complete system is to be investigated with the surrounding electronics, nonlinear electrical circuit simulation (so called Spice simulation) should be performed. Such a simulation would require an appropriate multi-domain model accounting for the behaviour of the semiconductor chip, completed with the thermal compact network model of the package and the complete thermal environment.

The compact thermal model of the package can be the same as the one used for thermal simulations.

At present no standard, multi-domain Spice-like LED models [6] exist. Such models also need to be developed in a way that their parameters could also be identified from appropriate LED measurements.

Dedicated methods are needed however to generate an appropriate model of the actual physical arrangement of the LED(s) in their actual application environment.

With the above models LED devices with large geometric dimensions like LED filaments or CoB LEDs can also be simulated.

As illustrated in Figure 3, with proper LED package compact models and multi-domain LED chip models the electrical-thermal-optical design space can be fully explored at all levels along the supply chain.

### D. Work package structure

To achieve the overarching goal and the specific objectives of Delphi4LED, the work plan is divided into six work packages as shown in Figure 4: WP0 dedicated to Project management.

The project will be executed in four stages, meant as a cycle to be repeated during the project: Stage 1 represented by WP1, stage 2 by WP2 and WP3 working in close collaboration, stage 3 by WP 4 working closely in a loop with WP2 and WP3, and stage 4 represented by WP5 taking care of the validation and disseminations of the project.



Figure 4 - Work packages of the project with their interactions

#### WP0: Project Management

This WP manages the overall project. This includes management of the consortium, monitoring technical progress, contacts with EC, ensuring project quality.

# WP1: Requirements Specification

WP1 integrates the physical knowledge on semiconductor physics, LED behaviour and light conversion for an appropriate description of the LED component. It contains a comprehensive LED component description exempt from confidential details of the LED architecture and design based on well described measuring procedures.

#### WP2: LED Characterization & validation

WP2 includes adaptation of existing measurement equipment, development of new measurement protocols for combined thermal-electrical-optical assessments. WP2 and WP3 are cooperating to validate the methodology for the compact model creation. Measurement protocols will be documented, verified and the accuracy of the measurements will be estimated.

# WP3: Extraction & Modelling

WP3 in close collaboration with WP2 includes:

• Development of methodology for exploring/optimizing the multi-domain behaviour at system level, including

operating environments appropriate to the needs of module makers or luminaire manufacturers, when compact models are supplied. This phase is assisted by computer simulation like 3D CFD/FEM (commercially available FEM, CAD and CAM packages)

- Development of tools for optimization of the compact models. 3D CFD simulation be used as part of the thermal network extraction by performing computation equivalents of T3Ster type measurement experiments.
- Investigate the qualities of compact model types that may be suitable to characterize the multi-domain behaviour of LED components. This should lead to a standard Compact Model type (standardization) that can easily be communicated between component suppliers and system level manufacturers.
- Development of software module able to accommodate the multi-domain compact LED model. Module to be integrated in commercially available software tools.
- Validate the accuracy and computation speed of fitting the compact models on real data.

The data storage and handling should use open source standards and the format and the metadata used have to be documented, in order to enable also other parties to implement the compact model.

#### WP4: Standardization

The results of the previous work packages must be used to prepare a proposal for an industry standard. The standard comprises the description of the compact models, the measurement techniques and protocol and the procedure to extract the compact model parameters from the measurements. The objective is to propose new CIE and JEDEC standards.

<u>WP5: Implementation, Dissemination, and Exploitation</u> WP5 includes:

- Verification of efficiency and proper use of LED compact model at system level for first time right: LED bulb, a LED module and a LED luminaire. Assessment of system level that is in terms of performance, predictability, and reliability by setting up and analysis of efficient tests (KPI: development time, reduction of material, reduction of cost).
- Test and improve the compact models and optimization tools given the user profiles. Make sure that they are sufficiently robust.
- Verify that the models are easy to use for product development, and also easy to use in an industrial environment.

Proper dissemination of the results includes publications at conferences and journals as well as seminars and courses.

# 4 Conclusions: Expected results and impact

Results and impacts are summarized in Table 2. The multidomain compact model approach will easing the tightly coupled thermal-optically-electrically performance prediction.

It is expected to improve the reliability throughout the whole design and manufacturing process chain: cost of non-quality is expected to be reduced by 25%. When speed and performance bumps are removed, the door can be opened to value-add activities like digitalisation and customization.

Problem	Multi-domain LED compact
addressed	models will

#### ( THERMINIC 2016 – 22<sup>nd</sup> INTERNATIONAL WORKSHOP

on Thermal Investigations of ICs and Systems ))

Erroneous information from LED suppliers and lack of uniformity among suppliers Need for shorter lifecycle and development cost reduction	Enable the <i>standardizing</i> of LED supplier inputs. Standardized <i>e-</i> <i>datasheets</i> will allow describing LEDs in all working conditions consistently. Reduce cost of non-quality and time of product development. It is expected that the development time will be cut by 1/3, development costs will be reduced by 50%, and non-quality costs will be reduced by 25%
Lack of innovative systems and solutions integrating digitalization	Enables <i>digitalization</i> of LED based lighting products. Delphi4LED allows early prediction of the field performance of the final end-user product by integrating LED compact models into prediction tools used for simulation of electronics cooling and simulation of electronics where models of electronic cooling assemblies and electronics component models are already available. Enable smooth integration into the whole <i>digital manufacturing</i> <i>development chain</i> ; Delphi4LED being the first link.

Table 2 - Solutions to identified problem

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## Multi domain modelling of power LEDs based on measured isothermal and transient I-V-L characteristics

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#### Abstract

Recent research has already proved that the characteristics of LED systems can be analyzed creating multi-domain models with tightly coupled electrical, thermal and optical operation. Transient models of the electric and thermal effects have been already successfully established but experimental verification of the dynamic optical behavior was neglected as fast radiometric and photometric measurements have not been available. The present paper outlines two measurement techniques which extend the methodology towards radiometric transients, calibrated by isothermal results. It proposes adequate instrumentation and highlights metrology problems through a measurement example.

#### 1 Introduction

The validation of electronics design has always been composed of two phases: *measurement* and *simulation*.

For this latter one needs *models* describing the objects in a mathematical way and a solver for getting the results.

The *model equations* describe a whole class of objects, and a set of numeric *model parameters* identifies a single instance.

In best case the model equations are based on physical roots instead of behavioral description. We consider the equations and parameters suitable if they are based on a large number of measurements and yield reasonable results in a broad range of realistic *external conditions*.

During the *parameter extraction* the parameters are started with some approximate values and then they are "tuned".

The models are accepted if the measurements and the model simulation carried out in a broad range of relevant conditions correspond without any further fitting.

#### 2 State of art and targets

LED based appliances are mostly used in nearly static applications (e.g. street luminaires) while some applications are rather transient ones (PWM use, LED flash). Moreover, whatever the final use will be, they are tested in the production line just by a short current pulse.

Proper modeling can provide many different advantages. One of them is appropriate support of CAD software calculating the electrical, thermal, and sometimes optical behavior of electronics containing LED components. Another use is relevant comparison of different products from different vendors, if model data are published in data sheets.

The starting point for the present work were the results published in [6][7] and [8]. There the authors created multi-domain models with tightly coupled electrical, thermal and optical operation, then tracked the steady state and transient behavior of the LED system in circuit simulation programs.

The above cited papers made possible verifying the extracted model parameters by comparing measurements and simulated *transient results* in the electric and thermal domain but optical measurements were limited to the "hot" steady state of the device.

In this work now we concentrate on the verification of dynamic parameters by stroboscopic measurements, calibrated by isothermal ones, in all domains.

#### 3 Methodology

The modeling occurs in two consecutive steps. The first is an *isothermal* characterization which yields the steady state radiometric parameters of the LED, and also a portion of the dynamic features in the electric and thermal domain. In the next, *dynamic* characterization step the device is typically placed in a different environment with different thermal boundaries and the optical transient behavior is recorded.





We wanted to elaborate a methodology which can be used as daily practice in a LED manufacturer's laboratory. So we targeted a technique which is relatively fast and needs no special instrumentation.

The actual configuration corresponded to the arrangement of Figure 1. Below we list the instruments which we used:

Mentor Graphics T3Ster 2000/100 thermal tester

Mentor Graphics TeraLED

integrating sphere with cold plate of programmable temperature and radiometric detector

Konica IS CAS140 CT

compact CCD array spectrometer

Mentor Graphics fast calibrator thermostat

Custom built microcontroller based timer

All instruments were used in their native modes, with their standard software. Some tests were carried out using a scripting feature of the thermal tester, which enables programming measurement cycles at a number of voltage / current / temperature points. The TeraLED system offers repetitive current / temperature / optical filter cycles in its standard graphical user interface.

An addition to a standard configuration was a simple microcontroller timer, which produced a given number of TTL level pulses on two outputs. Both T3Ster and CAS140 instruments have an external trigger input [11], but they start their data acquisition with different delay times.

#### 3.2 Isothermal characterization

As already suggested in [6] and [8], as a first step, the core LED element has to be identified in a series of steady state measurements. The dependence of the *static* parameters from the junction temperature and current level can be checked in the arrangement of Figure 2.

This characterization of the LED device occurs at a series of different fixed  $T_{ref}$  cold plate temperatures in the Teraled equipment.

After a prolonged heating period at several heating currents

the  $\Phi_e$  optical energy (radiant flux) is measured in steady state by both the TeraLED static detector and the CAS spectrometer. In such a way we have cross-calibrated values for subsequent measurements.

Then, switching off the LED to low measurement current, electric transients can be recorded. These transients have to be converted into thermal ones through a calibration step, either in an



Figure 3 The multi-domain LED model proposed in [6] (b); with the model of the CAS instrument added (a)

 $\begin{array}{c|c} & \textbf{Thermal} \\ \hline h_{h} & \textbf{Thermal} \\ \textbf{tester} \\ \hline \Delta T_{j}(t) \\ \end{array} \\ \begin{array}{c} \Delta V_{F}(t) \\ \hline \\ \neg \\ \Delta T_{j}(t) \\ \end{array} \\ \begin{array}{c} \textbf{THERMAL} \\ \end{array}$ 

Detector

-

LED

Test LED

Aux

Integrating

sphere

Figure 2 Identification of static model parameters in the thermal and radiometric/photometric test setup

external thermostat or summarizing all transients at different  $T_{ref}$  in the TeraLED software.

The *junction to ambient* thermal resistance of the arrangement is automatically produced by the process, just dividing the *temperature elevation* by the *power*. We can distinguish between  $R_{th\_el}$  electric and  $R_{th\_real}$  real thermal resistance, interpreting the power as the total electric input or the remaining heat after subtracting the emitted radiant flux.

The  $R_{thJC}$  junction to case thermal resistance of the device can be identified by taking two thermal transients with different boundary on the device case, as already proposed in [3] and standardized in [10]. The actual  $T_J$  temperature of the LED junction can be calculated from  $T_{ref}$ , the power and the thermal resistance,  $T_J = P_H \cdot R_{thJC-real} + T_{ref}$ .

With all these data, a *static* model as shown in Figure 3b can be composed. Moreover, the  $R_{th}$  thermal resistance was produced from calibrated thermal *transients*, a compact thermal RC model of the LED package and different cooling mounts can be built up already at this stage (Figure 4).

The actual temperature change will be affected by all elements of the heat conducting path in Figure 4.

Temperature controlled

OPTICAL

fiber to

ELECTRIC

CAS

heat sink

#### 3.3 Transient characterization

For enhancing the model with verified dynamic parameters in the optical domain, we have to acquire the transients of the  $\Phi_e$  radiant flux.

When identifying the model building blocks of Figure 3b, the electric and thermal transients can be captured at a very high sampling rate (above 1 MSample/sec).

However,  $\Phi_e$  cannot be sampled at this rate.

The CAS instrument is precise, at the cost

of operating with an integration method. For getting around the problem we developed two closely related techniques for recording the flux.

#### "Long pulse" technique

The thermal tester is put into waiting state in its control software. The microcontroller timer starts first a heating transient (by trig<sub>2</sub> in Figure 1), high current is applied on the sample for prolonged time.

Then the integration of the flux is started  $(trig_1)$ ; at certain  $t_{gap}$  time pace for  $t_{int}$  integration time. The latency of the CAS system is identified from [11] and from experiments; and is considered when applying the trigger signals.

Figure 5 and Figure 6 illustrate the method, with the *actual current and timing* used in measurements.

After applying 1A heating current  $\Phi_e$  slowly diminishes.



Figure 5 Applied current (I), radiant flux of the LED ( $\Phi_e$ ), and averaged radiant flux from CAS (Mse/t<sub>int</sub>)



Figure 6 Excerpt of Figure 5, the first two pulses, "long pulse" technique



Figure 4 Heat conducting path of a LED assembly

The CAS instrument actually measures the cumulated light energy, but transforms it into average power (Mse/ $t_{int}$  in figures), dividing it by the integration time.

Integration time slots of 20 ms were programmed at 300 ms distance, both very near to the limits of the instrument.

Selecting  $t_{int}$ =20 ms suppresses possible perturbations from the 50 Hz mains ( $t_{int}$ =16.6 ms is recommended for 60 Hz). In Figure 6 we can also observe the waveforms during the integration slot. The measurement with this method is short; a single heating transient time provides all results.

The "long" method cannot be used for times below 300 ms with the given CAS type; and it gives proper time data in the seconds range only.

We showed earlier in [4] that due to the low thermal conductance of typical LED materials a substantial change of the LED temperature occurs already in the millisecond time range, modeling the early behavior of the LED is essential.

#### "Short pulse" technique

In the "short" method the spectrometer is set to a long  $t_{int}$  integration time (minute range). The *thermal tester itself* can be programmed to a set of short current pulses of same  $t_{p1}$  length and amplitude; following each other after  $t_{gap1}$  time.

The series of radiant flux pulses emitted by the sample are integrated by the spectrometer over the  $t_{int}$  integration time.

From the full Mse<sub>1</sub> cumulated energy recorded by the spectrometer and the number of pulses during t<sub>int</sub> the average  $P_{opt\_aver1}$  power of single t<sub>p1</sub> long pulses can be calculated. The D=t<sub>p</sub>/(t<sub>p</sub>+t<sub>gap</sub>) duty cycle is set to 1:100 at least; so that the LED always starts from cool state. With all these we have a reasonable average flux belonging to t<sub>p1</sub> pulse length.

Repeating the whole process with a slightly longer  $t_{p2}$  pulse we gain an Mse<sub>2</sub> cumulated energy for  $t_{p2}$ . We can attribute  $\Phi_e = (Mse_1-Mse_2)/(t_{p2}-t_{p1})$  flux to a  $t_X$  timepoint somewhere between  $t_{p1}$  and  $t_{p2}$ . Lacking knowledge on where the actual flux matches the composed average, we have some jitter in the position of  $t_X$ . Making the difference between  $t_{p1}$  and  $t_{p2}$ smaller we approach the ideal

$$\Phi_{rad}(I_F,t) = \frac{d\overline{\Phi_{rad}}(I_F,t_{on})\cdot t_{on}}{dt_{on}}$$

value, but the numeric noise produced by the subtraction also grows. The technique consumes twice the  $t_{int}$  time for each point, as such it is rather slow. At the moment this is a manually controlled process.



Figure 7 Applied current (I), radiant flux of the LED ( $\Phi_e$ ) and measured integral value of the CAS (Mse)



"short pulse" technique

#### 4 Trial measurements for proof of suitability

Figure 3 and Figure 4 imply an LED model with a single major heat conducting path and a sole "junction" point where the heating energy is supplied. This model can be accurate for monochrome LEDs with a single die.

In case of white LEDs the accuracy of this model is affected by the geometrical position of the phosphor; which converts typically blue light into other spectra and also into heat.

As the proposed tests are time consuming and at the moment only partly automated, it is rational to check the suitability of the model for a specific LED type in a fast way.



Figure 9 Sample LED,  $V_F$  measured at cooling  $\Phi_{short}$  and  $\Phi_{long}$  taken at heating. Not to scale.

In the electric domain the simplest action is producing a transient of the  $V_F$  forward voltage at cooling. In the optical domain a "long time" capture can be done easily (at heating,

to have sufficient signal of course). For having some insight into early behavior a few points can be added in "short pulse" style.

Figure 9 shows the results of such a simplified measurement series on a monochrome red sample. ( $V_F$  as solid green line, points of radiant flux measured by short/long pulse denoted as  $\Phi_{\text{short}}$  and  $\Phi_{\text{long}}$  markers respectively). The work intensive calibration steps were skipped; the curves were just magnified and shifted along the vertical axis. Of course,  $\Phi_{\text{short}}$  and  $\Phi_{\text{long}}$  were processed by the same factors!

We can state that although many effects were not taken into consideration (non-symmetry of heating and cooling at constant current, nonlinearity of the voltage-temperature conversion etc.) the match of the *curvatures* is surprisingly good, which is the minimum requirement for believing in the validity of the proposed model.

#### **5** Actual measurements

We started our experiments on a CREE XQ-E LED sample soldered to a starboard. The data sheet claims that the LED has optimum performance at 350 mA but can withstand 1A, too. We performed the measurements at this highest current.

First, in order to identify the electric and thermal domain of the operation, we calibrated the device in a closed Peltier thermostat. Then we measured cooling transients by the T3Ster instrument at two different boundaries, on a cold plate, and with a paper TIM layer inserted between the device and the cold plate. The resulting Zth curves (thermal transients normalized by the input electric power) are shown in Figure 10. (CP\_el is the temperature change of the LED on cold plate, divided by  $P_{el}$  and TIM\_el is the similar curve with TIM inserted).



Figure 10 Zth curves, LED on cold plate and with TIM layer inserted, normalized by  $P_{el}$  and  $P_{heat}$ 

Then we ran a full TeraLED characterization, in order to make the optical correction of the power and such to get the remaining heating power  $P_{heat}$ .

Figure 11 illustrates the measured flux at several temperature and current values. The cold plate was programmed between 15 °C and 90 °C in 15 °C steps; current levels were applied between 50mA and 1A. At the highest cold plate temperatures the current was kept below 500mA, as the figure suggests we could have destroyed the device reaching its maximum  $T_J = 125$  °C temperature.



Figure 11 Radiant flux of the LED measured at different junction temperature and current

The figure is scaled instead of the actually programmed  $T_{ref}$  cold plate (reference) temperature rather in the  $T_J$  junction temperature, calculated from the thermal resistance which can be read in Figure 10 and Figure 13.



Figure 12 Radiant efficiency,  $\eta = \Phi e / P_{el}$  at different cold plate temperature and current

In Figure 12 we see how the radiant efficiency diminishes at growing forward current, it shrinks from 20% at 300mA to 12% at 1A. With the efficiency values we can recalibrate our curves, from  $P_{el}$  to  $P_{heat}$ .

The thermal tester recorded 3.1W electric power at 1A forward current. With the given efficiency we get 2.7W heating power and 0.37W radiant flux.

#### 6 Model parameter extraction

We can now add optically corrected CP\_opt and TIM\_opt plots to Figure 10, and from the Zth curves we can calculate the structure functions (Figure 13).

From the curves normalized on  $P_{heat}$  we can identify the RC ladder of Figure 4.



Figure 13 Structure functions, LED on cold plate and with TIM layer inserted, normalized by  $P_{el}$  and  $P_{heat}$ 

The junction to case thermal resistance is approximately 21.5 K/W, as we can deduce in the spirit of [10]. After this point we can construct the model of the cooling mount.

When making the structure functions also a Spice like transient compact model can be automatically generated. For example, the five generated ladder elements represented by dot-dash in Figure 13 :

.SUBCKT LADDER 1 0							
C0	1	0	8.782e-5	R0	1	2	5.051e-2
C1	2	0	9.471e-5	R1	2	3	3.364
C2	3	0	2.076e-3	R2	3	4	2.236
C3	4	0	7.804e-3	R3	4	5	1.011e+1
C4	5	0	2.104e-2	R4	5	0	5.230
.EN	DS I	LADI	DER				

When constructing the internal LED model of Figure 3b we followed the guidelines of [6] (or [5]). We attempted to find "best fit" parameters for an ELDO simulation. The parameters were "tuned" on steady state TeraLED results, but in the next section they will be verified on transients.

As the volume of the present paper does not allow details we just summarize the parameters identified from the measurements of the previous section:

 Table 1
 ELDO parameters of the LED model (at 25 oC)

Name of the parameter	sign [6]	sign ELDO	radiant diode	dissipative diode
Ideality factor	т	Ν	7.622	4.629
Current coeff.	I <sub>0</sub>	10	1.747E-08	3.643E-12
Current exponent	p¡∕m	XTI	6.1659	10.585
Bandgap	Wg	Eg	2.4	416
Series resistance	Rs	R	0.2	235
Thermal coeff. Rs	S <sub>RS</sub>	TC1	-1.42E-03	

The numbers belonging to a "good fit" are rather far from our expectations learned from physics. The model will be behavioral type.

#### 7 Simulation results compared to measurements

The chart in Figure 14 compares the measured thermal (heating) transients to the simulated ones, with both cold plate and TIM boundaries.



Figure 14 Comparison of measured and simulated heating transients, CP and TIM boundary

The simulated curves were shifted up by 3  $^{\circ}$ C for easy comparison. Taking into consideration the ~100  $^{\circ}$ C temperature excursion this is a small difference.

The fit is good from 10 ms, the model performs poorer at early times. The transient tester also recorded the actual trigger signal trig<sub>1</sub>.



Figure 15 Comparison of "long pulse" measurements with simulated flux transients, CP and TIM boundary,

Figure 15 compares the transients of  $\Phi_e$  during heating at both boundaries. Results of the "long pulse" measurement technique are shown. As indicated before, for the first few points the position along the time axis is questionable.

The simulated curves were shifted down by 10 mW for easy comparison. Taking into consideration the ~400 mW optical power this is again a small difference.

#### 8 Conclusions

Although existing methods were capable to establish LED models in electric / thermal / optical domain, the experimental verification of this latter was not realized.

We created two techniques for capturing optical transients by array spectrometer, a "long pulse" method for the seconds and minutes range and a "short pulse" method for the millisecond range.

The "long pulse" method is automated and can be carried out during a single transient; the "short pulse" method needs many repeated transients and suffers from some noise.

The accuracy of the models generated from transients in all domains is high in the seconds range. Below it needs further improvement.

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#### LED module multi-physic approach

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#### Abstract

Since the start of the Ledification of lighting systems, the multi-physic "optical, electrical, thermal" characterization of LED light sources is a critical task in Philips Lighting. Dedicated teams are responsible for determining multi-physic models and design-in rules of LED modules which will be later integrated in luminaires (lighting systems). Recent works have focus on generating more and more accurate LED Module multi-physics models. These models have been used to predict and guaranty the performance, reliability and safety of the developed luminaires. In this paper, recent results regarding multi-physics models are exposed. The evolution of the test methods and equipment is discussed highlighting the major challenges in the definition of "boundary independent" LED modules models. In addition, an inter laboratory comparison has been conducted on T3ster equipment. The comparison outcomes have been gathered to provide a non-exhaustive, but useful identification of discrepancies root causes and sources of uncertainty. In this paper some guidelines will be provided to limit them.

#### 1 Background

#### 1.1 Model generation

The key aspects for a massive adoption of LED lighting are an increase of performances, a decrease of energy consumption linked together with a better efficiency and a better reliability. Since few years, new LED based products are also filling the gap regarding light quality and are offering new embedded functionalities such as connected lighting, coded light or tuneable colours.

This status induce new requirements regarding LED modules characterization. Indeed new challenges appears with new architectures. Consequently, characterization processes need to be continuously adapted and improved.

Due to the strong correlation between optical, electrical and thermal parameters, the multi-physic approach for the LED based light source characterization appears to be mandatory. The considered characterization process was designed and optimized to extract all the information needed to ensure the LED light source integration. The quality of LED module implementation is ensured by a set of integration rules and can be validated through photometrical coupled with temperature measurements. Module temperature is measured on a dedicated and easily accessed location defined during the led module design. The balance between easiness for implementation and robustness of the correlation between this temperature and led module performances is crucial and will be discussed in the thermal characterization part of this paper. In the next parts of this paper, the definition of the test plan, its implementation as well as the links between the physical domains (optical, electrical, and thermal) will be described.

#### 1.2 Application case

The second part of the paper will focus on led module thermal measurements. Those measurements, mainly based on contact and radiation thermometry are also performed using a method coming from the semiconductor industry. This so-called "transient method" is performed using the T3STER equipment from Micred®.

Cross laboratory measurements have been performed in order to strengthen knowledge and confidence in interpretation of transient measurement results. T3STER cross measurements have been performed between French (Miribel) and Eindhoven High Tech campus laboratories. Cross measurements have been dedicated to "High density Chip-onboard" architecture which has been identified as one of the most challenging for many thermal aspects and one of the most demanding for transient testing. The comparison outcomes are used as an application cases for the extraction of thermal data presented in the "thermal characterization" part.

#### 2 Opto-electrical characterization

#### 2.1 methodology

Accurate and reliable LED data are critical in LED based luminaire design. As a consequence, when designing an LED module which can be used on an entire range of driving current and temperature the LED used as to be fully characterized and modelled. Such models allow product architects to precisely design the systems to meet the right performances such as product efficiency or lumen level. This modelling as to be proceed on the three main characteristics of opto-electronic components: optical, electrical and thermal parameters. Optical parameters discussed in this paper are directly linked to optical performances and not to optical distribution and emission patterns which are used in the design of optical systems. Optical performances of the LED include, flux (in lumen), optical power (in W), colour temperature (CCT), colour rendering index (CRI) and colour point. In this paper, electrical performances will focus on the forward voltage behaviour. The objective of this approach is to model these optical and electrical performances on the entire application range (driving current and temperature).

#### 2.2 Implementation

Opto-electrical characterizations are performed within an integrating sphere in DC continuous conditions. This has been chosen over pulse measurements as it is similar to application conditions. Additionally, in pulse condition the junction temperature is assumed to be similar to the setup temperature. Internal studies have shown that this statement depends upon the pulse configuration used (duration, number of pulses etc.) and is only valid for short pulse duration. However, characteristics in junction temperature are needed especially when comparing results with measurement from LED suppliers. The method to calculate junction temperature based opto-electrical model using DC continuous and thermal measurements will be discussed in the last part of this paper.

Studied LEDs are mounted on MCPCB test boards. In order to get a better statistical representation of the models, minimum of eight samples are measured. By characterizing this amount of samples, the impact of the distribution in production of the different LED parameters is reduced. The samples are mounted on a regulated temperature control device in order to precisely achieve the targeted reference temperature.

In order to build a proper model, a minimum of three driving currents combined with three temperatures is used. Extrapolation of LED behaviour is not considered and the interpolated model as to cover the entire application range of the LED. As a consequence, the three reference temperatures are defined as the minimum and maximal application temperatures as well as an additional temperature between these two. In most cases, reference temperatures used are 25°C, 90°C and 55°C. Test currents are defined according to the mission profile of the developed luminaires. Mandatory test currents are maximal and minimal currents as well as binning current as it is a reference point for the LED manufacturer. According to the mission profile, especially when the driving current range is large (e.g. applications when dimming of the LED is required) additional test currents can be performed in order to improve modelling.

#### 2.3 Tests results fitting

Results of the minimum nine conditions of measurement for the different opto-electrical parameters described above can 2 thus be fitted to assess the behavior of the LED on the entire application range. Different fitting equations can be used from purely analytical equation to physical one. In this method, a physical model is used for the flux in which the droop and the hot cold factors as well as their dependencies with both current and temperature are considered. In another hand, color parameters as well as CCT and CRI are fitted using analytical models. An example of the obtained surface for luminous flux and forward voltage are displayed in figure



Figure 1: (a) Luminous flux model and (b) Forward Voltage model for a 2mm<sup>2</sup> High Power LED

Using this information in combination with the other characterization steps described in this paper, development teams can design the luminaire with the needed information such as lm/W and lm/\$ over conditions of application.

#### **3** Thermal characterization

#### 3.1 Introduction

The reference temperature for LED multi-physic model must be correlated with the junction temperature. This correlation shouldn't vary with LED module configuration. Thus, an external point from the LED package is not appropriate. As it's not located in the main heat flux path its correlation with junction temperature and with others model parameters (Vf, current, lm, radiant) is depending on module configuration (PCB substrate and contact thermal performances, copper pattern and thickness).

The parallel can be made with the semiconductor industry were thermal characterization parameters, generally named  $\Psi$  are used. They have the units °C/W but are mathematical constructs rather than thermal resistances because not all of the heating power flows through the exposed case surface [1]. However for practical reasons an external point from the LED package named here T\_Ref is used during opto-electrical characterizations and by Led module integrators.



Figure 2: LED solder footprint example

A thermal characterization of the LED module is performed for the given PCB substrate, thermal interface material and coupling method (PCB configuration). This allows to generate a thermal model of the module (correlated with  $T_Ref$ ) and generate a LED Multiphysics model "configuration-proof" correlated with the junction temperature.



3.2 Measurement set-up

 $T_j$ : Junction temperature, is measured with T3ster equipment  $T_{th\,pad}$ : Hottest temperature of the LED solder, is extracted from T3ster cumulative and derivative structure function interpretation and  $T_{th\,pad}$  to  $T_{Ref}$  cross-checked with CFD simulation

3

 $T_p = T_{Ref}$ : Reference temperature point for opto-elctrical characterization and integrator, is measured with thermocouple (type K, awg40)

 $T_{Heatsink}$ : Heatsink temperature, is considered equal with  $T_{medals}$  as the medals is made of high conductive material. It's measured with a PT100 sensor appropriate with temperature range and repeatability constraints.

In addition, Infrared camera is used to measure gradient between LEDs. All correlations are then given for average and maximum LED temperature.

#### 3.3 Test conditions definition

Expected correlations between gradient observed (DT) and thermal power (Pth) are linear and should intersect [Pth,DT]= (0, 0). Thus only one operating point is necessary to generate theses correlations. However in order to assess its quality, several testing points are proposed. Three to four currents are tested to perform a regression analysis (which includes the maximum operating point). This operation is repeated with a re-implementation of the LED module and if possible with a second LED module for repeatability analysis. The board temperature is then regulated close to ambient temperature in order to avoid heat losses on the front side of the PCB. To assess, sensibility of correlation with this behaviour, an additional high temperature low current point is also tested. Finally, an additional point is tested with different contact performances. This allows, to better interpreted T3ster structure function as well as evaluate robustness of T<sub>i</sub> to T<sub>Ref</sub> correlation with implementation conditions. A generic example of performed test plan is presented in Table 1.

Test n°	Led module n°	Current	Cold Plate temperature	TIM
1 -4	1	4 different	Close to	Representative
		currents	ambient	with
5		Reference	Higher than	application
		current	ambient	
6		Reference current	Close to ambient	TIM X
7-10	2	4 different	Close to	Representative
		currents	ambient	with
				application

Table 2: test plan example

#### 3.4 Thermal resistances extractions

The main uncertainty for thermal resistance calculation is coming from thermometry. PT100 sensor used and thermocouple type K uncertainty can be considered constant in the measurement range  $+30 - +100^{\circ}$ C. Then a basic

Figure 3: measurement set-up description

regression (no weight) can be applied. As the expected correlation are thermal resistances, regression should be made on  $DT = \beta 1^*$  Pth for all correlations;  $\beta 1$  being the estimated thermal resistance or thermal correlation. In practice a  $\beta 2$  factor such as  $DT = \beta 1^*$  Pth +  $\beta 2$  will be introduced and discuss in the application case. An analysis of the residues allow to validate the overall process.

#### 4 Application case

#### 4.1 Purpose

As mentioned in §1.2 measurements where performed to strengthen our interpretation ability of thermal characterization and being more specific, about transient measurements. Decision was taken to focus on the responses and uncertainty discrepancies induced by the implementation and the measurement facilities particularities. In this chapter the impact of the sensor used to determine the various temperature of interest will be discussed. Quality of the thermal resistance model will also take place. Some questions will raise regarding structure function analysis and the gap remaining to obtain a boundary independent modelling from those measurements.

#### 4.2 Test samples :

Today, one of the most demanding LED architecture for Thermal measurement is high density chip on board (*HD CoB*).

*HD CoB (Figure4)*, used in retail lighting allow high lumen package in small footprint LED module. Several blue emitting chips are glued with high spatial density on a silver layered aluminium substrate. Chips are wire bonded together, connected to a metal ring and embedded in a silicon based luminophore.



Figure 4: High density chip on board schematics

This intensify a problematic already encountered with existing led module using packaged LEDs. The limited access to the discrete heat sources, leads to challenging situation in the evaluation of the temperatures of interest. The high flux density in the conversion layer and the thermal gradient from the center to the side of the Light emitting surface is also part of the challenges to face during the thermal characterization. As a consequence we decided to perform the application case on this specific type of LED source.

Three samples from the same manufacturing batch were measured in two facilities (*called F1 & F2*).

#### 4.3 Measurement facilities

We decided to focus on the implementation and hardware impact by keeping the same sample on the same mechanical assembly in each laboratory. The implementation on each laboratory was done by the same person. *Figure 5* show the commonality and particularities on the sample side and *table 2* on the instrument side. The definition given in §3.2 are still valid.



*Figure 5: measurement set-up and temperature of interest description.* 

	F1	F2
T3STER model	2000/100	2000/100
Software version	Control : 1.1c Master : 2.2	Control : 1.4.3.0 Master : 2.4
Booster version	BO2008/BH10V90	2014/HPWR 2.0
thermostat	Julabo CF41	Lauda RP855
Temp. control sensor	PRT 100 Ohm in cold plate	PRT 100 Ohm In bath
Cold plate	6 pass 305 mm x 178 mm	Flat tube, 2"x 2,25"
T <sub>medals</sub> sensor	Type k thermocouple	PRT 100 Ohm
T <sub>p</sub> sensor	Type k thermocouple	Type k thermocouple
Data logger	Fluke Hydra 2620A	Agilent 34972 A

 Table 2: hardware differences between facility 1 & 2

#### 4.4 Tests conditions

The tests plan described in table 3 was performed on the three samples in both facilities. The data extraction process from the measurements is according to the description done in  $\S3.4$ . The outcomes of the measurement are the thermal resistances described in *figure 6*.

Test	Current	Cold Plate temperature	TIM
K factor calibration	10 mA	25-85°C	
1	225	60°C	High end Phase change material
2	450	60°C	
3	700	60°C	
4	450	60°C	Gap pad

*Table 3: test plan* 



Figure 6: thermal resistances definition.

Those thermal resistances and correlations are part of the required data for a proper integration of the light source within a luminaire. Measured data are all processed by F1. Structure functions fitting is done on the first high capacitance after chip attached. Individual k factor is considered for each sample. Smoothed responses are used to determine junction temperatures. The junction temperature extracted from transient measurement is determined from the forward voltage of the LED module and not from individual chip. As a consequence the junction temperatures discussed in this chapter can be considered as averaged. Structure function and temperature gradients are compared. Discrepancies and associated root causes are studied and prioritized

#### 4.5 Results

Regression is made on  $DT=\beta 1*$  Pth +  $\beta 2$  for all correlations described in *figure 6*.  $\beta 1$  being the estimated thermal resistance or thermal correlation. Regression is calculated from measurement; F1 is compared to F2 and then to the global regression.



Table 4: regression factors summary



Figure 7: T<sub>p</sub>-T<sub>heatsink</sub> regressions

*Figure* 7 show significant discrepancies for confidence interval magnitude between F1 and F2. This was mainly due to the better reproducibility of the PRT compare to the thermocouple for  $T_{heatsink}$  measurement. The small temperature gradient between  $T_p$  and  $T_{heatsink}$  is due to the localization of  $T_p$  outside of the main heat path.



Figure 8: Tj-Tp regressions

*Figure 8* show the differences observed on regressions for F2 including or not sample1. The regressions are dedicated to the determination of  $T_j$  to  $T_p$  correlation. A regression  $DT=\beta1*Pth$  would lead to residues dependant with P\_PCB Heat, showing that the function is not appropriate. It is supposed that  $\beta 2$  can be associated with systematic error

such as thermocouple attachment ( $T_p$ ,  $T_{medals}$ ) or  $T_{medals}$  to  $T_{heatsink}$  gradient. This parameter is then used for the regression but no in the communicated value for integration. We can observed a difference between samples 1 and the two others. T3ster is used to determine if this is due to the sample or to repeatability aspects.



Figure 9: structure functions sample 1

Figure 9 show the structure function and associated derivative function observed for sample 1. The agreement between both facilities is noticeable. Some discrepancy appear in the early transient area. Those discrepancies can be due to the hardware switch behaviour variation between F1 and F2 coupled with the initial transient correction. As this area as a lower impact after fitting the curves together. The fitting effect won't be discussed in this paper. The curvature differences observed just before the high capacitance area is due to the set up differences illustrated in figure 5. The TIM 2 and cold plate layer for F2 has a longer heat path due to mechanical handling. The agreement observed for sample 1 was also observed for the two other samples. Significant thermal performance difference was observed from sample 1 to the other (figure10). This observation combined with figure 8 shows that the proposed measurements are more repeatable than sample to sample differences. Residues observed for similar sample fitting is less than ±1°C which is satisfying for LED integrations.



Figure 10: structure function sample 1,2 and 3

#### 5 Conclusion and discussions

This study proposed a methodology for LED multi-physic model creation. The model, "configuration-proof" can be used for different luminaire integrations, allowing optimization at system level.

The particular focus on thermal characterization showed a satisfying match for two different T3ster equipment. The equipment have been also used in order to detect samples and set-up differences. It's particularly appreciable in an industrial environment were a large amount of samples are rarely measured. A linear correlation have been identified as better fitting than expected thermal resistance. DT=  $\beta$ 1\* Pth +  $\beta$ 2 is used for thermal resistance determination ( $\beta$ 1),  $\beta$ 2 is supposed linked with systematic error but need to be further studied. Finally, ccontact thermometry have been identified as one of the 1<sup>st</sup> source of uncertainty in the determination of correlation for LED module integration. PT100 sensor have then been preconized for heat-sink measurement over the more widespread type-k thermocouples.

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#### Investigation of the Temperature-Dependent Heat Path of an LED Module by Thermal Simulation and Design of Experiments

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#### Abstract

One key aspect in light emitting diode (LED) systems engineering lies in the understanding and management of the heat transfer during device operation. A deeper understanding of the thermal behavior of an LED module can be gained by an in-depth thermal path analysis. The three-dimensional heat path of the LED is influenced by its operating conditions (e.g. heat sink temperature, driving current, the properties of the thermal interface materials of the device attachment to the heatsink). In this paper, different operating conditions were systematically varied in a set of experiments and its corresponding numerical simulations making use of a statistical Design of Experiments (DOE) approach. The operating conditions were treated as experimental factors of the DOE and the responses were derived from analyzing the resulting structure functions. The results quantified not only the sensitivities of the responses (thermal transients) to the operating conditions but also showed the influence of temperature dependencies in the material properties on the thermal behavior of an LED module.

#### 1. Introduction

The knowledge of the heat transport within an LED module, away from the junction downwards through all layers into the heat sink, is in the main focus of LED thermal engineering. The so-called structure function, calculated from thermal transient data, offers a method of analyzing the thermal properties of an LED and further information about reliability and quality assurance [1][2][3]. The structure function provides a map of cumulative thermal capacitances ( $C_{th}$ ) with respect to thermal resistances ( $R_{th}$ ) along the heat flow path, starting from junction to the ambient (see Figure 1). All essential structural changes in the heat flow path of LED are reflected by the structure function [4].



Figure 1: Schematic of the structure function and its alternative representation as a thermal  $R_{th}C_{th}$ -network. The heat flow starts at the driving point and ends up at the ambient. Each region (dotted lines) in the structure function can be assigned to an  $R_{th}C_{th}$ -pair.

In this work the thermal behavior of the device with respect to a set of different operating conditions was analyzed (see chapter 3.3). Therefore, the combination of the experiment and simulation was used to interpret the structure function. The temperature dependence of the material's thermal conductivities were implemented in the simulation describing the operating conditions' influences of the measured structure functions.

#### 2. Theoretical background

The  $R_{th}C_{th}$ -model, which is provided by the structure function, is assumed to be linear, that means all  $R_{th}C_{th}$ elements are considered to be temperature independent. As shown in [5] the assumption of linearity of the  $R_{th}C_{th}$ -model should be treated with care, if the device is driven in a broad temperature range. Due to the fact that the thermal resistance is not only the change of temperature ( $\Delta T$ ) divided by the heating power ( $P_H$ ), but also inverse proportional to the thermal conductivity (see equation 1), it can also be considered as a temperature dependent parameter. The geometry (the thickness  $\Delta x$  and the cross section A of a material) does not influence the non-linearity of the temperature depended thermal conductivity.

$$\frac{\Delta T}{P_H} = R_{th}(T) = \frac{\Delta x}{\lambda(T) A} \tag{1}$$

The most important source of this non-linearity effect is that the thermal conductivity ( $\lambda$ ) is dependent on temperature. The temperature dependency can be described by a simple power law, which is valid for the temperature range of 300 K to 800 K [6]: on Thermal Investigations of ICs and Systems ]]

$$\lambda(T) = \lambda_{300K} \left(\frac{T}{300K}\right)^{-\alpha} \tag{2}$$

The thermal conductivity at 300 K ( $\lambda_{300K}$ ) and the exponent  $\alpha$ , which is called coefficient of temperature dependency is a material property. Hence, the equation of the temperature-dependent thermal resistance is:

$$R_{th}(T) = R_{th_{300K}} \left(\frac{T}{300K}\right)^{\alpha}$$
(3)

#### 3. Experiment

#### 3.1. Test setup

The investigated device was a blue LED-module consisting of 4 blue LED chips, connected in serial. Therefore, the calculated structure function had to be considered as result of all four diodes.

The device was investigated thermally according to the JEDEC JESD 51-1 standard [7] with the T3ster measurement setup, and optically within an integrating sphere complying the CIE 127-2007 [8]. The LED was measured electrically by the thermal test setup (T3Ster from Mentor Graphics), whose output is the change of diode's forwards voltage V<sub>F</sub> as an answer of the current step from forward current IF to measurement current. The measurement current of all conducted experiments was 10 mA, the forward current was varied according to a DOE design (see chapter 3.3.).The forward voltage can be transformed into temperature values of the diode by a calibration procedure applying different heat sink temperatures. Hence, the output of the electrical measurement resulted in a thermal transient. The thermal transient is the cooling of device over time. Starting from this thermal transient, the structure function can be calculated by the setup's software (T3ster Master) [9]. All further analysis were based on the structure function.

The light output of the LED was recorded when the module was driven by the forward current at thermal equilibrium according to [8], to obtain the emitted optical power  $P_{opt}$ . The calculation of heating power  $P_H$  is shown in equation 4. The electrical power  $P_{elec}$  is the product of the forward voltage  $V_F$  and the operating current  $I_F$  of the diode.

$$P_H = I_F * V_F - P_{opt} = P_{elec} - P_{opt}$$
(4)

During the thermal transient measurements with the T3ster, the LED module was attached to the temperature controlled stage (heat sink). An active cooling plate connected to the refrigerated and heating circulator, "Julabo - F25", acted as a heat sink. According to the datasheet the cooling capacity of the heat sink is 260 W at 20°C. Here, the maximum power applying to the LED was 5 W, so the used heat sink ensures a sufficient cooling. The stabilization of temperature was controlled by the heat sink over the whole duration of the measurement.



Figure 2: Schematic diagram of the experimental setup of the LED

#### 3.2. Noise of measurement

In general, the mathematical transformation of the structure function is very sensitive to the quality of the recorded thermal transient. Thus the measurement of the thermal transient was repeated five times and averaged for noise reduction. The construction of the structure function for all single measured curves can also provide an estimation of standard deviation of the further calculation.

#### **3.3.** Design of experiment

In this study the design of experiment (DOE) approach was used to investigate effects of the device's behavior to a set of variations in its application conditions. [10]. The varied parameters of the DOE (see Figure 2) comprised the temperature of the heat sink ( $T_{HS}$ ), the forward current I<sub>F</sub>, two different thermal interface materials (TIM) attaching the LED-module to the heat sink, the correction of the electrical transient (Trans-Correction) and the time range of heating and cooling ( $t_{meas}$ ) steps. The measurement conditions according to the DOE are shown in Table 1.

Table 1: Parameters and levels of experiment

<i>I</i> <sub><i>f</i></sub>	Forward Current
$T_{HS}$	Temperature of the heat sink
<i>TIM</i>	Thermal Interface Materials
Trans-Correction	ndifferent analytical corrections of the
	electrical transient appearing in the first $\mu$ s of
	the measurement
tmeas	time range of heating and cooling

Europeinsontol Easter	Level			
Experimental racio	Low	High		
$I_F / mA$	350	500		
T <sub>HS</sub> / °C	25	60		
TIM	Thormal pasto	Ceramic plate		
1 11v1	Thermai paste	and paste		
Trans-Correction	Min. seek	Square root		
t <sub>meas</sub> / s	120	200		

These five operating conditions were the experimental factors of the DOE. Two levels of each experimental factor were used in the realization of the DOE (see Table 1). All possible combinations were investigated, meaning that a full factorial DOE was performed. This means  $2^5$  (=32) experiments were carried out. Exploiting the full factorial design obtained an understanding of the parameters, which mainly influenced the thermal properties. The responses of the DOE were derived from analyzing the resulting structure functions. Figure 3 shows a structure function of one measurement (500mA I<sub>F</sub>, 25°C *T<sub>HS</sub>*, Thermal paste as TIM,

2

Minimum seek as electrical transient correction and 200s  $t_{meas}$ ). The numbered  $R_{th}$  and  $C_{th}$  values mark the regions of a changing gradient in the structure function. The d $R_{th}$  represents the difference between two neighboring  $R_{th}s$ .



Figure 3: Schematic of investigated structure function's parameter (500 mA I<sub>F</sub>, 25°C T<sub>HS</sub>, Thermal paste as TIM, Minimum seek as electrical transient correction and 200s  $t_{meas}$ )





The analysis of the DOE offered the possibility to discover the influencing factor of each response. Regarding the thermal resistances ( $R_{th}$ 1-  $R_{th}$ 4, total  $R_{th}$ ) as the DOE's output, the  $T_{HS}$  had more influence on them than the other operating conditions. The effect of  $T_{HS}$  can be clearly seen in Figure 4 and additionally in Figure 5, comparing measurement with different  $T_{HS}$ . According to the DOE's result the  $T_{HS}$ 's shift (from 25°C to 60°C) caused a reduction of the  $R_{th}$ 2 -  $R_{th}$ 4 from ~0.5 K/W to ~0.9 K/W. Just  $R_{th}$ 1 presented an exception, the Trans-Correction had an impact on that parameter too. The minimum seek correction affected a smaller resistance than one with the square root extrapolation (further information in chapter 4.2.).



Figure 5: Comparison of two measurement (500 mA  $I_{fs}$  Thermal paste as TIM, Minimum seek as electrical transient correction, 120 s  $t_{meas}$ ) with different heat sink temperatures (blue line:  $T_{HS} = 60^{\circ}$ C, orange line:  $T_{HS} = 25^{\circ}$ C)

The  $T_{HS}$ 's influence is also reflected in the investigated dR<sub>th</sub>s, representing the difference between two neighboring R<sub>th</sub>s. The dR<sub>th</sub>'s changes are related to the heat sink temperature and they are shown in Figure 6. It is valid for all thermal resistances (Rth/dRth) that the higher the temperature the lower the thermal resistance. The variation of T<sub>HS</sub> caused a dR<sub>th</sub>1 change of around 0.43 K/W, which is a difference of 15% of the absolute value of the  $dR_{th}1$  average. This would mean 1.3°C less temperature distinction at 350 mA I<sub>F</sub> (see equation 1). Assuming that this effect wasn't caused by measurement fluctuation, but by the thermal conductivities' temperature dependencies of the materials within this measured LED module. Since the structure function is the heat-flow map of the device, dRths in the function are assigned to specific layers/materials in the module. Hence, the dR<sub>th</sub>1 change indicated that materials near the heat source had temperature-dependent properties.



Figure 6: Graphic of the temperature of heat sink effecting dR<sub>th</sub>1-4

Regarding the thermal capacitances, the evaluation revealed no statistically significant relationship with the experimental factors. This DOE methodology can be used to investigate any similar system in an effective way.

#### 4. Simulation

Further information about the thermal behavior of an LED module was gained by a thermal path analysis. This was performed by a finite volume simulation (FloTherm), which served as an analysis' supplement [11]. Comparing the experimental and simulated structure functions allowed verifying thermal models. Furthermore, the temperature

dependencies of material's thermal conductivities as provided in equation 2 was implemented in the simulation.

#### 4.1. Thermal modelling

In this work we investigated the three dimensional temperature distributions within the LED module. The simulation was based on a geometrical model, in which each structure element is characterized by a set of material properties (density, thermal conductivity, specific heat). The LED module consisted of four flip-chip LEDs connected (mechanical and electrical) through standard solder joints (SAC soldering) on a FR4 with a partly integrated copper based PCB (see Figure 7).



Figure 7: Design of the investigated device

As input material parameters literature values were used [12][13][14][15][16]. The temperature of the ambient and the power of the heat source were set as boundary conditions of the model. The boundary conditions should match as close as possible to the ones in the real LED during the experiment. The liquid-cooled cold plate was realized as a volume with a fixed temperature. The other parameters were chosen by the associated experiment. The active layer, GaN-layer on the bottom of the LED chip, served as heat source. Applying the junction's power the model converged to equilibrium. This equilibrium was the initial steady state of the model. It's the so-called "hot" steady state of the simulation.



Figure 8: The hot steady state as a first result/estimation of the LED's simulation

After reaching the "hot" steady state in the simulation, the power of the active layer was turned off. This temperature change from the "hot" to "cold" steady state was recorded as a function of time (simulated thermal transient). The temperature of the cold steady state is assumed to be the same as the heat-sink's temperature. Monitoring this temperature drop in the active layer of the device, made it possible to calculate the simulated structure function.

#### 4.2. Comparison between simulation and experiment

The thermal simulation of the LED module allowed the comparison between simulated and experimental structure function. Each experiment of the DOE was simulated too, which enabled a validation of the LED system in terms of thermal behavior.

If simulation and experiment do not match, because the parameters of materials are never known exactly, the simulation can be adjusted to the measurement by varying thermal properties (density, specific heat, thermal conductivity) of the materials. With the aid of this approach it was possible to identify the source of the difference between the two curves. The regions of deviation can additionally be regarded directly via their isothermals of the simulation, since  $R_{th}$  can be regarded as the  $\Delta T$  of two isothermals divided by of  $P_{H}$  (equation 1). Hence, the source of the observed difference can be assigned to a structure in the LED (see Figure 9).

If the simulated and the experimental structure functions match sufficiently, the resulting network in terms of thermal resistances and heat capacitances indicated a solution of the real network of the device. Thus, the numerical model can be regarded as validated in the investigated operation range. The structure function generated from the validated simulation model were used to perform the DOE again (according to the DOE setup described in chapter 3).



Figure 9: Comparison between measured and simulated structure function - the isothermals of the simulation show the affected regions in the LED module

Starting the validation, one measurement of the DOE (500mA I<sub>F</sub>, 25°C  $T_{HS}$ , Thermal paste as TIM, Minimum seek as electrical transient correction and 200s t<sub>meas</sub>) was picked out to simulate it (see Figure 9). The measurement's operating conditions were used as initial values. The simulated structure function was iteratively adjusted to the experimental structure function. The first estimation showed a too low R<sub>th</sub> at the rear part of the structure function. The thermal conductivity of TIM ( $\lambda_{TIM}$ ) had a lower value than the literature values [16] (see Figure 10). The value of  $\lambda_{TIM}$  was changed from 10W/mK to 0.5 W/mK. The reason for that could have been that the LED module was not perfectly

4

dispersed to the heat sink. (There could have been an air gap at the connection or the connection could have been too loose.) This approach can be regarded as a "virtual" dual interface experiment according to the JEDEC 51-14 standard [17], by which it is possible to divide the structure function into two parts. The front part corresponds to the resistance of the LED module and the rear part to the module's attachment to the heatsink [18]. Here, the splitting point of the two structure function with different TIMs takes place at 5K/W (see Figure 10). The value of the device's resistance are quite realistic since the resistance of the mounting can be set to 0 K/W in the simulation. After this validation process of simulated structure function (adjustment with experimental based results) it can be assumed that the simulation reflects (Figure 9) the structure function of a real measurement. There were small differences between simulation and experiment. One reason for that can be that some strongly correlated parameters, e.g. the boundary conditions of the simulations, may differ from those of the real measurement.



Figure 10: TIM has to be adjusted from the first estimation (blue) to its effective value (red) which fit to the experiment

In the first microseconds of the real measurement with the T3ster, an electrical transient occurred (see Figure 11, blue graph). It originates from a not perfect current step of the test setup due to a large amount of stored diffusion-charge-carriers. The electrical transient has no thermal information about the device. Hence, this part of the measurement was replaced with an analytical solution [19]. In the simulated transient, there is no electrical transient behavior, because the step function can be regarded as perfect. A transient correction is not needed in the simulation.

This method (combining simulation and measurement) offers on the one hand a calibrated LED-model, on the other hand an additional method to correct the electrical transient could be generated. At the intersection point of the two transients the measured electrical transient was replaced by the simulated thermal transient (see Figure 11). Therefore, the substitution of the electrical transient offers an approach to the thermal analysis of the first 100  $\mu$ s of the thermal transient [19]



Figure 11: Raw data and the replacement of the early sections of the measured thermal transient

In this chapter the validation process of one measurement was presented. The analytical way of the electrical transient correction was replaced by the numerical approach. The variation of the TIM just has effects on the rear part (here: from 5 K/W) of the structure function and  $\lambda_{\text{TIM}}$  can be determined by an iterative approximation to the experiment. The variation of these parameters revealed no further information about the heat path within the LED-module (see Figure 10), therefore these parameters were not taken into account in the DOE.

If the thermal conductivity was independent from the temperature, the changes of the operating conditions ( $T_{HS}$ , I<sub>F</sub>, t<sub>meas</sub>) would have no effects on the structure function of the simulation. The main focus on this simulation was to investigate the R<sub>th</sub>s differences performed at altered  $T_{HS}$ . The number of the DOE's experiments could be reduced from 2<sup>5</sup> to 2<sup>1</sup>.

Regarding the measurements, in which the I<sub>F</sub> and t<sub>meas</sub> were varied, the differences of the measurements were negligible small (0.3 % - 2 %) (see Figure 4). As shown in chapter 3.4. T<sub>HS</sub> strongly influenced the R<sub>th</sub>s of the structure function – this comes from the temperature dependencies of the thermal conductivities described in chapter 4.4.

### 4.3. Consideration of the temperature-dependent thermal conductivity

As described in chapter 2, the  $R_{th}$  is dependent on the thermal conductance in the heat-flow region between junction and the heat-sink. Combining the experiments of the DOE with the simulation, a temperature dependency of the thermal conductivity had to be taken into account. Different materials, which were implemented in the simulation model, behave differently. As first estimation literature values of  $\lambda(T)$  were used to see if the trends of the experiments were confirmed (see Figure 12) [12][20][21][22].

on Thermal Investigations of ICs and Systems]]



Figure 12: Temperature dependent thermal conductivity of the LED's materials, the right axis presents the values of the dotted line (FR4) and the left axis the values of the solid lines [12] [20] [21] [22].

Figure 12 shows the temperature dependency of  $\lambda$  of the LED's materials. Metals are quite temperature-independent. The point of interest in this simulation model was the  $\lambda(T)$  of the FR4. The parameter becomes higher with an increase of the temperature, in contrast to the thermal conductivity of the semiconductors.

### 4.4. Adjustment of the simulation to the corresponding experiment

The temperature dependency of the materials was implemented in the simulation, such that they were no constant parameters any longer. The simulations with different  $T_{HS}$  (25°C/ 60°C) were compared. The value of dRth1 strongly depends on the properties of FR4 (see Figure 9). As shown in Figure 12 the FR4 gets a higher thermal conductivity with a higher temperature. The difference of  $T_{Hs}$ was around 35°C, so the difference of the thermal conductivity could be estimated to a value around 0.15 W/mK (see equation 2). This lead to a shift of the  $dR_{th}1$ from a higher to a lower value and furthermore to a changing course of the further function. The dRth1 became smaller at a higher T<sub>HS</sub> in the simulation as well as in the experiment. The values of dRth1 and Rth2 of the simulation fitted quite well comparing to the measurement (see Figure 13), indicating that the literature values of FR4's  $\lambda(T)$  were confirmed.

However, the values of the total thermal resistance do not match. A reason was that the effective value of the thermal conductivity of TIM also changed. The thermal conductivity had to be higher regarding the comparison of the green and violet curve in Figure 13. No literature values were found showing such a great effect of the temperature dependency of  $\lambda_{\text{TIM}}$ . Expecting that the applied thermal paste can become more liquid at higher temperature and so a pre-existing air gap between LED module and heat sink can be filled. Therefore, the effective  $\lambda_{\text{TIM}}$  becomes higher in respect of higher temperatures. The enhancement of the  $\lambda_{\text{TIM}}$  was also simulated by an iterative approximation to the experiment (see Figure 14).

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Figure 13: The blue and the red curves show the result of the first calibration (Figure 9). The green line is the measured function at  $T_{HS}$ =60°C and the violet line is its corresponding simulation. It indicates the same peak shift at ~4 K/W, which can assigned to FR4.



Figure 14: The measured structure function (green) at 60°C and its simulations. The thermals resistance of the TIM become smaller with an increase of  $T_{HS}$ . The blue line shows the simulation in which the TIM has the same  $\lambda$  as in the simulation of  $T_{HS}$ .=25°C. The red line is the simulation with a corrected  $\lambda$  of TIM, which is 7% bigger than before.

#### 5. Conclusion

this paper, different operating conditions were In systematically analyzed via experiment as well as numerical simulations making use of a statistical Design of Experiments (DOE) approach. The statistical evaluation of the experiments pointed out the influencing factors and interactions according to the thermal path. For a deeper physical understanding, adjustments of the calibrated LEDsystem were performed in the simulation referred to the experimental DOE. The analysis of the simulated structure function and the heat path investigation by means of the isothermal surfaces showed clearly the influence of the temperature dependencies on the thermal conductivities. This method of combining numerical simulation and experiment linked with a DOE has proven to be a powerful tool, for analyzing complex electronic systems in terms of their thermal behavior.

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**SESSION 10** 

# **SESSION 10** LEDs and LED Lamps

#### Modelling LED Lamps with Thermal Phenomena Taken into Account

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#### Abstract

This paper is devoted to modelling LED lamps with the use of SPICE software with thermal phenomena taken into account. The electrothermal models of components of such lamps: the LED module and the power supply are proposed. The elaborated model of the lamp makes it possible to calculate optical and electrical quantities characterizing properties of the lamp and additionally, the internal temperatures of components of such lamps. The correctness of the elaborated model was verified experimentally for the selected types of LED lamps. A good agreement between the results of calculations and measurements was obtained.

#### 1 Introduction

Every LED lamp contains several components. The typical mechanical construction of the LED lamp is shown in Fig.1.



Figure 1: Mechanical construction of a LED lamp

The lamp consists of the element emitting light, the plastic lens, which is indispensable to fix an angle of the emitted luminous flux, the heat-sink removing heat generated in the lamp, and the switch-mode power supply. This power supply stabilizes the output current or the output voltage.

The light can be emitted by the single LED or by the module containing several LEDs situated on the common basis MCPCB [1]. In turn, the power supply contracted in the LED lamp converts energy from the electroenergy-network into the constants voltage or the constant direct current feeding lighting elements [2, 3, 4]. Because of the limited watt-hour efficiency of this circuit an essential increase of their internal temperature is observed as a result of a self-heating phenomenon [1].

Between the element emitting the light and the power supply, mutual thermal coupling occurs, resulting from the mechanical construction of the lamp, causing an additional increase of the temperature of the mentioned components of the lamp [5, 6]. To limit the value of this increase a heat-sink is used, to which both the mentioned components of the lamp are mounted.

While designing electronic devices computer programmes that perform an analysis of these circuits are used. Very often SPICE software is used [7, 8, 9]. In order to take into account thermal phenomena in the analysis, electrothermal models of the components of the investigated circuit are indispensable [10, 11, 12, 13].

Many papers aim at describing power LED properties [2, 3, 4, 5] and their modelling [1, 6, 11, 14]. Some network solutions of power supplies dedicated to the solid state lighting source are described in [15]. Some papers [5, 16] aim at presenting an influence of the selected factors on technical parameters of LED lamps. Unfortunately, until today we have not found any paper proposing the compact model of a LED lamp.

In this paper the electrothermal model of the LED lamp dedicated for SPICE is presented. This model takes into account electrical and optical phenomena occurring in the investigated lamp, self-heating and mutual thermal coupling between the components of the lamp.

#### 2 The model form

The worked out by the authors electrothermal model of the LED lamp, whose network representation is shown in Fig.2, has the form of a subcircuit for SPICE. In this model 4 blocks can be distinguished: the electrical model of the LED module, the lamp optical model, the power supply model, and the thermal model of the LED lamp. This model belongs to the group of compact electrothermal models and it is formulated according to the rules given in [6, 17].

The electrical model of the LED module describes the dc characteristics of the circuit consisting of m diodes connected in series. This model contains the controlled current source  $G_1$ , the linear resistor  $R_S$  and the controlled voltage source  $E_{RS}$ . The current source  $G_1$  describes the diffusive component of the current of diodes contracted in the module. This current is described by the following equation

$$i = I_0 \cdot \left(\frac{T_j}{T_0}\right)^3 \cdot \exp\left(-\frac{V_{go}}{n \cdot k/q \cdot T_j}\right) \cdot \left[\exp\left(\frac{v_G}{m \cdot n \cdot k/q \cdot T_j}\right) - 1\right] (1)$$



Figure 2: Network representation of the electrothermal model of the LED lamp

where k denotes the Boltzmann constant, q is the electron charge,  $V_{go}$  - the voltage corresponding to the band-gap energy,  $v_G$  - the voltage on the source  $G_1$ , m – the number of power LEDs included in the module,  $T_j$  – the internal temperature of power LEDs, n – coefficients of the emission of the diffusive component of the diode current,  $I_0$  – the model parameter, the value of which depends e.g. on the semiconductor material and on the area of this junction.

The resistor  $R_{S0}$  represents a series resistance of all the diodes contracted in the LED module in the reference temperature  $T_0$ , while the voltage source  $E_{RS}$  describes the linear increase of the voltage drop on the series resistance of the diodes contracted in the module on their internal temperature according to following formula

$$E_{RS} = v_{RS0} \cdot \boldsymbol{\alpha}_R \cdot \left( T_j - T_0 \right) \tag{2}$$

where  $v_{RS0}$  denotes the voltage on  $R_{S0}$  resistor and  $\alpha_R$  is the temperature coefficient of the diode series resistance.

The manner of estimating the values of parameters existing in equations (1 - 2) is described in [6].

The optical model of the LED module represents the controlled voltage source  $E_{L}$ , whose output voltage corresponds to power density of radiation emitted by this module. In the description of the source  $E_{L}$  the influence of temperature and of the current is taken into account [6, 18]

$$E_{L} = E_{0} \cdot \left[ 1 - \exp\left(-\alpha_{L} \cdot i \cdot \left(1 + \alpha_{LT} \cdot \left(T_{j} - T_{0}\right) + + \alpha_{LT2} \cdot \left(T_{j} - T_{0}\right)^{2}\right)\right) \right]$$
(3)

where  $E_0$  denotes power density of the emitted light in the reference temperature  $T_0$  at the maximum diode current value,  $\alpha_L$  and  $\alpha_{LT}$  are current and temperature coefficients of power density changes, respectively.

In turn, the electrical model of the power supply contains the controlled current source  $G_2$ , the controlled voltage source  $E_3$  and the resistor  $R_S$  (for the power supply with the constant output voltage) or the controlled current source  $G_3$  (for the power supply with the constant output current). The

source  $G_2$  describes the waveform of the current received from the network with the properties of the power factor correction circuit taken into account. The current of this source is described by means of the sum of sinusoidal functions of frequencies corresponding to the following harmonics of the network frequency.

$$G_2 = \sum_n a_n \cdot \sin(2 \cdot \pi \cdot n \cdot f \cdot t + \varphi_n)$$
(4)

where f denotes frequency of the input voltage, t – time, whereas  $a_n$  and  $\phi_n-$  the coefficients of the Fourier series describing the input current of the power supply. In the description of the output current of the source  $G_2$  only odd harmonics of the network voltage appear.

The description of the output voltage of the source  $E_3$  takes into account the influence of the internal temperature of the power supply on the output voltage of the not loaded circuit, and the resistor  $R_s$  represents the output resistance of this power supply. The voltage on the source  $E_3$  is described by means of the piece-wise linear function of the form

$$E_{3} = \begin{cases} b_{1} \cdot V_{1} + b_{0} \text{ if } V_{1} < V_{10} \\ b_{3} \cdot V_{1} + b_{2} \text{ if } V_{10} < V_{1} < V_{11} \\ b_{5} \cdot V_{1} + b_{4} \text{ if } V_{11} < V_{1} < V_{12} \\ b_{6} \text{ if } V_{1} > V_{12} \end{cases}$$

$$x = c_{1} \cdot T_{a}^{2} + c_{2} \cdot T_{a} + c_{3} \qquad (6)$$

where  $V_1$  denotes the RMS value of the input voltage,  $T_a$  – the ambient temperature, whereas  $b_0$ ,  $b_1$ ,  $b_2$ ,  $b_3$ ,  $b_4$ ,  $b_5$ ,  $b_6$ ,  $c_1$ ,  $c_2$ ,  $c_3$ ,  $V_{10}$ ,  $V_{11}$ ,  $V_{12}$  are model parameters.

The power supply producing the constant output current is modelled with the use of the controlled current source  $G_3$  described with the following formula.

$$G_{3} = \begin{cases} 0 \text{ if } V_{1} < V_{20} \\ d_{1} \cdot V_{1} + d_{0} \text{ if } V_{20} < V_{1} < V_{21} \\ d_{3} \cdot V_{1} + d_{2} \text{ if } V_{21} < V_{1} < V_{22} \\ d_{4} \text{ if } V_{1} > V_{22} \end{cases}$$

$$(7)$$

where  $d_0$ ,  $d_1$ ,  $d_2$ ,  $d_3$ ,  $d_4$ ,  $V_{20}$ ,  $V_{21}$ ,  $V_{22}$  are model parameters.

The thermal model of the LED lamp belongs to a group of compact thermal models described in e.g. [1, 6, 19, 20]. This model enables calculation of the value of the internal temperature of every diode contracted in the LED module  $T_j$  and the internal temperature of the power supply  $T_{j1}$ . The presented model takes into account both self-heating phenomena in every LED, and in the power supply, and mutual thermal coupling between diodes contracted in the LED module and between this module and the power supply.

The controlled current sources contracted in the thermal model represent thermal power dissipated in every diode contracted in the LED module - G<sub>pth1</sub>, power dissipated in the power supply - G<sub>pth2</sub>, the sum of power dissipated in the other diodes of the LED module - G<sub>pth3</sub>. The output current of the controlled current source G<sub>pth4</sub> is equal to the output current of the controlled current source G<sub>pth2</sub>, whereas the output current of the controlled current source G<sub>pth5</sub> is equal to the sum of output currents of the controlled current sources G<sub>pth1</sub> and G<sub>pth3</sub>. The output voltage of the controlled voltage source  $E_{T1}$  is equal to the voltage  $V_{T1}$  corresponding to an excess of the internal temperature of the diode in the LED module resulting from mutual thermal coupling between these diodes. In turn, the output voltage of the controlled voltage source  $E_{T2}$  is equal to the voltage  $V_{T2}$ corresponding to an excess of the internal temperature of the diode in the LED module resulting from mutual thermal coupling between the diodes and the power supply. The output voltage of the controlled voltage source  $E_{T3}$  is equal to the voltage V<sub>T3</sub> corresponding to an excess of the internal temperature of the power supply resulting from mutual thermal coupling between the diodes and the power supply. RC elements describe self and mutual transient thermal impedances in the considered model.

The output current of the controlled current sources existing in the thermal models are given by following equations:

$$G_{pth1} = \frac{v_G}{m} \cdot i - \frac{P_{opt}}{m} \tag{8}$$

$$G_{pth2} = \frac{v_G}{m} \cdot i \cdot (m-1) - \frac{P_{opt}}{m} \cdot (m-1)$$
(9)

$$G_{pth3} = \sqrt{\frac{1}{t}} \int_{0}^{t} V_{in}(x) \cdot I_{G2}(x) \cdot dx - V_{out} \cdot I_{out}$$
(10)

where  $P_{opt}$  denotes the optical power emitted by the LED module, t is the time,  $V_{in}(t)$  – the line voltage,  $I_{G2}(t)$  – the current of the source  $G_2$ ,  $V_{out}$  and  $I_{out}$  are the output voltage and the output current of the power supply, respectively. The value of  $P_e$  is described with the following formula

$$P_{opt} = \pi \cdot E_L \cdot l^2 \cdot tg^2 (\alpha/2) \tag{11}$$

where l is the distance from the LED module at which the value of power density of the emitted light  $E_L$  is measured and  $\alpha$  is an emission angle.

#### 3 Results

By means of the presented model a lot of characteristics of different types of LED lamps were calculated and the results of calculations were compared with the results of measurements. In the next part of this section the results of investigations of two LED lamps (CLA25 and CLA60) by OSRAM are presented. The nominal values of electrical power of these lamps are equal to 4 W and 8 W, respectively. The emitted luminous flux is equal to 250 lm for the lamp CLA25 and 806 lm for the lamp CLA60.

The LED module included in the lamp CLA25 consists of four power LEDs connected in series and mounted on the common MCPCB. The nominal value of the current flowing through this module is equal to 350 mA. The optical and electrical properties of this module are considered in paper [14]. The power supply included in this lamp has the form of switch-mode power supply with the constant value of the output voltage. This power supply consists of the classical rectifier bridge and the flyback dc-dc converter with the PWM controller.

In turn, the LED module of the diameter equal to 32 mm included in the lamp CLA60 consists of 13 power LEDs connected in series with an PTC thermistor. The nominal value of the current flowing through this module is equal to 120 mA. The power supply included in this lamp has the form of switch-mode power supply with the constant value of the output current. This power supply consists of the classical rectifier bridge and the flyback dc-dc converter with the PWM controller [15].

In the figures presented in the further part of this section points represent the results of measurements, whereas lines – the results of calculations. At first, the calculated and measured characteristics of the LED module from the lamp CLA25 operating outside the considered lamp are presented in Figs. 3 and 4. In the considered case the considered module operates at three different cooling conditions and the presented characteristics correspond to the steady state. Investigations were performed for the module situated on the aluminium heat-sink of the dimensions 8x180x118 mm (the big heat-sink), on the aluminium heat-sink of the dimensions 2x100x75 mm (the small heat-sink) and for the module operating without any heat-sink. The measurement of optical parameter are measured at the distance between the module and the lighting sensor equal to 16.5 cm.

Fig. 3 illustrates the dependence of power density  $P_e$  of the light emitted by the considered module on the supply current at the steady state.



Figure 3: Calculated and measured dependences of power density of the light emitted by the module CLA25 on the supply current at different cooling conditions

It is visible that the dependence  $P_e(I)$  is an increasing function, and at worsening the cooling conditions of the module, one can observe a fall in the value of the power

density of the emitted light. This fall increases in the function of the output current of the power supply, reaching even a dozen or so percent.

Fig. 4 illustrates the calculated and measured dependences of the temperature of the basis of the module  $T_c$  on the conduction current. Additionally, in this figure the calculated dependences of the internal temperature of the diode contracted in this module on the output current of the power supply are marked with dashed lines. As it is visible, both the temperature of the module, and the internal temperature of the diode are increasing functions of the output current of the power supply. The temperature of the module increases in the considered range of changes of the output current of the power supply even to 90°C.



Figure 4: Calculated and measured dependences of temperature of the module CLA25 on the current of the power supply at different cooling conditions

From the point of view of quality of the energy in the electroenergy-network, it is important, that the waveform of the current feeding the lamp has a shape most nearing to the sinusoid and that the phase difference between the course of the current and the feeding voltage is the least. Fig. 5 presents the calculated and measured waveforms of the current feeding the lamp CLA25 calculated at different RMS values of the supply voltage equal to 80 V, 130 V and 230 V, respectively.



Figure 5: Calculated and measured waveforms of the input current of the LED lamp CLA25 obtained at different RMS values of the input voltage

As one can notice, the shape of the obtained waveforms of the input current strongly differ from the sinusoidal waveform. Additionally, the amplitude of the input current decreases at an increase in the RMS value of the input voltage. The obtained shape of the waveform of the current  $I_{\rm in}$  shows that from the point of view of the electroenergy-network the considered system is seen as the rectifier with non-linear capacitive load.

Fig. 6 illustrates the calculated spectrum of the input current obtained at different values of the RMS value of the input voltage. As it is visible, up to 35 harmonics should be taken into account in order to properly describe the measured waveforms of the input current.



Figure 6: Calculated spectrum of the input current of the LED lamp CLA25 obtained at different RMS values of the input voltage

The parameter, which characterizes a discrepancy between the considered waveforms and the sinusoidal wave is the total harmonic distortion (THD). The calculated value of this parameter is very high and it is equal to 72.9% for  $V_{in} = 80 \text{ V}$ , 83.96% for  $V_{in} = 130 \text{ V}$  and 69.2% for  $V_{in} = 230 \text{ V}$ . These values of the THD are near the values of the measurements shown in [5] and they are very high. Such a high value of THD could lead to worsening of quality of the electrical energy in electro-energy network.

The next two figures (Fig. 7 and 8) illustrate the influence of mutual thermal coupling between the LED module and the power supply on the characteristics of the considered lamp CLA25. In these figures dashed lines correspond to the disassembled lamp, in which the LED module and the power supply are not connected together, and solid lines - the mounted lamp.

Fig. 7 presents the calculated and measured dependences of power density of the emitted radiation on the RMS value of the supply voltage for the lamp CLA25.

As it is visible, for the mounted lamp the value of power density is higher even by 25% than for components of the lamp operating separately. It is worth noticing that for the input voltage lower than 70 V the dependence  $P_e(V_{inRMS})$  is an increasing function. It is the result of the increasing output voltage of the power supply. In this range of change

of  $V_{inRMS}$  the output voltage of the power supply increases from 11.3 V to 12.5 V.



Figure 7: Calculated and measured dependences of the emitted optical power on the RMS value of the input voltage for the LED lamp CLA25

In Fig. 8 the calculated and measured dependences of the internal temperature of the LED module and of the power supply on the RMS value of the supply voltage for the lamp CLA25 are shown.



Figure 8: Calculated and measured dependences of the internal temperature of the LED module and of the power supply on the RMS value of the input voltage for the LED lamp CLA25

As one can observe, for the disassembled lamp the temperature of its components is even about 70°C higher than for the mounted lamp. The element, which more intensively gets warmer, is the LED module. The cooling system applied in the considered LED lamp allows reducing the temperature of the LED module. Thanks to this reduction of internal temperatures, we observe in Fig. 7 an increase in the value of power density of the emitted light.

In Figs. 9 - 11 the selected results of measurements and calculation characteristics of the LED lamp CLA60 are presented. Fig. 9 illustrates the influence of the RMS value of the input voltage on the waveforms of the input current of the lamp CLA60.

As it is visible, the shape of this waveform is nearer to sinusoidal waveforms than the waveforms obtained for the lamp CLA25 (Fig.5). The values of THD are as follows:

52.3% for  $V_{inRMS}$  = 70 V, 28.6% for  $V_{inRMS}$  = 130 V and 24.6% for  $V_{inRMS}$  = 230 V.



Figure 9: Calculated and measured waveforms of the input current of the LED lamp CLA60 obtained at different RMS values of the input voltage



Figure 10: Calculated and measured dependences of the emitted optical power on the RMS value of the input voltage for the LED lamp CLA60



Figure 11: Calculated and measured dependences of the internal temperature of the LED module and of the power supply on the RMS value of the input voltage for the LED lamp CLA60

In Fig. 10 the dependence of power density of the emitted lighting on the RMS value of the input voltage is shown, whereas in Fig.11 the dependences of the internal

temperature of the LED module and of the power supply on the RMS value of the input voltage are presented. In these figures dashed lines correspond to the disassembled lamp in which the LED module and the power supply are not connected together, and solid lines – to the mounted lamp.

In the considered figures it is visible that similarly as for the lamp CLA25, after assembling components of the lamp the increased temperature of the power supply and the lower temperature of the LED module occur. As a result of a fall of temperature of the LED module, the power density of the radiation emitted by the lamp increases. It is good to notice that power density of a radiation is a growing function of the input voltage.

#### 4 Conclusions

In the paper the manner of modelling LED lamps in SPICE was presented. Electrothermal models of components of such a lamp, i.e. the power supply and the LED module were proposed. These models have a simple form and they could be used both in dc and transient analyses. In these models one took into account both self-heating phenomena and mutual thermal couplings between the mentioned components of the lamp. The correctness of the worked out model was verified experimentally for two types of lamps and the good agreement between the results of calculations and measurements was obtained.

The presented results of investigations prove that the power supplies used in the considered lamps are characterised by very different values of the THD of the input current. For both the considered lamps the value of THD is high and in order to compensate their favourable influence on quality of the electrical energy the power factor correction circuits (PFC) should be installed at the input of these lamps.

On the other hand, the mutual thermal coupling between components of these lamps makes it possible to reduce the value of the internal temperature of the LED module and consequently to increase the value of the emitted luminous flux.

The presented model can be useful for designers of lighting systems and in teaching properties of solid state lighting sources.

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## Embedded multi-domain LED model for adaptive dimming of streetlighting luminaires

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#### Abstract

Temperature dependence of solid state lighting products is often not considered. Lighting products are designed either to be too robust to fulfil the requirements under any possible environmental conditions, or fail to perform the minimal expectations due to high ambient temperature. However, temperature dependent nature of LEDs even could be a new benefit, taking it into account in the design stage. Keeping the light output values at the desired level at any ambient temperature would be a cost efficient solution. This paper shows power saving effects of a smart adaptive system using a controlled current source and describes a method to gain the controlling functions. A case study with real meteorological temperature dataset is carried out.

#### 1 Introduction

Significance of LED based luminaires is rapidly increasing in the field of outdoor illumination applications such as streetlighting. In terms of efficacy and expected product life time modern high-power LEDs already provide better performance than incandescent and fluorescent lamps and nowadays are competing with gas discharge lamps. Although, thermal constraints of semiconductor based luminaires require careful development of the cooling capabilities due to the increasing dissipation density and to the temperature related nature of LEDs, the temperature dependence of the operating parameters can be well characterized and can be turned into a new benefit of such devices.

Operation of LEDs is highly sensitive to the temperature of the pn-junction; at a constant forward current, with the increase of the junction temperate, the forward voltage, the efficiency and the efficacy decreases, altogether decreasing the radiant and luminous flux output of the device. Therefore, the minimum light output characteristics of a streetlighting luminaire must be designed according to the highest possible ambient temperature that can occur (i.e. the hottest summer night) when later using the specific luminaire model. However, such considerations will make the design too robust over the rest of the year (e.g. during the cold winter nights), especially at geographical locations where the average temperature is much lower. Keeping the light output characteristics at a constant level over the year and at any geographical position would significantly increase the efficiency of outdoor solid-state lighting (SSL) products. By monitoring the ambient temperature a smart adaptive system can fix the light output values through a controlled current source or through dimming with variable duty-cycle, according to a pre-specified look up table (LUT) of forward current vs. ambient temperature. Such LUTs for controlled current sources can be generated from the so

called iso-flux characteristics (set of operating points providing constant radiant/luminous flux values under any environmental conditions) of an LED. LUT generation for adaptive dimming requires AC simulations due to the different capacitive effects; AC simulations are out of the scope of this paper but DC simulation results for adaptive current controlling are described later on as a preceding step to AC dimming.

#### 2 Technical background

Characterisation and simulation of power LEDs is a multidomain task due to the strong interactions between the operating parameters; performance of an LED in the electrical, optical and thermal domains must be handled simultaneously. The JESD51-5x family of standards [1], [2], [3] provides an appropriate recommendation for packaged LED measurements. According to the standards, optical parameters are measured in thermal and electrical steadystate which is then followed by a so called thermal transient measurement. Knowing the K-factor of the device (reciprocal of the temperature dependence of the forward voltage of a diode) by post-computing it is possible to detect the thermal RC map of the mechanical structure from junction to case and also to reveal the junction temperature of the steady-state during the optical measurements. This way temperature dependencies of the device under test are obtained, however, scope of the technique has much rather an "external observer" nature (LED performance under specified external conditions like ambient temperature and thermal resistance of the mechanical assembly).

A step forward in the characterisation techniques has been achieved by Mechanical Analysis Division of Mentor Graphics with the T3Ster and TeraLED test equipment by automatic control of the ambient temperature in order to reach pre-defined junction temperature values. By such techniques it is possible to reveal the real isothermal characteristics of an LED; forward current – forward voltage and forward current – radiant/luminous flux value pairs while the pn-junction temperature is kept constant (see in Figure 1 and in Figure 2).

Considering the total radiant flux of an LED is essential since a significant part of the consumed electrical power leaves the package in the form of light; the measured electrical power needs a correction by the total emitted radiation to get the proper heating power data. Measuring luminous flux values is not indispensable for correct electrothermal simulations but highly desirable when dealing with applications where perception of the human eye is a major issue.

Measured radiant and luminous flux values may be handled by various ways during coupled electrical, thermal and optical simulations. The most commonly used quantities are:

- *Radiant efficiency* (of a source of radiation) "is the ratio of the radiant flux of the emitted radiation to the power consumed by the source" (symbol is  $\eta_e$ ; unitless) [4].

– *Luminous efficacy* (of a source) is the "quotient of the luminous flux emitted by the power consumed by the source" (symbol is  $\eta_v$ ; unit is [lm/W]) [5].

– Luminous efficacy of radiation is the "quotient of the luminous flux,  $\Phi_v$ , by the corresponding radiant flux,  $\Phi_e$  (symbol is capital-Greek K; unit is [lm/W]) [6].

In our example Figure 3 shows the isothermal efficacy  $(\eta_v)$  characteristics of a test LED sample.

#### 3 Iso-flux characterization

Our new approach is driving the LEDs according to their iso-flux characteristics which assigns a forward current value for each ambient temperature value in order to keep the radiant flux and/or the luminous flux of an LED constant. Method of generating the ambient temperature vs. forward current function depends on the complexity of the SSL device.

#### 3.1 Direct measurement

In case of simple 1-LED assemblies (or in cases when there are no considerable cross heating effects and the main heatflow path is 1D like) merely the isothermal characteristics allow "hot lumen" calculations. Since the junction temperature is fixed, the power dissipation at any measurement point is independent from the thermal resistance of the actual mechanical structure; by substituting the thermal resistance of the required fixture it is possible to calculate the set of ambient temperatures corresponding to the specific points of the isothermal characteristics. Once the ambient temperature - forward current - radiant/luminous flux triplets are available, by simple regression and extrapolation methods the desired iso-flux ambient temperature vs. forward current function can be derived. Figure 4 and Figure 5 show simulated iso-flux characteristics of a test LED mounted on a simple Zhaga heatsink. (100% light output defined at 50 °C ambient

temperature and 350 mA forward current; 100%, 80%, 60%, and 40% light output characteristics.)



*Figure 1: Isothermal forward voltage – forward current characteristics of a test LED* 



*Figure 2: Isothermal forward current – radiant flux characteristics of a test LED* 



*Figure 3: Isothermal forward current – efficacy characteristics of a test LED* 



Figure 4: Iso- $\Phi_{\rm e}$  characteristics of a test LED sample; 40-60-80-100% of the reference light output characteristics; reference defined at  $T_{\rm ambient}$ =50 °C and  $I_{\rm forward}$ =350 mA



Figure 5: Iso- $\Phi_v$  characteristics of a test LED sample; 40-60-80-100% of the reference light output characteristics; reference defined at  $T_{ambient}=50$  °C and  $I_{forward}=350$  mA

Isothermal characteristics of any setup can also be measured directly by regulating the forward current in-situ, in order to keep the light output characteristics at the desired level while step-by-step changing the cold-plate temperature of a combined electrical, thermal and optical measurement system. This method does not need specific simulation methods and even could be automated, however, it could be time-consuming, inaccurate and inflexible – possibly the most significant drawback is that it cannot be performed in the design stage.

#### **3.2** Measurement and simulation

In case of complex mechanical structures where crossheating effects must be considered (like in case of outdoor luminaires) multi-domain simulations may be necessary to reveal the "hot-lumen" map of the luminaire. Chip-level multi-domain LED models – that can be implemented in Spice-like circuit simulator software and are applicable for variable forward current values – have been proposed and described in many previous papers [7], [8], [9]. In the articles [10] and [11] the proposed LED model is used to calculate the hot lumens of a real streetlighting luminaire (see the CFD model in Figure 6). As the next step, the iso-flux characteristics of the same luminaire are derived from new simulation results.



Figure 6: 3D CFD model of the luminaire with the LED package footprint [11]

## 4 Simulation with embedded multi-domain LED models

The thermal resistance net of the luminaire assembled with the multi-domain model of the arbitrarily chosen LED sample was tested in -30 °C, -15 °C, 0 °C, +15 °C and +30 °C ambient temperatures. At each ambient temperature, independent simulations were performed with forward current sweep, using the Eldo circuit simulator software [12].

Forward voltage, radiant flux and junction temperature were operating point parameters obtained from the Eldo simulations. Hot lumens were calculated using the luminous efficacy of the test LED, defined from previous measurement results. Forward current- and temperaturesensitivity of the luminous efficacy were both considered for each assembled LED individually due to the junction temperature differences along the luminaire.

#### 4.1 Simulation results

Figure 7 shows the simulated forward current vs. "total hot lumen" characteristics of the luminaire. Deflection of the +30 °C curve is due to the growing decrease of the luminous efficacy at high junction temperatures ( $T_j = 120.4 - 124.7$  °C at 700 mA forward current and 30 °C ambient temperature; radiant efficiency and light conversion efficiency in the phosphor both decrease). Considering the forward current and ambient temperature dependence of the total hot lumens, by 2<sup>nd</sup> degree polynomial regression the iso-flux  $\Phi_v^{total}(T_{ambinet}; I_{forward})$  formula was set. The

simulated iso-flux line with the correspondent temperature – current pairs is also indicated in Figure 7.



Figure 7: Simulated total hot lumens of the luminaire with the defined Iso- $\Phi_v$  line (where the corresponding ambient temperatures are indicated)

The same regression technique was applied to specify the iso-flux power consumption of the whole luminaire as the function of forward current and ambient temperature (power consumption while the total luminous flux output is kept constant at any ambient temperature). Power consumption curves are indicated in Figure 8.



Figure 8: Simulated power consumption of the luminaire with the defined Iso- $\Phi_v$  curve (where the corresponding ambient temperatures are indicated)

#### 4.2 Case study

The gained iso-flux formulas were applied for real-life conditions to test the energy saving ability of the proposed technique. Daily temperature values of the past decade are available at the Hungarian Meteorological Service [13]; data series of the last 10 years of Szombathely (Hungarian city; 47.23512°N 16.62191°E) was chosen to compare adaptive current control and constant current mode.

Reference boundary conditions for which the luminaire is supposed to be designed (maximum forward current and highest ambient temperature) were set arbitrarily. The reference forward current was set to be 700 mA (a common datasheet value for power LEDs) while the expected maximum temperature was set to be 27.9 °C (the highest daily minimum temperature in Hungary, measured: 20.07.2007, Pécs-Árpádtető [14]). Having only the daily maximum, minimum and mean temperatures, to acquire cautious and conservative results we calculated with the daily mean temperatures (instead of the daily minimum values) and considered all the dark periods to be 8 hours (neglecting the increasing length of the winter nights).

Figure 9 shows power consumption charts during the first 2 years of the 10-year period. The result of the investigation is 2.84 MWh (97.2 W in average) for constant current mode and 2.55 MWh (87.3 W in average) for adaptive controlling; in the investigated period 10.2% of the consumed electrical energy could have been saved by the proposed technique.

Figure 9 also shows some specific properties of LED based devices: under constant current drive, power consumption increases with decreasing temperature due to the negative temperature sensitivity of the forward current.

In our case study the expected maximum temperature was chosen arbitrarily. For stricter nominal requirements towards the SSL device the savings are also higher. Figure 10 shows the energy saving up to 40 °C reference ambient temperature which is still not inconceivable in real-life conditions. During a hot summer evening, temperature of a luminaire placed in the Sun and above a hot driveway may reach even higher temperatures; however, luminous flux output of the luminaire should be above the nominal value shortly after sunset as well as during the night.



*Figure 9: Power consumption of adaptive current control* (lower) and constant current mode (upper) during the first 2 years of the investigated decade



Figure 10: Energy saving in Szombathely as the function of the reference (expected maximum) ambient temperature (reference forward current is 700 mA)

#### 5 Conclusion

Streetlighting luminaires are designed to fulfil the requirements under any possible environmental conditions, making the designs too robust. Keeping the light output values at the desired level at any ambient temperature would be a cost efficient solution; a smart adaptive system needs a controlled current source or a variable duty-cycled dimming, according to the monitored ambient temperature and a prespecified look up table. Such look up tables can be generated from the iso-flux characteristics of the applied LEDs. According to the early simulation results efficiency of SSL devices may be increased even by 10% by applying adaptive controlling techniques.

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#### Experimental Study of Electroluminescence And Temperature Distribution In High-Power AlGaInN LEDs & LED Matrixes

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#### Abstract

Comprehensive analysis of current spreading, temperature distribution, and near-field electroluminescence of high-power "face-up" AllnGaN LEDs and LED matrixes been performed by combination of different experimental and methods. A thermal resistance characterization consists in investigations of transient electrical processes in the diode sources under heating by direct current and analysis using a thermal equivalent circuit (the Cauer model). By the involved method, thermal resistances of internal elements of the LEDs are determined. At the same time high resolution mapping of EL and thermal radiation was obtained by optical microscope and infra-red images technique. It has been established correlation of the thermal resistance with a change in the current distribution at high excitation levels (current crowding).

#### 1 Introduction

One of the main trends in the LED development is the increase of the luminous flux, achieved by increasing the area of the emitting chips and operating currents. This leads to high junction temperature and temperature gradients which causes the degradation of optical performance as well as the low reliability. In this connection, special importance is the task of precise determining the junction temperature, taking into account a possible non-uniformity of its distribution on the chip area. Successful thermal management of LEDs requires both current and heat distribution simulation in real LED structures and improvement of experimental methods for determining of resistance. Several approaches thermal such as electroluminescence (EL) spectrum, infrared (IR) thermal microscopy, Raman spectroscopy are available for junction temperature measurement.

However, the most widely used the thermal transient method based on passing step-electric current through a diode and measuring the response, which is measurement of the temperature of the p-n junction during the diode heating to its steady-state condition. The p-n junction temperature is determined by a temperature-sensitive parameter - forward voltage drop on a diode at low measuring current. A heating curve analysis based on the structure functions allows determining total thermal resistance and contribution of internal elements of LEDs [1].

This paper reports on a comprehensive analysis of the heat transfer (thermal resistance), current spreading and temperature distribution in connection with the overall performance of high-power "face-up" AlInGaN LEDs and LED matrixes, carried out with a combination of advanced characterization techniques. High-resolution mapping of the IR radiation and EL were used to obtain the information on the lateral distributions of temperature and near-field light emission intensity in the LED and LED matrixes. The thermal resistance was measured by the forward-voltage relaxation method with Thermal transient tester T3Ster (MicRed) [2].

The samples studied were commercial LEDs produced by Epistar having so-called "face-up" design, in which the epitaxial AlInGaN heterostructure is saved at the initial sapphire substrate and high-power LED matrixes based on them.

#### 2 Experiment

#### 2.1 Samples

Commercial ES-CABLV45P LED chip (Fig.1) produced by Epistar with a chip area of 1140x1140  $\mu$ m<sup>2</sup> was used in the experimental study [3]. As the figure 1 shows a chip has a rather complicated "branching" topology of electrodes to improve the conditions of the current spreading. The single "face-up" chip was mounted onto a metal-core printed circuit board (MCPCB). The schematic view of the chip and heat transfer path is shown in the insert of Fig. 4. The MCPCB, in turn, was soldered to an external heat sink. The operating current density could exceed 100 A/cm<sup>2</sup>



Figure 1. Schematic design of the "face-up" chip, the geometry of the electrodes is shown in black.

In a similar manner it was made LED matrixes (chip-onboard technology) with total input power of 100 W (that corresponds to a current of 350 mA through a single chip). The matrix consists of 10 parallel-connected LED arrays, each of which comprises 10 LED chips connected in series. The matrix was placed in the Al housing size of 20x20 mm<sup>2</sup>. Photo of matrix and schematically cross-section of construction are shown in Fig. 2.



Fig. 2. General view and construction of 100-chip LED matrix.

ambient

#### 2.2 Measuring of the thermal resistance.

The total thermal resistance and thermal resistance of internal elements of the LEDs were determined basing on thermoelectric analogy. The 1D heat transfer through the active region, sapphire substrate, and MCPCB was considered similarly to the current flow in an equivalent electrical circuit. Generally, there are two conventional models for building up the equivalent circuit; we used Cauer's one combines all the capacitances to a common bus [4].

Detailed studies of thermal resistance of LEDs and LED matrix were produced by method based on time relaxation of the forward voltage and calculation cumulative or differential structure function. Its essence is that the LED is supplied heating step a given power, and during the heating periodically for a short time a heating power is switched off and measures the temperature-sensitive parameter – forward voltage drop on the p-n-junction at low test current. As mentioned above, this method is realized in the T3Ster-Thermal Transient Tester.

First, in the calibration stage LED was driven by a fixed test current of 5 mA (for the matrix used 50mA by the number of parallel LED arrays). During calibration the temperature of the whole setup including LED, MCPCB and radiator was gradually increased by external heater and dependence of the forward voltage on the temperature was tabulated. The linear dependence with a temperature coefficient TCU ~ -1 mV/<sup>0</sup>C was established for a single LED. Later this dependence was used to determine the p-n junction temperature. The test current was assumed to provide no additional heating. All temperature measurements were done with accuracy of at least 0.5 <sup>0</sup>C.

Next, in step measurement a large (heating) current is applied to the LED, causing it to heat up. Then the large current is turned off and the smaller test current is forced into the device again and the forward voltage measurement is performed continuously with a high sampling rate. The temperature evolution during heating was measured by a short pulse of test current cut through heating current (while heating current is turned off). From these data, one can determine the components of the equivalent RC-circuit clearly displayed in the form of calculated differential structure function.

## 2.3 Measuring of near-field of electroluminance (emission intensity distribution).

The near-field of EL was used to estimate the distribution of the current density on the area of p-n-junction. As a first approximation both distribution can be considered coincident, although more accurate determination requires taking into account the dependence quantum efficiency on the current density and the scattering of light in the chip. For these reasons the EL non-uniformity is slightly more smoothed than the current density one [5]. However, at high operating currents, studied in this paper, the dependence of the quantum efficiency on current disappears and compliance of current and EL emission distribution is quite satisfactory. The EL was mapped by a Mitutoyo optical microscope with a Canon digital camera (12 Mpxl CMOS photosensitive matrix). The minimum and maximum field of view of the optical system was 536x357 and 5362x3520 mm<sup>2</sup>, respectively, with the best spatial resolution of 0.25 mm. The optical system collected the light within the  $15^{0}$  cone around the normal direction. The CMOS matrix was equipped with four Bayer filters. Operating with blue LEDs, we used them as neutral filters with different transmittances at the wavelength of 470 nm, which enabled measurements in a wide range of luminance variation. Another way to increase the dynamic range of our measurements was variation of the CMOS matrix exposure time in the range of 5-1000 ms.

#### 2.4 IR thermal imaging

An alternative well known approach to determining the surface temperature distribution is based on the application of thermal imaging equipment. This allows to measure the temperature directly and thus to obtain more detailed information on the temperature distribution. To obtain the temperature distribution inside the chip, the IR thermal radiation in the spectral range of  $2.5-3 \mu$  was mapped by a specially designed IR microscope. We would like to emphasize that using a relatively short wavelength IR radiation (compared to an  $5-12 \mu$  range utilized in conventional thermal-imaging systems) allowed us to reduce diffraction blurring and thus to improve the spatial resolution of the IR mapping down to 3 µ. Earlier, we investigated in detail by thermal imaging microscopy temperature fields in the chips of different designs [6]. In this study, we focused on temperature fields in high-power LED matrixes.

The main methodological problems of thermal imaging of AlInGaN structures are (i) the transparency of the sapphire substrate and epitaxial layers for IR radiation and (ii) a large difference in the emissivity of the materials utilized in the LED, i.e., semiconductor layers, metallic electrodes, reflective coatings, mounting elements, etc. [7]. So, extraction of correct temperature distributions from the IR images requires preliminary calibration of data for every particular object. Such a calibration was made with the temperature control by external heater in the range of 20-100 °C and recording the IR radiation from the LED matrix at zero current. An example of such calibration curve for LED matrix coated with silicone is shown in Fig.3. The calibrated relationship between the IR radiation intensity and temperature was then used to determine the absolute temperature of every element of the matrix under actual operation conditions. Using the above approach, we were able to measure the temperature with the accuracy better than 2 K.



Figure 3 Calibration curve temperature- IR-signal for silicone covering the LED matrix

#### **3** Results and discussion

In Fig. 4 are shown the results of measurement of thermal resistance for single ES-CABHV45P LED obtained with T3Ster. The differential structure functions for set of heating current: 300 mA, 500 mA and 1000 mA are presented. One can see that first peak related to thermal resistance R1 from the p-n junction to the chip bottom surface is nearly the same for all heating currents. While the second peak related to thermal resistance R1+R2 (chip + glue) and the third peak related to the thermal resistance R1+R2+R3 (chip + glue + MCPCB) are shifted right indicating increase of the respective thermal resistance with the current. Quantitatively for the "face-up" LED increase in current from 300 mA to 1000 mA leads to an increase in thermal resistance of 1.5 -1.9 times. It seems reasonable to associate the growth of the thermal resistance with current to the change in current distribution, respectively the heat generation. To confirm this assumption, studies electroluminescence distributions across the chip area have been conducted.



Figure 4 Differential structure functions of LED at the four values of the driving current 300, 500 and 1000 mA obtained by T3Ster. Peaks indicate components of thermal resistance. Insert shows schematic view of the chip and heat removal path

The experimental near-field EL emission patterns obtained at the current of 300 mA and 1000 mA are shown in Fig. 5. According to the initial concepts, both the current density and EL intensity increase near the edge of the p-electrode, due to the insufficient conductivity a semi-transparent contact to p-GaN and a thin p-GaN semiconductor layer. The observed increase of the emission intensity next to electrode edges is an evidence for considerable current crowding. The evolution of the EL intensity distribution when driving current vary from 300 mA to 1000 mA is demonstrates clearly localization of current and heat generation near the n-contacts pads which means the reduction of the effective cross section of the heat flow. Thus, the behaviour of the thermal resistance with current (the deviation from a constant), and not only the absolute value of it should be the criterion of possibility of using LEDs at high operating currents.



Figure 5. Profiles of EL intensity in the cross-section A at two values of operating currents: 300 mA and 1000 mA

Let us now consider the thermal resistance and temperature distribution for high-power LED matrix. As for measuring the thermal resistance of the LED matrix by T3ster equipped with a booster, its results are represented as a differential structure function shown in Fig.5. The total thermal resistance (chip + glue + MCPCB of about 0.3 K/W is approximately 20 times (not in 100) less than for a single LED of the same design. Naturally it is explained by the fact that the heat dissipation from the center of the matrix is worse than at the periphery. The latter clearly demonstrates the direct measurement of temperature distribution obtained by infrared thermal imaging. The observed lateral distribution of the IR intensity and corresponding temperature (with account of the emissivity calibration) at the cross-section A is shown in Fig. 7. As the shape of the curve, there is a noticeable difference in the temperature reaches about 15 C, between the central and peripheral parts of the matrix. This should be considered when evaluating the values of the thermal resistance obtained from the electrical measurements (Fig .6) which are the average.



Figure 6 Differential structure functions of the 100 W LED matrix at the current 3.5 A obtained by T3Ster



Figure 7 Temperature distributions in the central crosssection of LED matrix at input power of 100 W

#### 4 Conclusions

High-power AlInGaN blue LEDs of "face-up" design and LED matrixes based on them have been studied by advanced experimental techniques including high-resolution mapping of EL and IR radiation (thermal imaging) and transient thermal analysis. It was studied and analysed EL emission intensity distributions and thermal resistance values of LED chips in wide range of operating currents. Comparison of the pictures of the current spreading and dependency of the thermal resistance on current revealed that "face-up" LEDs at high current (~1A) due to localization of current near the contact pads increase its thermal resistance by 1.5 times. The "current crowding" effect is due to the insufficient conductivity a semi-transparent contact to p-GaN and a thin p-GaN semiconductor layer. It was established a good correlation between the picture of the current distribution and the thermal resistance of LEDs. Localization of current near the contact pads at high levels of excitation is manifested as increase of thermal resistance by reducing the cross section of the heat flux from the active region to the radiator.

The slope of current dependence of the thermal resistance at transition from small to large currents can be used to estimate current and temperature dependence of the
efficiency of the LED and the non-uniformity of the distribution of current density and temperature structure. Consequently, the behaviour of the thermal resistance with current increase can be a criterion for the suitability of LED for operation at high loads.

The picture of the temperature distribution in the LED matrix obtained by IR thermal imaging evidences of significant thermal gradients from the center to the periphery. The difference in the temperature at an input power of 100 W is about 15 <sup>o</sup>C. The latter to be considered when evaluating the thermal resistance based on the electrical measurements, which has an average value.

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**SESSION 11** 

# **SESSION 11** Reliability Investigations

#### Aging Tendencies of Power MOSFETs -

#### A Reliability Testing Method Combined with Thermal Performance Monitoring

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#### Abstract

Die attach degradation in power electronic devices is a common failure mode besides bond wire damage. This paper describes the chip and packaging level effects of high cycle count power cycling on novel mid-power automotive MOSFETs. The related investigation is carried out in controlled ambient conditions. The thermal transient measurements during the active temperature cycling reliability test were evaluated along with K-factor calibration to identify different failure modes. The described measurement method gives the opportunity to distinguish between electrical and thermal related structural error modes. The newly developed thermal interface used in the DUTs was found to withstand the 150 °C thermal amplitude well beyond 100,000 cycles without fatal failures. The thermal performance degradation was less than 28.5 % after 70,000 cycles for the complete assembly.

#### 1 Introduction

Nowadays power electronics such as diodes, MOSFETs, IGBTs and integrated circuits are getting even more complex with increasing dissipated power density. They often have to work in harsh environmental conditions. As transferred energy is on a rise both in commercial and industrial application, every year the challenge is getting bigger for the manufacturers to increase the power rating and load current capability of their devices without sacrificing reliability. Also, the designers have to develop new thermal interface materials (TIM) facing the high power dissipation of such devices, and reliable bonding techniques. Thermal-aware design and selecting the proper thermal interface material for the application is mandatory to avoid premature failures [1]. At the stage of product development, it is mandatory to have data on the estimated lifetime in a certain application. These estimations can be supported by reliability test data.

The idea behind reliability testing is to fully characterize the system under test before aging and to apply harsh environmental conditions (e.g. high amplitude temperature and relative humidity changes) for a certain time and to measure thermal, electrical and optionally optical parameters at regular intervals. The 2014 year Therminic paper of the authors introduced a combined reliability test method for light emitting diodes, so now an enhanced method will be introduced for discrete MOSFET devices [2]. The core of the reliability test environment was the Viking Reliability Tester.

There are standard testing methods to reveal the aging phenomena of electrical devices. These standards usually define the test environment, the measurements to be performed, and the requirements towards the test equipment.

The JEDEC JESD 22-A family of standards (e.g. [3], [4]) deals with semiconductor devices generally. The most

commonly used method for testing the long-time behaviour of die-attach materials is temperature cycling. These tests may be carried out on dummy samples in high volumes; however, such tests are time-consuming and require special environmental chambers [5].

These commonly used standards typically use directly measurable electrical parameters to monitor the device aging and usually do not provide data about rootcauses of aging, such as increased thermal resistance of a given section of the junction-to-ambient heat flow path.

Degradation of the main heat flow path can be mapped by the so called *structure function* of the device package. In case of semiconductor power electronics the structure function can be revealed by the well-established thermal transient testing method [6], [7] and [8].

This structure function analysis along with the power cycling that mimics temperature cycling is the basis of the method that was used along with the versatile Viking Reliability Tester.

#### 2 Experimental

The system to utilize the described method was designed for flexible operating in various reliability testing environments, especially for long term power cycling and temperature cycling. As the related tests could last for several weeks, special requirements has to be fulfilled. The system has to operate continuously, even in case of test environment rearrangement or hardware error. Its operating has to be independent of the physical nature of the sample sets while different timings and powering could be able to be applied. Sample sets of identical physical nature have to be operated synchronously using same timing and powering settings. The system has to operate smoothly, without interruption at sample change or fault. The Viking Reliability Tester (VRT) was developed to meet these requirements and to serve as a low and medium power laboratory test environment.

#### 2.1 Test environment

The scheme and photo of the new integrated and fully automated reliability test environment is shown in Figure 1 and in Figure 2, respectively. The core of the system is the Viking Control Box. It is responsible for the control of the external hardware components, for the signal conditionings of the DUTs and for the measurement data storage.



Figure 1: General scheme of the Viking Reliability Tester (VRT)



Figure 2. Customized reliability tester for MOSFET power cycling

In the actual configuration a Mentor Graphics T3Ster transient tester, a general purpose power supply unit and a coldplate with a Julabo F25-MC refrigerated heating circulator are connected externally. The 5 MOSFETs are mounted onto a coldplate in the displayed setup. Between the DUTs and the coldplate, special high thermal resistance interface film was used. Next to the samples there is a custom built 24 relay measurement point selector.

#### 2.2 Test method and specimens

The passive temperature cycling is a heavily time and resource consuming procedure. For speeding up the test, active power cycling was used in a special way to mimic temperature cycling with triggering only defined failure modes.

To achieve this, two main guidelines were followed. First, the temperature gradient in the whole package was minimized while maximizing the temperature amplitude. Second, the load current was minimized while using soft ramp up. These ensure that the device sees a passive temperature cycling, triggering only thermally induced failure modes.

To maximize the dissipated power while keeping the forward current low, the gate and the drain were shorted forming a two pole device with a forward voltage close to the threshold voltage of the MOSFET. This setup needs minimal control hardware (no need for external gate voltage setup circuitry) while gives maximal forward voltage thus maximal power dissipation during low forward currents.

The load current was minimized (under 2 A in all modes) compared to the absolute maximum current ratings of the device (beyond 5 A). The forward voltage for this 2 pole device was 2.3 V, thus the total power dissipation was around 4.6 W. This yielded a 147.2 °C thermal amplitude for the cycling with the mentioned high thermal resistance (32 K/W) interface film under the devices. Such a film was used, that has got poor thermal performance but had outstanding thermal stability in preliminary measurements, thus not affecting the measured results. With the water cooled coldplate temperature set to  $T_{coldplate} = 25$  °C, the maximum temperature of the junction and of the whole package was  $T_i = \sim 175$  °C at the beginning of the cycling test. This was set to reach the absolute maximum operating temperature of the device. 30 seconds on and off time was used during the cycling. This was determined by the time constants from the first few thermal transient measurements during pre-stress testing, so that the whole package can reach the maximum and minimum temperature in every cycle.



Figure 3: Discrete Power MOSFETs from a recognized vendor with novel Ag sinter paste

The MOSFETs shown in Figure 3 were manufactured with newly developed high reliability and low thermal resistance Ag sinter paste from Infineon (20% porosity). The inner structure of the package is not available, however, with thermal transient measurements during active cycling, not only the layer structure can be examined but also useful assumptions can be made on the localization of the degradations.

#### 3 Results and discussion

#### 3.1 Package level degradation

The thermal reliability results are separated as there is package and chip level degradation too. The boundary conditions were selected not to trigger electrically induced failure modes thus using low current load with a soft ramp up. This way bond wires and inner layers are stressed only together with the whole structure. The temperature gradient in the structure is minimized with the poor thermal conductance of the interface film under the DUTs. From preliminary measurements it was reviled that the package has an extreme low thermal resistance, under 1 K/W. The total  $\sim$ 32 K/W for the assembly ensures that the package sees an even temperature distribution once the steady state is reached in every cycle. This way the active cycling acts as a passive temperature cycling but with much lower resources used.

Thermal transient measurements were carried out in every 5 thousand cycles until 30,000 cycles in order to have a higher resolution of the possible initial break-in period. Such effects were not visible but this gave a good picture on the repeatability of the measurements. Hereafter the standard step for thermal measurements was 10 thousand cycles. From these transient measurements, the overall junction to coldplate thermal resistance was determined. The time evolution of this can be seen in Figure 4.



Figure 4. Overall degradation of DUTs during power cycling

Until 40,000 cycles no remarkable degradation was observed. However, it was visible that some structural fatigue was started. At 50,000 cycles all samples started a slight but clearly detectable aging. This aging affected also the chip itself and the FR4 substrate but at this stage, only a joint result can be seen. After 70,000 cycles, all samples were functional and the slight change in thermal performance was not severe or fatal (smaller than 28.5% in  $R_{th}$  for the whole assembly). The K-factor calibration was carried out both at the beginning and at the end of the test procedure to verify that no electrical parameter related aging was induced. Further analysis of this indicator is not in the focus of this paper.

The chip level failures if there are any, are not visible in this joint diagram, because there can be several order of magnitudes between the caused resistance increases. Structure function analysis (carried out for all of the 5 samples) was used to differentiate between the aging and degradation of the chip and of the outer assembly (soldering, FR4, thermal interface film).

#### 3.2 Chip level degradation

The chip level aging mechanisms are in the range of 0.1 K/W. For examining such small deviations a very good voltage resolution is needed during transient testing, however increasing this would not help the signal to noise ratio. So the key is to produce such a high heating temperature or such a low overall thermal resistance during measurement to get low noise (under 3-5 LSB) during measurements. Thus, the maximum allowed temperature was selected during thermal transient testing, so the heating current used for testing was the same as the active cycling forward current. This gave maximum resolution during testing without disassembling the whole aging assembly. One could easily take the DUTs out of the sample holder to test them with the JEDEC standard dual interface measurement technique but this would affect the heatpath not to mention the lack of automation.

After the structure function evaluation the following structural degradations can be seen for a single sample.



Figure 5. Structure function time evolution

The two circles indicate the observed structural changes at the chip (red circle) and at the outer assembly (yellow circle) observed during cycling, in Figure 5. The aging induced structural change at the chip region is relatively small compared to the whole aging of the assembly. The effect of chip level fatigue can be better seen in Figure 6.

The overall thermal resistance increase of all of the 5 chips were in the range of 0.4-0.5 K/W. This slight change is not critical. As the junction to case thermal resistance is in the range of 0.9-1K/W, in real life conditions where adequate cooling would minimize the peak junction temperature, only minimal aging would arise.



Figure 6. Chip level structural degradation after 70,000 cycles

The testing of the medium power MOSFET samples with the Viking reliability test demonstrator clearly indicates that insitu thermal transient measurement during power cycling followed by structure function analysis can be successfully applied for reliability test evaluation and for fatigue tracking.

#### 4 Conclusion

A novel in situ reliability testing method was described in this paper for the characterization of thermal interface material aging effects in medium power MOSFET devices. The method uses minimal time and resource for mimicking temperature cycling with power cycling on samples with artificially prepared heatpath. The high thermal amplitude and the low electrical stress during cycling triggers only selected failure modes that can be proved and tracked with the subsequent thermal transient tests. The used reliability testing hardware and software system utilizes Mentor Graphics T3Ster transient tester to analyze the stress-induced deviations in the heat flow path from the pre-stress reference results. Measurement results collected during the active cycling of the DUTs at regular intervals serve as basis for the comparison. The details of the degradation process can be used as input for life-time prediction and for physics of failure modeling.

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#### **Implementation of Moisture Diffusion Model in Multi-material System Including Air Cavities**

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#### Abstract

Polymeric materials are often used in assembling and packaging MEMS devices. Polymers are prone to absorb moisture which can lead to reliability issues and different types of failures of the package. In contrast to the IC components cavities are usually essential part of the MEMS devices. The gas tightness of these cavities must be ensured for proper operation. This paper presents an extension of the moisture diffusion simulation methodology towards gas filled cavities embedded in multi material systems. The formulation involves the transformation of convection diffusion vapour transport equation into the form of a general transport equation which is solved by a commercially available simulation package. The implementation allows the coupling of additional physical models to the simulation such as condensation models.

#### 1 Introduction

The manufacturing of microelectromechanical systems (MEMS) typically requires several structural layers as well as integrated circuit (IC) components to be assembled together in the final product. Because of the technological requirements and cost saving efforts polymeric materials are often used in the process of assembly and packaging. Adhesives are used for bonding structural components together (e.g. wafer to wafer or wafer to substrate bonding), sealing the device by encapsulating them, or for protective layer for an individual die [1]. Several applications of adhesives in MEMS devices are listed in [1].

Polymeric materials are prone to absorb moisture if they are exposed to humid environment. This property can lead to reliability issues and different types of failures of the package. Such failure mechanisms identified in the literature [2] are the followings: popcorn cracking during oven reflow process; delamination due to the effect of polymer size change over long period of the time because of moisture absorption and swelling; electrochemical corrosion due to the presence of moisture and electric potential difference. Extensive testing of the surface mount IC packages are performed in order to determine the moisture sensitivity level (MSL) of the component, based on which the failure of the package can be avoided during assembly and product operation.

In order to investigate the effect of moisture simulation techniques for moisture diffusion in solid multi-material systems have been developed [3, 4, 5]. Simulation techniques can help to identify potential delamination areas and can led the development of decreasing the moisture sensitivity of the packages.

In contrast to the IC components cavities are usually essential part of the MEMS devices. The gas tightness of these cavities must be ensured for proper operation. Insufficient long term hermetic isolation of the MEMS cavity can lead to a package reliability issue and especially adhesive sealed MEMS packages are sensitive for vapour diffusion trough the package barrier. The absorption of moisture can also lead to water condensation in cavities which can result in unreliable operation, and failures of the device. Therefore detailed investigation of moisture transport process including the cavities may be necessary.

This paper presents an extension of the moisture diffusion simulation methodology towards gas filled cavities embedded in multi material systems. The formulation involves the transformation of convection diffusion vapour transport equation into the form of a general transport equation which is solved by a commercially available simulation package. The implementation allows the coupling of additional physical models to the simulation such as condensation models, advanced multiphase models etc. Additionally it also allows independent specification of material parameters for each solid, therefore not having the restrictions of a heat transfer analogy based solution such as in [4] where same activation energies and densities for the materials are required.

#### 2 Theory

#### 2.1 Governing equation of solution diffusion process

The transport of moisture can be described by a convection diffusion equation representing the mass conservation for vapor.

$$\frac{\partial C}{\partial t} + \nabla \cdot (C\mathbf{v}) = \nabla \cdot (D\nabla C) \tag{1}$$

where C [kg/m<sup>3</sup>] is the vapor concentration, v [m/s] is the velocity vector, D [m<sup>2</sup>/s] is the diffusion coefficient.

Equation (1) can be solved on a single material system by a wide variety of numerical methods such as finite difference, finite volume, finite element methods, etc. In case of a multi material systems one important aspect of the physical behavior is described by the Nernst distribution law, which states that at equilibrium conditions at the interface

$$\frac{C_{mat1}}{C_{mat2}} = \chi \tag{2}$$

where  $\chi$  is a constant at a given temperature. This law shows that the vapour concentration can be discontinuous at the interface, where different materials are joining. Therefore direct solution of (1) on a multi material system requires the specification of appropriate boundary conditions at the materials interface, and then solving (1) on each material separately with the coupled boundary conditions. However this is not the only way for generalizing the solution towards multi material systems. Based on Henrys law the following can be written:

$$S = \frac{C}{\phi} \tag{3}$$

Where  $\phi$  is the partial vapour pressure [Pa], and S is the vapour solubility of the material [kg/m<sup>3</sup>/Pa]. At the interface the partial vapor pressures must be equal:

$$\phi_{interface} = \frac{C_{mat1}}{S_{mat1}} = \frac{C_{mat1}}{S_{mat1}} \tag{4}$$

Showing the partial vapor pressure is a  $C^0$  continuous variable through the material system. Therefore substituting (3) into (1) the following transport equation can be obtained:

$$\frac{\partial S\phi}{\partial t} + \nabla \cdot \left( S\phi \mathbf{v} \right) = \nabla \cdot \left( D\nabla S\phi \right) \tag{5}$$

This equation with appropriate boundary conditions can be solved for the partial vapor pressure  $\phi$  on the whole multimaterial system without using special boundary treatment at the material interfaces. When the convection term of (5) is zero, because for example only solids are considered therefore  $\mathbf{v} \equiv 0$  the equation represents the so called solution diffusion problem [6], [7], The solution diffusion equation with simplifications is presented as "advanced analogy" in [4] because of the analogy to heat transfer equations.

The general transport equation for a scalar variable  $\phi'$  is written as follows in computational fluid dynamics (CFD) literature [8]:

$$\frac{\partial \rho \phi'}{\partial t} + \nabla \cdot \left( \rho \phi' \mathbf{v} \right) = \nabla \cdot \left( D \nabla \phi' \right) + S_{\phi'} \tag{6}$$

Here  $S_{\phi}$  is a source term of the equation. By comparing (5) and (6) one can immediately see an opportunity for implementing (5) as a general transport equation by defining  $\phi' \equiv \phi$  and embedding the differences between the two equations in  $S_{\phi'}$ .

In order to represent the same convection term in (5) and (6) one can use the formulation of effective solubility for the gas phase [Fan2010]:

$$S_{gas} = \frac{M_w}{R_u T} \tag{7}$$

Where  $M_w$  is the molecular weight of water,  $R_u$  is the universal gas constant and T is the temperature. For the state equation of the gas phase the incompressible ideal gas law can be used.

$$\rho_{.} = \frac{M_g p_{op}}{R_u T} \tag{8}$$

Where  $p_{op}$  is a constant reference pressure and  $M_g$  is the molecular weight of the gas.

#### 2.2 Implementation of the governing equations

Equation (6) is implemented with the appropriate source terms in the general purpose CFD solver ANSYS Fluent, using the ANSYS customization toolkit, Fluent user defined functions and scheme interface language. The material properties can be temperature dependent meaning that the moisture diffusion properties of the solid material as well as its density can be specified independently of each other. Therefore this general transport equation formulation opens a possibility for lifting some of the restrictions of the advanced analogy presented in [4], where the activation energy and density should be constant throughout the material system. Moreover the presented methodology with the effective solubility formulation and incompressible ideal gas model for the gas phase allows the computation of moisture transport in the cavities coupled with solid materials without implementing special boundary conditions.

#### 2.3 The material solubility and diffusivity coefficients

For solid phases the vapor diffusion and solubility coefficient is described by the commonly used Arrhenius forms:

$$D(T) = D_0 e^{\frac{E_d}{RT}} \tag{9}$$

$$S(T) = S_0 e^{\frac{E_s}{RT}}$$
(10)

D<sub>0</sub>, E<sub>d</sub>, S<sub>0</sub>, E<sub>s</sub> are material constants.

For fluid phases the vapor diffusion coefficient is defined with the following formula:

$$D(T) = D_m \left(\frac{T}{273}\right)^{D_e} \tag{11}$$

Based on literature [6], for vapor diffusion in air the fitted parameters are:

$$D_m = 2.16 \cdot 10^5$$
 (12)  
 $D_e = 1.8$ 

The solubility of the air phase computed with the equivalent model (7) which is derived from the assumption that the vapor phase behaves as an ideal gas in the cavity.

#### **3** Verification of the model implementation

Limited amount of data are available in the literature for verifying and validating moisture diffusion codes. One reference calculation that has been used for verification of the advanced analogy is presented in [4]. The reference case is a finite difference solution for the mass diffusion problem in a bimaterial system Fig 1. The materials are initialized to a constant temperature, and the outer walls are heated according to a temperature profile. Both materials has a thickness of 1 mm, density of 1000 kg/m<sup>3</sup>,  $E_s = 4 \times 10^4$  J/mol,  $E_d = 5 \times 10^4$  J/mol. The additional material properties of material 1 are c<sub>p</sub>=1000 J/kg/K,  $D_0 = 5 \times 10^{-3}$  and  $S_0 = 6 \times 10^{-10}$ . Material 2 has c<sub>p</sub>=500 J/kg/K,  $D_0 = 4 \times 10^{-3}$  and  $S_0 = 2 \times 10^{-10}$ . The computation mesh is the same as in [4] namely 200 cells used across each material piece.

The results of the computation in the form of temperature and vapor concentration distribution at different time instances are shown in Fig.2–5. The figures show that the implementation correctly reproduces the results obtained in the reference calculation. A discrepancy between the reference calculation and the current implementation can be observed in Fig. 4 close to the material interface location but the difference between the two calculations is very small. The verification case shows the correct implementation of the moisture diffusion transport on a solids system.





Figure 1: The bimaterial verification case [4].



Figure 2: Temperature distribution of the bimaterial system after1800s. Solid line shows the results of the current implementation, circles show the reference calculation.



Figure 3: Vapor concentration distribution of the bimaterial system after 1800s. Solid line shows the results of the current implementation, circles show the reference calculation



Figure 4: Temperature distribution of the bimaterial system after3600s. Solid line shows the results of the current implementation, circles show the reference calculation.



Figure 5: Vapor concentration distribution of the bimaterial system after 3600s. Solid line shows the results of the current implementation, circles show the reference calculation

#### 4 Model capabilities demonstration

As an example of the capabilities of the extended calculation methodology including air cavities, a coupled solid, air cavity and ambient air system is investigated. A 3D generalized MEMS device with air cavities is presented in Fig. 6. The device contains moisture impermeable materials as well as different types of polymers. The adhesive for mounting the IC and sealing the MEMS cap has material properties as follows:  $E_s = 4 \times 10^4$  J/mol,  $E_d = -3.7 \times 10^4$ J/mol,  $D_0 = 5 \times 10^{-6}$  and  $S_0 = 3 \times 10^{-11}$ ,  $\rho = 900$  kg/m<sup>3</sup>, specific heat  $c_p=2300$  J/kg/K, thermal conductivity,  $\lambda = 0.18$  W/m/K. The material properties of the outer casing polymer are:  $E_s = 4 \times 10^4$  J/mol,  $E_d = -3.6 \times 10^4$  J/mol,  $D_0 = 4 \times 10^{-6}$  and  $S_0 = 1 \times 10^{-10}$ ,  $\rho = 2719$  kg/m<sup>3</sup>, specific heat  $c_p=871$  J/kg/K, thermal conductivity,  $\lambda = 202$  W/m/K. The material properties of the other parts of the model are:  $\rho = 2719$  kg/m<sup>3</sup>, specific heat c<sub>p</sub>=871 J/kg/K, thermal conductivity,  $\lambda = 100$  W/m/K. The controller IC heat generation is about 0.5 mW.



Figure 6: The investigated 3D package geometry. Red parts are from polymeric materials. On the right is the MEMS assembly, on the left the controller IC.

The device is cooled with an air flow of 0.1 m/s directed toward the right surface of the package. The ambient temperature is 30°C, and the ambient partial vapor pressure is 2200 Pa. Initially 2200 Pa partial vapor pressure is patched for the internal cavities and polymeric materials. The simulation has been run until thermal equilibrium is reached. At this point the partial vapor pressure can be seen in Fig. 7 One can observe the elevated pressure in the adhesive below the IC chip, which is due to the elevated temperatures and slow diffusion process towards the edges of the chip. This elevated pressure can cause delamination type of failure of the package.



Figure 7: The partial vapor pressure distribution after thermal equilibrium reached. Elevated pressure can be seen below the IC. Unit is [Pa].

After the thermal equilibrium reached in the second phase of the simulation the ambient temperature is decreased to -10 °C as well as the partial vapor pressure is decreased to 240Pa. The flow field and the temperature distribution are shown in Fig. 8 at this stage.

The partial vapor pressure right before the start of the condensation in the MEMS cavity can be seen in Fig. 9. One can observe that the partial vapor pressure is higher in the cavity inside the MEMS assembly than in the outer cavity. In the second phase of the simulation the ambient vapor pressure is decreased and due to diffusion the amount of water vapor inside the cavities also decrease. The vapor transport is faster trough the large surface area outer casing than through the small cross section of the MEMS cap seal polymer, therefore the partial vapor pressure decreases more rapidly in the outer cavity than inside the MEMS assembly.



*Figure 8: The velocity vectors and the temperature distribution in the symmetry plane of the package.* 



Figure 9: The partial vapor pressure distribution in the symmetry plane right before the condensation starts in the MEMS cavity. Unit is [Pa].

The temperature distribution of the device can be seen in Fig. 10. at the time when the condensation starts. The right side of the MEMS assembly is slightly cooler than the left, showing that the most intense condensation can occur in the right part of the device. Condensation-evaporation model limits the partial vapour pressure to the saturation pressure at the local temperature in the gas phase.



Figure 10: The temperature distribution in the symmetry plane when the condensation starts in the mems cavity. Unit is [C].



Figure 11: Isosurface of condensed water concentration inside the MEMS cavity.

Condensed water isosurface can be seen in Fig. 11 at the expected location on the right side of the device. As time progress the amount of condensed water inside the cavity increases. The model also handles the evaporation of the water.

It must be pointed out that in the gas phase through the condensation mechanism the vapour concentration relative to the saturated vapour concentration is limited to 1, while in the solid phase there is no such a limitation exist in the presented implementation.

#### 5 Conclusions

With the help of formulating the mass conservation equation of the water vapor in a form of a general transport equation, the paper shows that the vapor convection-diffusion problem can be successfully solved for air cavities coupled with solid components. The solution procedure is implemented in a commercial CFD solver therefore modeling of additional physics phenomenon such as condensation can be investigated as well. The paper presents a verification of the method for bimaterial system using a reference literature data. The verification shows excellent matching with literature results. A complex 3D multi material MEMS system including polymer sealed air cavities and ambient convection air cooling is analyzed as a demonstration of the capabilities of the implemented model. The results shows an example of water condensation in the cavities, however quantitative analysis of the water condensation would be reasonable only if accurate geometry data of a real device is available alongside with the measured material properties of the used polymeric seals.

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### In-situ monitoring of interface delamination by local thermal transducers exemplified for a flip-chip package

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#### Abstract

We have developed a novel, rapid, robust and non-destructive experimental technique for in-situ monitoring of delamination of interfaces for electronic packages. The method is based on a simple thermal transducer matrix of so-called THIXELS (thermal pixels) which allows a spatially resolved real-time image of the current status of delamination. The transducers are small metal wire meanders which are driven and electrically read out using the well-known 3-omega method. This method has special advantages over other thermal contrast methods with respect to robustness, sensitivity and signal-to-noise ratio. Notable is the absence of cross-effects. The proof of concept has been furnished on an industry-grade flip-chip package with underfill on an organic substrate. The technique is especially powerful for buried interfaces, where time-honoured methods like scanning acoustic microscopy (SAM) cannot be applied. As the technique effectively performs a thermal diffusivity sensitive scan, it may not only be useful for stress testing during package qualification, but sensor applications on other fields of health monitoring seem also possible.

#### 1. Introduction and Motivation

Today, there is no non-destructive, simple, inexpensive and yet accurate in-situ monitoring technique for cracks and delamination available for routine use in electronic package testing. However, such a method is highly desirable, as stress testing is part of every qualification programme in industry and interface delamination a prominent failure mode [1]. Rapid failure analytical techniques which allow introspect and easy-to-interpret information on adhesion loss during stress testing, analogous to e.g. electrical resistance monitoring as indicator for solder joint integrity, would enable considerable speed up of the development process of advanced packaging technologies, especially also for situations where not even classical ex-situ methods like scanning acoustic microscopy or pulse phase thermography are applicable (e.g. for inaccessible chip surfaces buried by an attached heat sink, etc).

So this paper proposes a radically new, possibly inexpensive and practical approach for in-situ detection and monitoring of (interface) cracks in electronic packages as a nondestructive technique. The technique is based on the detection of local thermal diffusivity variations caused by propagating cracks above a thermally sensitive structure which can transform this information into electrical signals for remote readout. An array of these thermo-electric transducers form a matrix of so-called *THIXELS* (thermal pixels), designed to produce in-situ proximity images as from a "delamination camera". These thermo-electrical transducers are based on the 3-Omega ( $3\omega$ ) method. In this method, the  $3\omega$ -structure or Thixel serves as emitter and receiver of propagating, damped thermal waves which are reflected e.g. by a crack, then producing an alteration in the electrical output voltage.



**Figure 1:** *Example SAM image of typical delamination* (*highlighted areas*) at the interface between underfill (UF) and chip in a flip chip (FC) device.

In order to furnish proof of this novel concept and put it to a test we have conducted a simulative and experimental study on an industry-grade flip-chip device under autoclave testing conditions. A more introspect introduction into the idea of the Thixel-matrix and calibration has been published by some of the authors earlier in [2].

#### 2. The 3-Omega Method

The 3-Omega method [3] is a well-known method for precision measurement for thermal conductivity  $\kappa$  of materials. A typical set-up is given in figure 2, where a pure metal structure is patterned on a substrate. Layouted as a 4-point measurement and driven by an AC current with angular frequency  $\omega$ , it produces a voltage U3 $\omega$  oscillating

with  $3\omega$ , which is a measure of the local temperature of the transducer according to equation 1. For further reading please refer to [4].



**Figure 2**: Typical layout of a  $3\omega$ -structure as used in many applications for precision measurement of  $\kappa$ .

As will become apparent, we will not use the 3-Omega method for precision measurement of a thermal conductivity, but as a qualitative sensor of maximum sensitivity of local changes in the thermal diffusivity of the surrounding materials.

$$U(t) = I(t) \cdot R(t) = I_0 R_0 \cos(\omega t) +$$
  
+ 
$$\frac{1}{2} I_0 R_0 \alpha T_{2\omega} [\cos(\omega t - \varphi) + \cos(3\omega t - \varphi)].$$
(1)

As the 3-Omega-measurement is continuous and periodic, it is very suitable for lock-in amplification, boosting the signal-to-noise ratio. Further robustness is given to the method by the fact that the response signal is located exactly on the  $3\omega$  frequency in the spectrum.

#### 3. Concept, Design and Manufacturing

The governing idea is shown in figure 3. If a crack approaches a sensor ( $3\omega$ -transceiver), the thermal wave emitted by it will be influenced. The thermal wave travels from the  $3\omega$ -transceiver into the surrounding materials. Then, the wave is reflected by outer and inner surfaces, i.e. material interfaces and cracks in particular. This reflection, and thus its effect on the detectable signal, should be most prominent within the radius of the thermal penetration depth which is assumed to be close to the thermal wave length  $\lambda$  given in equation 2

$$\lambda = 2\pi \sqrt{D/\omega} \,, \tag{2}$$

Where D is the diffusivity of the material.



**Figure 3:** Principle of the  $3\omega$ -method for in-situ crack and delamination detection.

The thermal wave length depends thus not only on the material, but also on the frequency of the AC drive signal [2]. This fact can be used to tune the probing depth of the sensor to within a range from several to hundreds of microns, depending on the materials. So should a crack propagate through the polymer, the wave would be reflected at the newly generated interface and reach, due to the shorted thermal path d, again the structure, which would then result in a temperature increase, i.e. the upward cooling path is blocked by the crack. So one should expect that if the thermal path d is smaller than the thermal wave length  $\lambda$ , the oscillating temperature  $T_{2\omega}$  will rise and also the  $U_{3\omega}$  signal resulting in a detection of the crack.

Table 1:	Used	material	properties.
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Material	k [W/mK]	c <sub>p</sub> [J/gK]	ρ <b>[g/cm3]</b>	D [cm2/s]	α <b>[1/K]</b>
Silicon	149	0.7	2.33	0.9135	
Aluminium	230	0.92	2.7	0.9259	3.7 e-3
SiO <sub>2</sub>	1.4	0.75	2.2	0.0085	
Epoxy Resin	0.25	2	1.3	0.0010	

First, Finite Element (FE) simulations were conducted to design the sensor and the possibility to arrange them into a thermal pixel array to optimize geometry and signal characteristics of the  $3\omega$ -structure. Therefore, material properties in table 1 were used.



**Figure 4:** 3D FE-model numerical results of the  $U_{3\omega}$ -signal for  $f_{th} = 5$  Hz excitation frequency for Silicon and glass substrate. Note the much higher signal output for SiO<sub>2</sub>: Signal increases ca. 35 % after interface delamination. Thumbnails indicate the momentary delamination front w.r.t. to the 3 $\omega$ -transducer (blue rectangle).

The result of the 3D FE-simulations is seen in figure 4: Very nicely one observes the effect of reduced upward heat flux due to the propagating crack. The effect amounts to an approximately 36 % increase in the signal voltage, predicted to be in the two-digit millivolt range. Both would mean very robust and reliable detection by standard equipment. The detection range is shown to be very localized to the 3 $\infty$ -sensor (meander extends from L =  $-50 \ \mu m$  to  $+50 \ \mu m$  in figure 4), with the signal decaying rapidly with distance from it. This corresponds to a calculated thermal wave

length in the range of  $\lambda \approx 100 \ \mu\text{m}$  in polymers for the given frequencies. All that would very much favor this principle and geometry for the targeted application. (For more details on the design see again [2]).



Pd / Au Patternplating Ni Passivation PE-CVD SiO<sub>2</sub> 0.5 μm Aluminum 0.1 μm (Meander and circuits)





**Figure 6:** Layout of two different  $3\omega$ -testchips A and B. Chip size  $A_c = 10 \times 10 \text{ mm}^2$ .  $3\omega$ -structures (red square) are designed as meanders with  $R_0 = 100 \Omega$ .  $A = 100 \times 100 \mu m^2$ .

Next, a simple test chip with a Thixel matrix was fabricated, using 100 nm thick sputtered aluminium meanders as  $3\omega$  structures which were protected by 500 nm thick CVD glass to mimic a real chip surface. As substrate a glass wafer was used for reasons of better sensitivity compared to Silicon (c.f. figure 4). For dimensions and materials see the schematics in figure 5 and 6.



**Figure 7:** Optical microscope image of  $3\omega$ -structure (Thixel) and contact pads (left). Chip variant B on PCB with Au-wire bond connections ready for encapsulation (right). FIB-cut (bottom).

The chip is designed with a UBM to accept solder bumps and can be mounted face down as a flip-chip device. The result of the successful fabrication can be seen in figure 7.

#### 4. Proof-of-Concept on Flip-Chip Package

For that purpose we decided to put the method to a test under industrial boundary conditions, i.e. with an industrygrade package and a pressure cooker (PC) / autoclave test. As demonstrator a flip-chip package on organic substrate (FR-4) with capillary underfill (UF) was chosen. All surface finishes, materials and processes were chosen as under realistic manufacturing conditions. The result can be seen in figure 17 (left), featuring also some voids in the UF.



**Figure 8:** Glass test chip A (c.f. figure 9) with 3 $\omega$ -structures mounted as flip-chip on organic substrate: (Left) the structures and wiring are visible through the glass, (right) SAM after 24 h PC testing: delamination is clearly visible for all test structures (arrows).

Then, the chips underwent PC testing (T = 121 °C, H = 100 %rh, p = 2 bar) for t = 24 hours. This test was chosen to highly accelerate delamination at the interfaces w.r.t. a thermal cycling test. The results after failure analysis can be seen in figure 8 to the right: The area under all  $3\omega$ -structures is clearly delaminated as can be seen in the scanning acoustic microscope, see also the set-in arrows. This is a bit unfortunate, as one would have liked to see partially-delaminated  $3\omega$ -structures and successive delamination during the test and the effect of moisture saturated UF on sensor sensitivity. Still, there is clear evidence for a gradual delamination (see [2]).



**Figure 9:** *Proof of concept: Characteristic curve of one Thixel: Unequivocal detection of delamination is possible.* 

Now,  $U_{3\omega}$  was compared before and after PC testing. For this evaluation, only  $3\omega$ -structures with no neighboring voids were chosen. The result is plotted in figure 9 for three representative sensors: A clear separation between the curves for undamaged and delaminated areas should be noted. Then, values for undamaged interfaces are very reproducible for the whole scanned frequency spectrum. (This will later change in the presence of voids).

Taking the scatter of the values for both situations into account, N = 27 3 $\infty$ -structures were evaluated statistically for two relevant frequencies f = 10 Hz and f = 200 Hz, the first for its maximum absolute U3 $\omega$  output, the second for a maximum difference voltage. The result can be seen in figure 10.



**Figure 10:**  $U_{3\omega}$  signal separation for proof of unequivocal detection of delamination (nok) w.r.t. perfect adhesion and no voids (ok) for a statistical lot of N = 27 3  $\omega$ -structures. Given are mean values and min/max bars for two different excitation frequencies f.

Also, the recorded U3w values agree really well with the simulatively predicted ones as given in figure 11.



**Figure 11:** Good agreement of simulative prediction with experimental average for glass substrate and f = 10 Hz. This should be compared to figure 4.

#### 5. Unambiguous Detection and Parasitic Effects of Voids

One interesting feature is that delamination can be clearly differentiated from voids. In figure 12 data for the undamaged interface but partly with voids (all solid lines) are compared to delaminated areas (dotted lines). As expected, voids have a similar effect as delamination, namely to (partially) block the heat path across the interface into the UF, thus causing a temperature increase and consequently a  $U_{3\omega}$  increase. An intuitive correlation is validated in the experiment: The closer the void to the sensor (b) or even the more overlap the sensor has with the void (c), the higher the  $U_{3\omega}$  signal to the point where it merges with the curves for the delaminated areas (d). However, this is only true for low frequencies (f < 500 Hz). At higher frequencies (e), however, voids seem to leave a different signature than a delamination and a clear distinction seems possible. This is due to the fact that the sensors at high frequencies, i.e. smaller thermal penetration depths, probe only their immediate surroundings and hence the effect of a void would be larger there.



**Figure 12:** Measured curves for underfill with imperfections (voids) different situations: (a) undamaged and no voids, (b) undamaged with voids at ca. 100  $\mu$ m distance, (c) pristine with voids partially overlapping with 3  $\omega$ -structure, (d) after PC testing with various delaminated locations (dotted curves). At high frequencies f > 500 Hz one can discern a distinction between void and delamination (e), see arrows.

So even if for a mature technology voids should be rare, this method possibly allows their detection separately from the identification, onset and propagation of interface cracks, i.e. delamination.

What is more, the method allows also to make statements about the void or crack configuration or even shape above the sensor when the spectral response is investigated in more detail. For that purpose, FE simulations were carried out. A brick-shaped void is modelled and held at different distances *b* above the Thixel as depicted in the inset in figure 13.  $U3\omega$  is normalized w.r.t. the undamaged flip-chip configuration and plotted versus the excitation frequency  $f_1$ .



**Figure 13:** Simulation of void in polymer at different distances b above the Thixel. A characteristic maximum in the normalised  $U3\omega$  curve appears.

As one can see, the signal amplitude goes down with increasing distance which is to be expected as the configuration converges to the undamaged one. But an interesting feature is that there is a clear maximum that gets shifted to smaller frequencies for larger distances. This also is in line with the thermal wave length which defines the probing length or range of the Thixel and decreases with frequency as explained in section 3.



**Figure 14:** *This maximum correlates well with the vertical distance between the void and the Thixel.* 

Upon plotting the frequency vs distance for the maxima one obtains a nomogram (figure 14) which should enable to correlate distance with the frequency maximum in measurements. This is investigated now for two void configurations and a delaminated surface as given by the images in figure 15.

Also the experimental curves feature a maximum voltage as predicted by the simulations. A Thixel fully covered by a void (cfg. A) increases the amplitude significantly as expected by severing the heat path. A partially covered void (cfg. B) increases the amplitude not so much. According to the results of figure 14, void A should be closer to the Thixel than void B, which is difficult to tell without crosssectioning. As for the delaminated area (cfg. C), there should be some polymer residue of a few microns still on the surface. This needs to be looked into in more detail in the future.



**Figure 15:** *Experimental curves (solid lines) for different void configurations and delamination (optical micrographs) and simulation result for a brick shaped void according to cfg. A (dashed line).* 

Still, the simulated (dashed) curve of a brick-shaped void above the Thixel reproduces the main features of the curve to a good degree. The amplitude match is perfect, at the higher frequencies shape or interface effects may play a role.

#### 6. Measurement Speed, Accuracy Scaling & Robustness

For routine industrial application the here proposed measurement must be comparable in scope with other failure analytical measurements as e.g. online electrical resistance monitoring of four-point Kelvin structures or Daisy Chain structures to check bump integrity. Such measurements may take less than one second per bump.

To estimate the time duration of one U3 $\omega$  measurement, including lock-in averaging, measurement convergence and an excitation frequency specific processing scheme we have conducted a series of measurements to find out a minimum integration time during lock-in. The result of this is shown in figure 16: As expected, error bars decrease with increasing integration time. We see that both mean value as well as standard deviation stay within a band of  $\delta U = \pm 15 \ \mu V$ , even at low integration times of several tens of milliseconds. This is more than two orders of magnitude below the given signal separation in table 3, i.e. a very good signal to noise ratio.

This signifies that for this set of input variables one  $3\omega$ structure can be remotely read out within t < 100 ms with great safety margin at the frequencies of interest. However, all these values scale with excitation current, i.e. with lower currents the margins become much smaller and the lock-in integration time might have to be larger to extract the signal from the background noise. The same would be true for using silicon chips instead of glass chips. Eventually, there will be a trade-off between low excitation currents (low thermal load) on one hand and high sensitivity (small integration times) on the other. As it looks now, there is still much headroom.



**Figure 16:** Integration time during lock-in procedure and resulting measurement accuracy at f = 100 Hz for a typical  $3\omega$ -structure. Error bars are standard deviations from six measurements à 10 samplings during integration. Note the y-axis spans here only  $U_{3\omega} = 30 \ \mu V$ . Mean value fluctuations should be due to the steep temperature increase at the start of the measurement.

So the obtained measurement time is well comparable, or even better, to time honored failure analytical methods. This would allow, using the geometry and materials given above, screening of a 1 cm<sup>2</sup> chip down 2 mm into the peripheral bump rows (region of interest) within < 1 min. This would be fully compatible with routine failure analysis during product development in industry.

#### 7. Conclusions and Outlook

We have proposed and furnished the proof of concept for a radically new, non-destructive, possibly inexpensive and practical failure analytical technique with intuitive contrast for local in-situ detection and monitoring of (interface) cracks in electronic packages on an industry-grade package. Thereby, we have introduced the new concept of the *Thixel* as a thermal pixel of a "delamination camera". We have shown by experiment, simulation and technology, the main results:

- The 3-Omega Thixels are able to clearly identify a crack front propagating above them: At an optimum excitation frequency, the contemplated polymer / glass interface provides a usable contrast change of more than 20% upon passing of a crack front, allowing unequivocal detection and differentiation from other structural defects such as e.g. voids.
- Experimental and simulated values of the 3-Omega output voltage show very good correlation.
- The delamination front detected by the Thixels is consistent with the SAM result used as benchmark.

- The method is very local (here: ca. 200 µm range at 200 Hz) preventing thermal sensor to sensor crosstalk. The spatial resolution is thus only limited by the pitch, the spatial extension of the Thixels, the involved materials and the excitation frequency.
- The detectable 3-Omega signal is in the two-digit millivolt range. This allows a very good signal to noise ratio and robust remote electrical readout and lock-in amplification by standard electronics.
- The method is insensitive to cross-effects, as e.g. moisture ingress and swelling.
- The chip technology is very simple and inexpensive, so the method can easily adapted to specific devices. It opens e.g. a way to the design for testability for SiP and online generation of lifetime data.

Current work concentrates on a fast read-out scheme for a  $n \ge n$  Thixel matrix camera chip and an extension to other interesting packages as e.g. microprocessors and an optimisation of operational parameters. We believe that there will be interesting applications in future failure analysis in competition to the time honoured methods.

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**SESSION 12** 

# **SESSION 12** Thermal Characterization and Modeling

#### **Design of Heated-micro-resonator Rings**

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#### Abstract

To facilitate the design the heated-micro-resonator rings, we develop a numerical model. Particularly, an etching model based on a diffusion equation is implemented to distinguish the etched and non-etched regions. The simulations reveal that air trenches can significantly increase the thermal resistance and, as a result, reduce the power consumed in the heater to get the same tuning performance. It is found that the tunability of MRR is exponentially enhanced with the underetch level as RL > 0.825, whereas the tuning efficiency is almost the same, as RL < 0.825. The tuning efficiency is ~0.1 nm/mW without air trenches, but it becomes 20X larger at the etched-through extreme.

#### 1 Introduction

Tunable semiconductor lasers have been of great interest to enable future flexible and scalable optical networks and to achieve more bandwidth and services/€ [1,2]. Among them, microring resonator (MRR) tuned lasers have received much attention due to wide tunability, compact size, and easy realization of large-scale photonic integrations [3]. Matsuo and Segawa [4] reported that a MRR tuned laser exhibiting a 50-nm tuning range with a side-mode suppression of 50 dB. Typically, the thermo-optic effect is used to control the MRR. Joule heaters are employed to manipulate the local temperature (T) of the microring structure and change the waveguide materials refractive index  $(n_r)$  to effectively control the resonant wavelength ( $\lambda$ ). However, local temperature control using integrated heaters can be highly energy inefficient (small  $d\lambda/dP$ ) due to a significant amount of generated heat (P) being dissipated to the substrate through the relatively high thermal conductivity substrate material. As a result, the power requirements for thermooptic MRR tuning can become a significant portion of a device power budget. To mitigate this issue, a strategy of locally increasing the MRR thermal resistance by introducing etched "air trenches" has been pursued [8]. This approach has been demonstrated to be very effective, resulting in an order of magnitude increase in tuning efficiency (10× larger  $d\lambda/dP$ ) [8].

In the paper, we will first give an example of microring resonators in a real photonic device. Next, we develop a numerical modeling strategy for capturing the air trench etch process and subsequent thermal tuning efficiency with the aim of optimizing the tuning efficiency with respect to the air trench fabrication process. The performance of microring resonators with/without air trenches is then discussed.

#### 2 Example of Microring Resonators in a Real Photonic Device

Heated microring resonators are currently being used to finely tune the wavelength of our hybrid laser output using the Vernier effect for use in a silicon photonics platform [1, 8]. Figure 1 provides a schematic of a typical design incorporating two MRRs to tune the wavelength of the laser. On the MRR, a nickel-chrome (NiCr) heater using Joule effect is employed to vary the local temperature around the waveguide of the MRR to change its refractive index and, hence, its resonance wavelength. The MRR components used for wavelength tuning have been characterized, showing that ~150 mW of power is required to achieve the full wavelength tuning range (~40nm, which is standard for C-band telecom applications). This has been corroborated by numerical simulations, which show that heat loss through the substrate is the key reason for these large power dissipation requirements and highlights the need for thermal isolation of the MRRs from the substrate.



Figure 1: Schematic of a tunable laser structure. BM denotes the Bragg mirrors, GC represents the vertical grating couplers, A is the active region, C is the metal contact,  $R_1$  is the first microring and  $R_2$  is the second microring.

#### **3 METHODOLOGY**

Figure 2 depicts one of MRRs having air trenches. The microring is 450nm in width and 220nm in height and are enclosed by silica (SiO<sub>2</sub>). The ring resonator is in a racetrack resonator shape and has several turns of  $\sim 5\mu$ m in radius. The coupling coefficient of the MRR versus the input/output waveguides is ~0.05. The metallic heater with a typical ohmic resistance of ~100  $\Omega$  sits atop the MRR.



Figure 2: Microscopic image of MRR with wet etched air trenches.

A numerical model of the MRR structure used in the tunable laser source was developed to thoroughly investigate the thermal performance of this structure in the presence of air trenches. The simulated geometry is shown in Figure 3. A Si ring resonator structure formed in the device layer of the SOI is situated below a ~1 $\mu$ m layer of SiO<sub>2</sub>. A NiCr heater ring with the ~100 nm thickness sits atop. The model is driven by injecting current into the metal pad A, while the pad B is electrically specified as ground. Thermally, all boundaries are adiabatic except for the bottom of the SOI substrate, which is fixed at a temperature of  $T_{sub} = 300$  K. The material properties used in the simulation are given in Table 1.



(b)

(a)

Figure 4: Geometry of the simulated MRR. (a) Isometric view; (b) Top view.

Table 1: Thermal and electrical properties used to model the MRR structure [5–7]

Material	<i>k</i> (W/m-K)	σ (S/m)
NiCr	11.3	8×10 <sup>5</sup>
Air	0.02	_
Si	148×(T/300) <sup>-1.3</sup>	_
SiO <sub>2</sub>	1.38×(T/300) <sup>0.33</sup>	_

Two sets of governing equations were considered for this model: (1) an electro-thermal model and (2) an etching model, which are described in detail next. The etching model was first solved and the size of the etched region was controlled through the choice of various solution parameters. The purpose of this was to develop a thorough understanding of the effect of under-etching on the thermal performance of the MRR device.

**Electro-thermal modelling** – A Joule heating model was implemented to capture the distribution of heat generated in a resistive NiCr alloy heater used to tune the temperature and, hence, refractive index of a Si ring resonator structure. Numerically, the temperature and electric current distributions are obtained by solving the governing equations.

$$\nabla \cdot [-k(T)\nabla T] = \mathbf{j} \cdot \mathbf{E}$$
 Eq. 1

where k is thermal conductivity, **j** is the current flux and **E** is the potential field determined from solution to the charge conservation equation

$$\nabla \cdot \mathbf{j} = 0$$
 Eq. 2

**Etching modelling** – We developed a diffusion-controlled etching model to differentiate the etched and non-etched regions [9]. The mass concentration distribution of the etching component in the etchant, c, is determined by solving a diffusion equation

$$\frac{\partial c}{\partial t} = D\nabla^2 c \qquad \qquad \text{Eq. 3}$$

where *t* is time and *D* is the isotropic diffusion coefficient. The schematic in Figure 4 details the approach taken where the areas in which etchant is initially applied through the etch mask were specified (see the area represented by 'Initial Mask' in Figure 4) and then Eq. 3 was solved to find the concentration distribution after a given etch time. The trench formed by the etching process was defined by the resulting iso-concentration surface as demonstrated in Figure 4. This surface is defined where the concentration at the front). The domain with  $c > c_F$  represents the area where the material has been etched away. It should be also

pointed out that the etched region is not geometrically removed, but is treated as a material of poor thermal conductivity. Figure 3 demonstrates the result of this etching model for a simplified case where a source surface was implemented with *D* set to 0.0001 and the case ran for 2 minutes. In Figure 4, k = 0.02 W/mK (air) inside the trench front, which was defined using  $c_F = 0.9$ . In addition, the thermal conductivity around the trench front is smoothed to mitigate the mathematical discontinuity appearing at the interface.



Figure 4: Schematic of a diffusion-controlled etching model for a simple rectangular mask geometry. Note the trench front corresponds to  $C_F = 0.9$ .

#### 4 Results

The simulated results for the MRR design without air trenches are given in Figure 5. Here,  $dT = T_r - T_{sub}$ , where  $T_{\rm sub} = 300$  K. Note that the absolute temperature ( $T_r$ ) appears in Figure 5. The simulation reveals that a low temperature region occurs at the location where the heater joins the contact pads. However, the remainder of the heater has a uniform temperature (~560 K). Figure 5b shows that the simulated dT/dP = 3138.1 K/W for the case having contact pads and temperature-dependent material properties. Note that the presence of the contact pads was considered due to the fact that a certain mount of heat is dissipated through them and 25% reduction in dT/dP occurs as shown in Figure 5. Since the simulation of heated-phase sections discussed above only reveals the thermal performance, the measurement cannot yield the optical performance directly. To quantitatively correlate these two aspects, we derive a mathematical relationship of thermal resistance (dT/dP) with the wavelength shift against the power consumption  $(d\lambda/dP)$ , as detailed in Appendix.

The simulated results for the MRR design without air trenches are given in Figure 5. Here,  $dT = T_r - T_{sub}$ , where  $T_{sub} = 300$  K. Note that the absolute temperature  $(T_r)$  appears in Figure 5. The simulation reveals that a low temperature region occurs at the location where the heater joins the contact pads. However, the remainder of the heater has a uniform temperature (~560 K). Figure 5b shows that the simulated dT/dP = 3138.1 K/W for the case having contact pads and temperature-dependent material properties. Note that the presence of the contact pads was considered due to the fact that a certain amount of heat is dissipated through them, leading to a 25% reduction in dT/dP occurring compared to the case without contact pads(as shown in

Figure 5). Since the simulation of heated-phase sections discussed above only reveals the thermal performance, the measurement cannot yield the optical performance directly. To quantitatively correlate these two aspects, we derive a mathematical relationship of thermal resistance (dT/dP) with the wavelength shift against the power consumption  $(d\lambda/dP)$ , as detailed in Appendix.







(b)

Figure 5: (a) Simulated temperature distribution along the tunable ring at heater power P = 60 mW; (b) The simulated ring temperature variation against the heater power. Note that no air trenches are considered in the simulations.

The simulated ring temperature for the designs with and without air trenches is shown in Figure 6. It should be noted that the underetch level is quantitatively defined as RL =  $(L_R-l)/L_R$  as schematically explained in Figure 6a. In particular, RL = 1 means the etched-through extreme. Figure 6b reveals that air trenches can significantly increase the thermal resistance and consequently less heater power is consumed to achieve the same tuning performance. Apparently, the larger heater powers yield the unrealistic MRR temperature (larger than the melting temperature of silicon), which would not happen in practice in that the power needed to achieve the targeted wavelength range is substantially smaller. Moreover, we studied the tuning efficiency at different underetch levels (RL). As revealed in Figure 7, the tunability of MRR is exponentially enhanced with the underetch level as the etching front reaches MRR at  $RL = \sim 0.825$  (denoted by the red line in Figure 7). However, as RL < 0.825, the tuning efficiency is almost the same. Particularly, the tuning efficiency is only ~0.1 nm/mW without air trenches, but it becomes 20X larger at the etched-through extreme (RL = 1).



*(a)* 



(b)

Figure 6: (a) Schematic of underetch level. Here  $RL = (L_R - l)/L_R$ . (b) Function of MRR mean temperature versus power consumption at different underetch levels (RL).



Figure 7: Function of tuning efficiency versus underetch level. Note that  $d\lambda/dT = 8.76 \times 10^{-2}$  nm/K in Eq. 5 is used based on the typical MRR configuration.

#### 5 Conclusions

To aid in the design of energy efficient microring resonators, we developed a novel numerical model for the air trench design that captures an isotropic etch process and the resulting tuning efficiency. A mathematical relationship of the simulated thermal resistance with the measure wavelength shift was also derived to enable quantitatively comparing the thermal performance with the optical performance. The simulated results show that air trenches can significantly increase the thermal resistance and, as a result, reduce the power consumed in the heater to get the same tuning performance. It is also found that the tunability of MRR is exponentially enhanced with the underetch level as RL > 0.825, whereas the tuning efficiency is almost the same, as RL < 0.825. The tuning efficiency is ~0.1 nm/mW without air trenches, but it becomes 20X larger at the etched-through extreme.

#### **Appendix: Derivation of Thermal Resistance**

In general, optical measurements only yield the function of the wavelength shift with the power consumption  $(d\lambda/dP)$ . It is difficult to be directly used for comparing with the simulated thermal resistance (dT/dP). To correlate these two parameters, we mathematically decompose the thermal resistance as

$$\frac{dT}{dP} = \frac{d\lambda}{dP} \times \frac{1}{d\lambda/dT}$$
 Eq. 4

where  $d\lambda/dT$  represents the wavelength shift vs. temperature, which is related to the material properties of the ring resonator and the confinement factor ( $\gamma$ ) and is expressed as

$$\frac{d\lambda}{dT} = \left(\frac{d\lambda}{dn_{eff}}\right) \times \left(\gamma \frac{dn_{\rm Si}}{dT} + (1-\gamma) \frac{dn_{\rm SiO2}}{dT}\right) \quad \text{Eq. 5}$$

where  $n_{eff}$  is the effective refractive index and  $n_{Si}$  and  $n_{SiO2}$ are the temperature-dependent refractive indices of silicon and silicon dioxide respectively. Because the optical path length difference (*OPD*) of a ring resonator is given as *OPD*  $= n_{eff} \times L = m \times \lambda$ , there is a linear relationship between  $n_{eff}$ with  $\lambda$ 

$$\frac{d\lambda}{dn_{eff}} = \frac{L}{m}$$
 Eq. 6

where L is the perimeter of the ring resonator and m is the mode number at the designed wavelength.

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#### Novel Test Stand for Thermal Diffusivity Measurement of Bulk and Thin Films

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#### Abstract

This paper deals with the development of a new test stand for thermal diffusivity measurement based on Ångström's method (called TIMAwave<sup>TM</sup>). The concept of the test stand has been proved by FE simulation and experiments on standard samples. The test stand has been realized and integrated into the hardware of the already existing test stand LaTIMA<sup>TM</sup>, which was developed for the measurement of thermal conductivity of highly conductive materials. The combination of these two test stands in one device is a great advantage, since the diffusivity and the conductivity of a sample can be measured at one specimen in one device. The results allow the calculation of the specific heat capacity or the density of the sample. Several materials have been characterized by using the new test stand. Some selected results will be discussed in this paper.

#### 1 Introduction

The knowledge about thermal properties is a key for many material applications in many fields like high power application, consumer electronics or automotive. Finding new methods is essential for the characterization of the new materials since the structure, sizes and thicknesses are getting smaller and smaller. Two innovative test stands based on the steady state method have been developed in recent years for in-plane and out-of-plane characterization of TIMs, die attaches, substrates etc. The TIMA<sup>TM</sup> test stand which is based on the standard ASTM 5470 is suitable for characterization of a relatively wide range of material types and provide high flexibility of sample geometry, however is limited for material with low and medium thermal conductivity. A systematic study of the limitations of TIMATM has been reported in [1] and showed that the smallest thermal resistance value, which can be measured with measurement error below 10%, is around 1 mm<sup>2</sup>K/W. This value corresponds, for example, to materials with 50 W/mK thermal conductivity in 50µm thickness. Therefore, a further test stand (LaTIMATM) has been developed which is based on a modified application of the same measurement principle [2]. The LaTIMATM test stand allows direct measurement of thermal conductivity of high thermally conductive samples such as metals, sintered mono metals, substrates etc. different Materials have been characterized by LaTIMATM test stand [3].

This paper deals with the development of a new test stand for the measurement of thermal diffusivity of bulk samples, multi-layer samples, thin films etc. The new test stand has been named *TIMAwave*<sup>TM</sup>, as it is part of *TIMA*<sup>TM</sup> family and its measurement principle is based on thermal wave theory. The main advantages of the *TIMAwave*<sup>TM</sup> test stand are:

- High flexibility in sample geometry
- Broad spectrum of sample thermal diffusivity
- Knowledge of sample geometry not necessary
- Contactless temperature measurement
- No further temperature sensors needed
- Quick and reproducible measurement

#### 2 Methodology

The new test stand is based on Ångström's method. Modulated heat (periodic square or sinus wave) is applied to one end of a semi-infinite sample, while the other end is kept in a constant temperature (see Figure 1). The modulated heat flow through the sample results in the form of a 1D-damped thermal wave, which can be described by the following equation [4]:

$$T(x,t) = A \cdot e^{-\frac{x}{\mu}} \cos\left(\omega t - \frac{x}{\mu}\right) \qquad (1)$$

where  $\mu$  is thermal diffusion length, expressed by

$$\mu = \sqrt{\frac{2 \cdot \lambda}{\omega \cdot \rho \cdot C_P}} = \sqrt{\frac{2 \cdot \alpha}{\omega}}$$
(2)

 $\lambda$  is thermal conductivity,  $\rho$  is density,  $C_P$  is specific heat capacity,  $\omega$  is modulation frequency and  $\alpha$  is thermal diffusivity.

The thermal diffusion length  $\mu$  is defined as:

on Thermal Investigations of ICs and Systems ]]

$$\mu = \frac{1}{k} \quad \Longrightarrow \quad k = \sqrt{\frac{\omega}{2 \cdot \alpha}} \tag{3}$$

where k is the wave number, so the equation (1) can be written in the form:

$$T(x,t) = A \cdot e^{-k \cdot x} \cos(\omega t - k \cdot x)$$
<sup>(4)</sup>

The temperature along the sample is measured contactless by an infrared camera. The amplitude and the phase per pixel of the damped thermal wave are determined by lock-in processing and rendered to images mapping the amplitude and the phase of the sample surface. As can be seen in equation (3) and equation (4) the thermal diffusivity ( $\alpha$ ) is connected with the damped amplitude term as well with the phase of oscillation term. The slope of the natural-log plot of the temperature amplitude ( $\Delta T$ ) over the sample length (X) as well as the slope of the phase over the sample length is k, whereof the thermal diffusivity can be calculated by applying equation (3).



Figure 1: Schematic of measurement principle of the new test stand  $TIMAwave^{TM}$ 

#### 3 Proof of Concept

First, the measuring principle will be demonstrated in principle by means of transient thermal simulations. In a further step possible parasitic effects are studied and discussed.



Figure 2: Simulation model with boundary conditions and principle result (here thermal wave amplitude).

Figure 2 shows a simple model of a metal strip (copper, 20 mm x 5 mm x 1 mm). One side (left bottom) is maintained at constant temperature and the other top side is impressed with a sinusoidal modulated heat flow. In order to quickly achieve the state of steady oscillation, the temperature distribution of a thermal steady state simulation with a constant heat flow (half power) is used as starting condition.

The results for two different excitation frequencies are shown in Figure 3. A path along the sample surface is plotted over location. As expected from equation (4) we get linear slope of phase (upper graph) and linear slope of natural-log scaled amplitude plot (lower graph). Different slopes arise for different frequencies where higher frequencies result in higher slopes.



Figure 3: Results from simulations. Different linear slopes for different frequencies.

The following Table 1 summarises and compares material data put into the model and extracted by  $TIMAwave^{TM}$  method.

		f [Hz]	Expected values	Calculated values	Deviation
	itude	2	232	270	16%
[1/m]	Ampl	10	520	615	18%
Slope	ase	2	232	236	2%
Ph	10	520	517	1%	
/s]	[s] itude	2		82	30%
y [mm²,	Ampl	10	116	83	29%
ffusivit	Diffusivity	2	116	113	3%
Dil		10		118	2%

Table 1: Overview on simulation results compared to expected diffusivity from the simulation input material data.

The results confirm the expected paths of phase and amplitude. However, there are large deviations (< 30%) in the amplitude slopes and extracted diffusivities. The phase slopes fit very well (<3%). As it will be discussed below, the deviation of the amplitude information is due to an insufficient number of excitation periods. The stationary oscillation has not been reached till then. The phase information is less sensitive on this effect.

Equation (4) is only valid if the sample has reached the state of the static oscillation. As described in [5, p65] there exists a further term allowing the complete description of the problem which is difficult to assess analytically.

$$T(x,t) = A \cdot e^{-k \cdot x} \cos(\omega t - k \cdot x) - \frac{2A}{\sqrt{\pi}} \int_{0}^{\frac{x}{2}\sqrt{\alpha \cdot t}} \cos\left(\omega t - \frac{x^{2}\omega}{4\alpha \cdot u^{2}}\right) \cdot e^{-u} du$$
<sup>(5)</sup>

The second term in equation (5) is a transient disturbance caused by starting the oscillation of surface temperature at time t=0. It vanishes as time increases and leave the first term which is a steady oscillation.

For practical measurements that means to wait sufficiently long before valid results can be extracted from the slopes. The experimental data from a measurement of a copper plate in Figure 4 illustrate this fact. The respective lines for differently long wait actions (100... 3800 periods @1 Hz) were overlaid. This particularly significant occurs for the amplitudes. Offset drift and change of slopes can be observed. Phases may already be evaluated after 100 periods or less.



*Figure 4: Experimental result for different excitation periods. Slopes for phases converge faster than amplitude slopes.* 

To understand this circumstance and other parasitic effects such as losses due to convection and radiation that are expected particularly for low excitation frequencies, simulation studies were carried out and will be continued.

### 4 Design and realization of *TIMAwave*<sup>TM</sup> test stand

For the realization of the *TIMAwave*<sup>TM</sup> test stand the following components are needed:

- Cooler to keep one end of the sample at constant temperature
- Laser diode as modulated heat source focused on the other end of the sample
- Infrared camera to measure the surface temperature of the sample
- Electronics for the lock-in processing and the synchronization between modulated heat source and IR image acquisition

Cooler and IR camera are part of the already existing steady state test stand  $LaTIMA^{TM}$ , which has been developed for thermal conductivity measurement of highly conductive materials [2]. The  $LaTIMA^{TM}$  test stand has been extended by an additional heat source (laser diode) and the required electronics. Thus a combined test stand has been created, which is able to measure thermal diffusivity and thermal conductivity of the same sample. Figure 5 shows the hardware, where both  $LaTIMA^{TM}$  and  $TIMAwave^{TM}$  test stands are integrated. The IR camera is mounted onto three linear guides with stepper motors and can be moved in three axes automatically.



Figure 5: Mechanical hardware including LaTIMA<sup>TM</sup> and TIMAwave<sup>TM</sup> test stands



Figure 6: Left: LaTIMA<sup>TM</sup> test stand, right: TIMAwave<sup>TM</sup> test stand.

#### 5 Characterization results

To verify the functionality of the *TIMAwave*<sup>TM</sup> test stand, the thermal diffusivity of several materials has been measured by using the new test stand.

The thermal diffusivity  $\alpha$  is calculated according to the theory described in section 2 from the slops of the amplitude and phase images. However, all following results were calculated from the phase information. The results of the amplitude showed systematically lower thermal diffusivity and large dependency on the frequency. To clarify this effect further investigations are necessary and in progress (see section 3).

The thermal conductivity  $\lambda$  results from the measured thermal diffusivity  $\alpha$ , the specific heat capacity  $C_P$  and the density  $\rho$ .

$$\lambda = \alpha \cdot C_P \cdot \rho \tag{6}$$

The results of some selected materials will be shown in following sections.

#### 5.1 Characterization of bulk metals

Four bulk metals with well-known thermal properties have been selected to be characterized by the new test stand  $TIMAwave^{TM}$ . The same samples had also been measured by the *LaTIMA*<sup>TM</sup> test stand which is reported in [3].

Table 2 shows the results of thermal diffusivity measured by  $TIMAwave^{TM}$  and the resultant thermal conductivity in comparison to the thermal conductivity of the same samples measured by  $LaTIMA^{TM}$ . The values of specific heat capacity and density have been taken form the literature [6], [7].

Table 2: Thermal diffusivity and conductivity results of $TIMAwave^{TM}$  compared to LaTIMA<sup>TM</sup> results

Material	α (TIMA wave)	Cp (Lit) [J/kg*	ρ (Lit) [kg/	λ (TIMA wave)	λ ( <i>LaTIMA</i> <sup>TM</sup> )
	[mm²/s]	K]	m <sup>3</sup> ]	[W/mK]	[W/mK]
Silver (Ag99.9)	167±3	10490	239	419±15	429±20
Aluminium (Al99.5)	88±8	2702	895	212±21	230±11
Copper (Cu HCP)	105±9	8952	385	363±25	377±20
Brass (CuZn37)	31±2	8400	377	99±8	120±7

The results of thermal conductivity of  $TIMAwave^{TM}$  measurement fit within their error intervals with the results of  $LaTIMA^{TM}$ . However, the thermal conductivity values calculated from  $TIMAwave^{TM}$  measurement are systematically lower than the  $LaTIMA^{TM}$  results. The reason could be due to the uncertain literature values of specific heat capacity and density used for diffusivity calculation.



Figure 7: Thermal diffusivity of bulk metals measured by  $TIMAwave^{TM}$ 



Figure 8: Resulting thermal conductivity of bulk metals measured by TIMAwave<sup>TM</sup>

#### 5.2 Characterization of bulk ceramics

Three bulk ceramics, Al<sub>2</sub>O<sub>3</sub>, AlN and Si<sub>3</sub>N<sub>4</sub> ceramics which are usually used in electronics industry as substrates for circuit boards, have been measured by *TIMAwave*<sup>TM</sup>.

The results of thermal diffusivity and the calculated of the thermal conductivity values fit well with the literature values for these bulk ceramics.

Table 3: Results of thermal diffusivity and conductivity results of different bulk ceramics measured by TIMAwave<sup>TM</sup>

Matarial	α	Cp (Lit)	ρ (Lit)	λ
Material	[mm²/s]	[J/kg*K]	[kg/m³]	[W/mK]
$Al_2O_3$	7.2±0.2	3986 [6]	781 [6]	22.4±0.8
AlN	68.7±1.4	3260 [8]	745 [8]	167±6
Si <sub>3</sub> N <sub>4</sub>	34.4±2.3	3440 [9]	715 [9]	85±7



Figure 9: Thermal diffusivity  $\alpha$  of  $Al_2O_3$ , AlN and  $Si_3N_4$  measured by TIMAwave<sup>TM</sup>



Figure 10: Thermal conductivity  $\lambda$  of  $Al_2O_3$ , AlN and  $Si_3N_4$  measured by TIMAwave<sup>TM</sup>

#### 5.3 Characterization of multi-layer samples

Silicon samples with  $SiO_2$  and  $Si_3N_4$  passivation layers have been characterized by *TIMAwave*<sup>TM</sup> in order to investigate the influence of the passivation layers on the in-plane thermal conductivity. The following samples have been characterized:

Sample 1: Si with 670µm thickness Sample 2: Si plus 1µm SiO<sub>2</sub> layer Sample 3: Si plus 2µm SiO<sub>2</sub> layer Sample 4: Si plus 1µm Si<sub>3</sub>N<sub>4</sub> layer Sample 5: Si plus 2µm Si<sub>3</sub>N<sub>4</sub> layer

Layer 2 (SiO2 or Si3N4)	
Layer 1 (Si)	

Figure 11: Schematic of the tested multi-layer sample

The in-plane thermal diffusivity values show no measurable deviations between the bulk silicon sample and the samples with SiO<sub>2</sub> and Si<sub>3</sub>N<sub>4</sub> passivation. The measured thermal diffusivity value of  $85\pm1$  mm<sup>2</sup>/s fits with the expected value for silicon.

The thermal conductivity values have been calculated according to equation (6). However, the density  $\rho$  and the specific heat capacity  $C_P$  have been calculated for each sample according to following equations:

$$\rho = \frac{\rho_1 \cdot d_1 + \rho_2 \cdot d_2}{d} \tag{6}$$

and

$$C_{P} = \frac{C_{P_{1}} \cdot d_{1} \cdot \rho_{1} + C_{P_{2}} \cdot d_{2} \cdot \rho_{2}}{\rho \cdot d}$$
(7)

#### Where:

- $C_P$ : specific heat capacity of the whole sample
- *C*<sub>P1</sub>: specific heat capacity of layer 1
- $C_{P2}$ : specific heat capacity of layer 2
- *ρ*: density of the whole sample
- $\rho_1$ : density of layer 1
- $\rho_2$ : density of layer 2
- *d:* thickness of whole sample  $= d_1 + d_2$
- d<sub>1</sub>: thickness of layer 1
- d<sub>2</sub>: thickness of layer 2

For the calculation of the density and specific heat capacity the following literature values have been used:

Table 4: Literature values of density and specific heat capacity for Si, SiO<sub>2</sub> and Si<sub>3</sub>N<sub>4</sub>

Material	ρ [kg/m³]	Cp [J/kg*K]
Si	2329 [10]	732 [10]
SiO <sub>2</sub>	2650 [11]	744 [11]
Si <sub>3</sub> N <sub>4</sub>	3440 [9]	715 [9]

The resulting density and specific heat capacity for the samples are listed in the following table:

Table 5: Calculated values of density and specific heat capacity for Si, SiO<sub>2</sub> and Si<sub>3</sub>N<sub>4</sub>

	ρ [kg/m³]	Cp [J/kg*K]
Sample 1	2329,0	732,00
Sample 2	2329,5	732,02
Sample 3	2329,5	732,04
Sample 4	2330,5	731,97
Sample 5	2332,3	731,93

It can be seen, that the resulting density and heat capacity for the multi-layer samples are very close to the values of silicon, due to the relatively thin thickness of the passivation layers compared to the thickness of the silicon layer.

From the measured thermal diffusivity and the calculated density and specific heat capacity, the in-plane thermal conductivities of the samples have been calculated (Figure 13).



Figure 12: Thermal diffusivity Si, Si with SiO<sub>2</sub> and Si with  $Si_3N_4$  passivation layers measured by TIMAwave<sup>TM</sup>



Figure 13: Thermal conductivity of Si, Si with SiO<sub>2</sub> and Si with  $Si_3N_4$  passivation layers measured by TIMAwave<sup>TM</sup>

#### 6 Summery and Outlook

In this paper an innovative test stand for the measurement of thermal diffusivity based on Angström's method has been presented. By means of FE simulation and simple experiments the concept and the method have been proven. It has been shown by combined simulation and experiment, that results calculated from the amplitude images of the lock-in processing show high uncertainty, while the results of the phase images are very reliable and reproducible. The investigation of this effect is in progress and will be reported in a future publication.

The test stand has been designed, realized and integrated into the already existing test stand  $LaTIMA^{TM}$ . Through the combination of the two test stands in one device, it becomes possible to measure the diffusivity and conductivity of the same sample and to calculate the specific heat capacity or the density.

Several materials were measured by the new test stand. To demonstrate the functionality and accuracy of the test stand, samples with well-known thermal properties have been characterized which is reported in this paper. Further investigations of advanced samples and materials from multilayer to thin films are in progress.

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## Temperature Characterization of Small-Scale SOI MOSFETs in the Extended Range (to 300°C)

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#### Abstract

In this work, results of electrical measurements and their analysis are demonstrated for a small-scale 180-nm SOI CMOS technology in the extended temperature range (up to  $300^{\circ}$ C). Comparison with high temperature electrical characteristics of 0.5 µm technology is drawn. Modified model for SOI MOSFETs, based on BSIMSOI model is developed and model parameters are extracted for SPICE simulation of IC blocks. Results of subsequent SPICE simulation of analog and digital circuit blocks characteristics are presented. The potential feasibility of using small-scale SOI CMOS technology (180-nm) for extended temperature range integrated circuits (ICs) is demonstrated.

Keywords: SOI MOSFETs, high temperature electronics, integrated circuits, circuit simulation, electrical characteristics measurement, SPICE models

#### 1 Introduction

Currently one can distinguish several fields of application of electronic units capable of operating reliably in the high temperature range: motor, aircraft and space vehicles, deep hole drilling (see e. g. [1]–[4]). For designing of extendedtemperature integrated circuits (with maximum operational temperature up to 300°C) for various applications, bulk Silicon complementary metal-oxide-semiconductor (CMOS) technologies are not suitable as they feature high values of leakage currents and leakage rise rates with temperature. At the same time, CMOS technologies on insulator (SOI CMOS) are already utilized in production of ICs for high temperature electronics (up to 225°C) as they provide substantially lower values of leakage current at high temperature [4]. In the recent years several works were published (e.g. [5]-[8]), where SOI MOSFET characteristics measurement results in the extended temperature range were presented. In [5] n- and p-channel SOI MOSFETs with 1 µm feature size and in [6] with 0.35 µm feature size in the range up to 450°C are investigated. In [7] measurement results for threshold voltage, drain and gate leakage currents for an nchannel SOI MOSFET with  $W/L = 10/0.12 \mu m$  and with T up to 300°C are shown. In [8] IV-curves for n- and p-SOI MOSFET with  $L = 3 \,\mu\text{m}$  and with T up to 250°C are demonstrated, and for device with  $L = 1 \mu m$  and with T up to 300°C threshold voltage, leakage current shifts, and specific leakage current for various length devices are shown. In most publications, however, minimum feature size  $(0.35 \,\mu\text{m})$  is noticeably larger than those in the advanced digital technologies (< 200 nm), which does not

allow for utilization of small-scale devices benefits in high temperature IC design.

The aim of this work was to study the potential feasibility of using small-scale 180-nm SOI CMOS technology in the extended temperature range (up to 300°C). Shown are the measurement results for SOI MOSFETs with various size placed within a test chip fabricated with the developed technology; dependencies of transistor model parameters on temperature are identified, correlation with transistor width and length is also addressed. A compact model based on the standard BSIMSOI model for circuit simulation is presented; its temperature coefficients are identified. Several standard analog and digital circuit blocks are simulated and their characteristics degradation with temperature is quantified.

#### 2 SOI MOSFET Test Structures Measurement Procedure

For high temperature applications, necessary modifications have been introduced into the technology process concerning traces and vias materials, gate dielectric etc. The test chip included a large number of SOI MOSFETs of various size and structure: n- and p-channel A-type (with the active layer connected to the source) and H-type (with a terminal to the active layer) fabricated with two technologies (for comparison), modified for hightemperature applications. The *first* technology featured 0.5 µm design rules, 3.5 V supply voltage, gate length in the range  $0.5 \div 5$  µm, width in the range  $0.7 \div 10$  µm, active layer thickness  $t_{Si} = 190$  nm, gate oxide thickness  $t_{ox} =$ 11 nm. The *second* technology featured 0.18 µm design rules, 1.8 and 5.0 V supply voltage, gate length in the range  $0.18 \div 10 \,\mu\text{m}$ , width in the range  $0.7 \div 10 \,\mu\text{m}$ ,  $t_{Si} = 90 \,\text{nm}$ , gate oxide thickness  $t_{ox} = 3 \,\text{nm}$ .

Experimental part of the SOI MOSFET investigation comprised measurement of the standard set of electrical characteristics (transfer and output curves with and without voltage bias at the body terminal, parasitic bipolar transistor curves) on a set of selected transistors from the whole number of test chip devices (*large, short, narrow, small*, and several others to identify width- and length-dependent effects). Gate width and length values of the *large, short, narrow, small* transistors from both technologies are summarized in Table 1.

The actual set of test devices and their curves to be measured was defined according to the requirements of the IC-CAP [9] SPICE model parameters extraction system.

Table 1	. Test	transistor	gate	dimensions
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Transistor function	Technology no. 1 with $L_{\min} = 0.5 \ \mu m$		Technology no. 2 with $L_{\min} = 0.18 \ \mu m$	
	W, µm	L, µm	W, µm	L, µm
large	10	5	10	10
short	10	0.5	10	0.18
narrow	0.7	5	0.7	10
small	0.7	0.5	0.7	0.18

Heating of SOI MOSFETs and simultaneous electrical curves measurement was done on-wafer with a probe station and a thermal chuck. Measurements were automated with a software-hardware system based on a 2-channel source-measurement unit Keithley 2602 and a separate voltage source and a multimeter, operating under the control of LabView software [10].

#### 3 Results of SOI MOSFET Characteristics Measurement

Figure 1 presents an example of measured subthreshold transfer IV-curves for the *short* n- and p-channel SOI MOSFETs of the two technologies at drain bias 0.05 V at different values of temperature from 27 to 300°C. Figure 2 shows parameters shift with temperature for the *large*, *short*, *narrow*, and *small* transistors: absolute shift of threshold voltage, relative shift of mobility for both technologies.

These results allow drawing several conclusions with respect to temperature-induced MOSFET parameters changes:

1) Threshold voltage reduction of transistors with 0.18  $\mu$ m design rules is lower upon the average by 20% than that of the 0.5  $\mu$ m design rules transistors, while differences among various size devices are not larger than 25%.

2) Carrier mobility reduction is lower by 10%, while a) short-channel devices (with  $L = 0.5 \mu m$  and  $L = 0.18 \mu m$ , respectively) demonstrate a lower reduction than longchannel ones (with  $L = 10 \mu m$ ) (by 30 and 15% respectively, b) length dependence of mobility reduction is substantially stronger than width dependence.

3) Subthreshold slope enlarges by 100 mV/dec with temperature rise from 27 to 300°C; differences between transistors of various size are within statistical error.

4) Off-state leakage current at  $V_{GS} = 0$  V for the *short* transistor increases to 10–20 nA from 27 to 300°C for the technology no. 1, while the current at  $V_{GS} = -1$  V increases to 200–300 pA. Corresponding factors for the technology no. 2 per the same W/L ratio is however 2.5 times higher.

The measurement results confirmed that changes of characteristics and parameters of small-size (0.18  $\mu$ m) SOI MOSFETs at 300°C are not critical and that so small SOI MOSFETS can be used for high temperature IC s.

#### 4 SOI MOSFET Modeling for High Temperature Applications

A modified compact SPICE model based on the standard BSIMSOI [12] model for SOI MOSFETs was developed in this work for circuit simulation with account for high temperature in the extended range (up to 300°C). The initial BSIMSOI model does comprise thermal equations, but they are valid only up to 150°C, and substantial error reveals itself in the extended temperature range.

As an illustration of this fact, Figure 3 presents comparison between experimental data ([13] for SOI MOSFETs with gate length  $L = 1 \mu m$ ) and BSIMSOI threshold voltage equation evaluation in the extended temperature range. The built-in temperature dependency is merely a linear function, which results in 25–30% error in threshold voltage calculation in the extended temperature range (solid line in Figure 3). At the same time, extrapolating the curve defined in the range up to 150°C has a disastrous impact on calculation accuracy in the extended temperature range (dashed line in Figure 3).

The developed model uses an extended set of temperaturedependent parameters and comprises a refined set of thermal equations. For a SOI MOSFET those parameters are threshold voltage-related (VTH0, K1, K2 etc.), carrier mobility-related (U0, UA, UB etc.), p-n-junction leakage currents (JDIFS, NDIODES etc.), saturation voltage (VSAT), serial resistance (RDSW), channel overlap length (XL) impact ionization current (ALPHA0, BETA0 etc.), subthreshold slope (VOFF, NFACTOR) and others. Several parameters of the initial model use the built-in dependencies on temperature, while new or refined dependencies were introduced for a number of parameters.



Figure 1. Measured subthreshold  $I_D$ -V<sub>GS</sub> curves of the "short" n- and p-channel SOI MOSFETs with  $W/L = 10/0.5 \,\mu m$  (technology no. 1, a), and with  $W/L = 10/0.18 \,\mu m$  (technology no. 2, b) at 0.05 V drain bias at various values of temperature



Figure 3. Degradation of SOI MOSFET threshold voltage in the extended temperature range: symbols—experiment [13], solid/dashed line—approximation in the range up to 400°C/150°C

Temperature changes produce model parameter shifts according to the polynomial expression (valid for all parameters except mobility):

$$a_0 + a_1 \Delta T + a_2 (\Delta T)^2 + \dots$$
 (1)

Temperature dependence of mobility is expressed with a hyperbolic function:

$$UO(T) / UO(0) = b_0 \, (\Delta T)^{bl}.$$
 (2)

Figure 2. Measured n-channel SOI MOSFET parameters shift versus temperature in the range from 27 to 300°C: absolute shift of threshold voltage (a, c), relative reduction of mobility (b, d) for the "large", "short", "narrow", and "small" transistors fabricated with technology no. 1 (a, b) and no. 2 (c, d)

In both expressions (1) and (2)  $\Delta T$ —temperature change with reference to the normal value,  $a_0$ ,  $a_1$ , etc.—fitting coefficients.

For the developed technology, SPICE model parameters were identified for the purpose of subsequent circuit simulation. SOI MOSFET IV-curves simulation error is within 20% for the whole set of transistor dimensions and values of temperature. Figure 4 presents measured and simulated SOI MOSFET IV-curves for both technologies at 27°C and 300°C.

#### 5 SOI MOSFET Circuit Simulation with Account for High Temperature Ambient

The aim of this step was to estimate the capabilities of IC blocks fabricated with the SOI CMOS technology under test, having small-scale design rules (180-nm), in the extended temperature range (up to 300 C).

In the furtherance of this goal, a number of analog and digital circuit blocks were simulated with account for high ambient temperature effects using the model parameters extracted at the previous stage, and the given blocks resistance to temperature was estimated. Simulation was done with HSpice vA-2008 in the "standard accurate" mode.


Figure 4. Comparison of measured and simulated transfer (a, b, e, f) and output (c, d, g, h) characteristics of a "short" SOI MOSFET with  $W/L = 10/0.5 \mu m$  (technology no. 1, a–d), and with  $W/L = 10/0.18 \mu m$  (technology no. 2, e–h) at 27 C (a, c, e, g) and 300 C (b, d, f, h)



Figure 5. Simulated electrical characteristics of a SOI CMOS full adder circuit (28 MOSFETs) at f = 500 MHz in the temperature range 27 C÷300 C: a) summands A and B, input carry digital signal waveforms, b) sum signal, c) output carry signal

As a first example, Figure 5 presents simulated electrical characteristics of a SOI CMOS full adder circuit (28 MOSFETs) at f = 500 MHz in the temperature range 27 C÷300 C. Simulation results indicate only mild timing parameters derating, but no functional failure.

As a second example, Figure 6 presents simulated electrical characteristics of a SOI CMOS operational amplifier circuit (38 MOSFETs) in the temperature range 27 C $\div$ 300 C. Simulation results confirm that even at 300 C opamp internal voltage gain does not decrease more than twofold, which is a good figure.

#### 6 Conclusion

1. Analysis of small-scaled SOI MOSFET experimental IVcurves and parameters measured in the extended temperature range (up to 300 C) allowed obtaining particulars of transistor behaviour and their constraints in this ambient.

2. It was demonstrated that  $0.18 \,\mu\text{m}$  SOI MOSFETs as compared to their  $0.5 \,\mu\text{m}$  predecessors, in addition to a higher packaging density, provided for several advantages with respect to circuit engineering: lower shift of threshold voltage and lower reduction of transconductance, presenting only slightly higher values of leakage current.



Figure 6. Simulated electrical characteristics of a SOI CMOS operational amplifier circuit (38 MOSFETs) in the temperature range 27 C÷300 C: a) frequency response, b) transient response at f = 1 kHz and Vin = 10  $\mu$ V, c) transient response at f = 1 MHz and Vin = 5 mV

3. In order to make SOI CMOS circuits simulation in the extended temperature range possible, a compact SPICE macromodel was developed for SOI MOSFETs based on the standard BSIMSOI model with a refined set of thermal equations. Thermal coefficients of the proposed model were extracted for test transistors, which allows for SPICE simulation in the extended temperature range up to 300 C; simulation error of SOI MOSFET IV-curves is within 20%.

4. Results of analog and digital IC blocks simulation confirmed their operating capability in the extended temperature range.

Thus, it was endorsed that the small-scale 180 nm SOI CMOS fabrication technology was feasible for design of extended temperature range (up to 300 C) integrated circuits.

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## **Investigation of Heat Transfer Coefficient Variation in Air Cooled Hybrid Electronic Circuits**

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#### Abstract

This paper discusses the problem of heat transfer coefficient variation in air cooled hybrid circuits. The investigations are based on a practical example of a circuit containing a bipolar transistor heat source. Its temperature is measured using the base-emitter junction. Additionally, infrared measurements of circuit surface temperature are taken. The measurements are carried out in a wind tunnel for different values of dissipated power and with variable cooling air speed. The measurement results are analysed allowing the assessment of heat transfer coefficient variation with surface temperature and cooling air velocity. Based on the analyses, compact thermal models are generated for the circuit allowing fast and accurate simulation of circuit temperature in various cooling conditions.

#### 1 Introduction

Thermal processes are commonly modelled by the Fourier-Kirchhoff heat equation [1]-[2]. In the case of electronic circuits the linear version of this equation, in which model parameters do not depend on temperature, is usually used. The impact of model linearity on simulation accuracy was previously studied in literature, e.g. [3]-[5], indicating that in most real cases, especially with good cooling conditions, nonlinear effects are negligible, even if in reality material thermal properties vary with temperature.

However, as shown in [6], in the case of air cooled devices boundary conditions might strongly depend on outer surface temperature, hence their variation should be accounted for in thermal analyses. This problem was already investigated by the authors for a discrete device with a heat sink [7]. Here, a hybrid circuit is analysed. Such circuits usually have large surface area and consequently local values of the heat transfer coefficient, modelling heat exchange with ambient at outer surfaces, can differ significantly

The following section of this paper presents the investigated hybrid circuit and the equipment used in experiments as well as the thermal analysis method employed by the authors. Next, thermal behaviour of the circuit is studied both in free convection and forced air cooling conditions. Finally, circuit heating curves are simulated with compact thermal models and compared with measurements.

## 2 Experimental setup

#### 2.1 Benchmark circuit

The investigations presented in this paper concern a hybrid circuit manufactured in the Insulated Metal Substrate (IMS) technology. The 160 mm long and 33 mm wide aluminium substrate has the thickness of just 1 mm and it is insulated by a 100  $\mu$ m resin layer on which all electrical connections are printed in a thin copper foil.



Figure 1: Scale drawing of the hybrid circuit indicating the location of heating device (dimensions in millimeters).

From the experimental applicability point of view, the most important feature of this circuit is that it contains a bipolar power transistor in the DPAK package whose exact location in the circuit layout is shown in Fig. 1. Then, this transistor can be used as a heater and at the same time it might serve as a temperature sensor. Thus, before the measurements the device was calibrated on a cold plate for different emitter current values. The results presented in Fig. 2 indicate that the base-emitter junction voltage decreases linearly with temperature and its sensitivity is reduced from 2.0 mV/K at 100 mA emitter current to 1.5 mV/K at 2 A.



Figure 2: Measured dependence of base-emitter voltage on temperature for different emitter current values.



Figure 3: Photograph of the wind tunnel.

#### 2.2 Measurement equipment

The experiments presented throughout this paper consisted in recording of transistor cooling curves for various values of dissipated power in still air conditions and with different cooling air velocities. For this purpose the T3Ster equipment manufactured by Mentor Graphics was used. The recorded curves were processed further with the software, provided together with the equipment, which implements the Network Identification by Deconvolution method. This allowed for each recorded curve the computation of their respective time constant spectra and cumulative thermal structure functions providing information necessary for the subsequent analyses of thermal phenomena [8].

The measurements with forced air cooling conditions were carried out in the dedicated wind tunnel pictured in Fig. 3. This tunnel has the rectangular cross-section with the side of 40 cm. During the measurements the circuit was firmly fixed horizontally along the tunnel with thermally insulating clamps in the section with transparent walls where the air velocity is known to be laminar. The maximal air velocity in the channel is 4 m/s.

Additionally, for verification purposes in natural convection cooling conditions steady state surface temperature values were measured with the Flir P660 infrared camera allowing real time fusion of visible and infrared light images; hence facilitating the identification of particular devices in images. Before measurements the entire hybrid circuit surface was sprayed with black matt paint so as to assure uniform and well-determined emissivity.



Figure 4: Measured dependence of temperature rise on dissipated power value.

## 3 Natural convection cooling

Initially the temperature measurements were taken in natural convection cooling conditions and the device cooling curves were recorded with the thermal tester for the emitter current values ranging from 100 mA to 2 A whereas the collectoremitter voltage was maintained at 3.5 V. Additionally, steady state temperature distribution images were registered using the infrared camera. The steady state transistor junction and package surface temperature values measured for different values of dissipated power are represented in Fig. 4 with the markers. The measured temperature values were also fitted with the second order polynomials, represented by the lines so as to assess the problem linearity.

Indeed, as can be seen in the figure the surface temperature rise increments are gradually reduced with increasing power resulting in the thermal resistance decrease by some 2 K/W, i.e. almost 15%. Such an important change caused by the improved radiation and convection cooling is not negligible and it should be taken into account in the thermal modelling. On the other hand, the decrease of total junction-to-ambient thermal resistance is not so significant and for higher power values it remains fairly unchanged.

This observation can be explained analysing the cumulative structure functions and the time constant spectra presented in Figs. 5-6 respectively. Namely, these curves diverge not only at their ends corresponding to the heat exchange with ambient, but they differ already close to their origins what indicates that the internal package thermal resistance also varies with temperature. When power dissipation is low this resistance is visibly smaller, but at the same time the cooling resistance is much higher because of poor convection at low surface temperature rise values.

The curves cross each other around the thermal capacitance value of 10 J/K, what roughly corresponds to the calculated capacitance of the thin aluminium plate supporting the entire circuit. Except for that, there are two tiny flat sections in the below the thermal capacitance of 1 mJ/K which possibly can be attributed to the semiconductor and the die attach.

Analysing the time constant spectra, there exist three peaks clearly separated at the time constants of 0.3 ms, 32 ms and 1.4 s. The remaining section of the spectra is affected by the change of cooling conditions because of the variable power dissipation. The thermal resistance values of the first and the third peak virtually do not depend on the power dissipation and on average they are equal to 0.46 K/W and 2.84 K/W. On the contrary, the thermal resistance of the middle peak rises gradually with power dissipation causing the increase of the thermal resistance attributed to these three peaks from 5.66 K/W to 6.21 K/W hence confirming the earlier remark on the increasing internal package thermal resistance.

The thermal resistance corresponding to the remaining parts of the spectra with a maximum around 95 s decreases with increasing power dissipation from 11.00 K/W to 8.91 K/W because of the enhanced radiation and, above all, convection cooling. However, this change is partially counterbalanced by the increase of the internal package resistance.

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Figure 5: Cumulative structure functions with natural convection cooling for different values of dissipated power.

Knowing the exact hybrid circuit surface area, average heat transfer coefficient values could be estimated. The two latter given thermal resistance values yield the respective heat transfer coefficient values of 17 W/( $m^2$ K) and 21 W/( $m^2$ K), which for joint radiation and natural convection heat transfer mechanism are very realistic.

#### 4 Forced convection air cooling

Similar transient measurements were carried out also in the wind tunnel for various air velocities at the emitter current of 1 A. The cumulative thermal structure functions and the time constant spectra computed for the recorded curves are shown in Figs. 7-8 respectively.

This time the cumulative structure functions for various air velocities diverge only at their ends when cooling conditions start to influence the heat transfer processes. The junction-to-ambient thermal resistance decreases from 15.21 K/W for natural convection to 11.02 K/W at the maximal air velocity. The analysis of the time constant spectra demonstrates that the resistance contained up to the minimum located at 1.4 s remains for all the air velocities at the previously mentioned value of 6.21 K/W.



Figure 6: Time constant spectra with natural convection cooling for different values of dissipated power.

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Figure 7: Cumulative structure functions with forced cooling for different air velocities at 1 A emitter current.

Consequently, the entire reduction of the thermal resistance is due to the change of cooling conditions. The estimated value of the heat transfer coefficient at the air speed of 4 m/s is 39 W/(m<sup>2</sup> K). However, the dependence of heat transfer coefficient value on air velocity is not linear since for the speed of 2 m/s the corresponding value is 31 W/(m<sup>2</sup> K).

#### 5 Thermal simulation

The previously presented results of thermal analyses were used to generate for the considered hybrid circuit compact thermal models in the form of RC ladders. As shown in [9], good simulation accuracy for a limited number of RC ladder segments can be achieved by dividing spectra in the location of their minima and computing thermal resistance values for each segment.

Next, the optimal time constants are found bringing in each section of the spectra delimited by the minima the average simulation errors to 0. Then, thermal capacitances are found dividing the time constants by the respective resistances. Such a procedure produces models in the form of RC Foster ladders, which cannot have any physical interpretation, but they can be easily implemented in a computer program.



Figure 8: Time constant spectra with forced cooling for different air velocities at 1 A emitter current.

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*Figure 9: Comparison of measured and simulated transient curves with natural convection cooling.* 

Thus, the spectra from Figs. 6 and 8 were also divided in the locations indicated by the arrows. The simulated transient thermal responses obtained using generated compact models (black lines) are compared with the measurement results (lighter lines) in Figs. 9-10. As can be seen, in spite of their simplicity, the models provide satisfactory accuracy and the maximal error value is always less than 5% of the steady state temperature rise values.

Foster RC ladder element values, as mentioned previously, cannot have any physical interpretation, thus such compact models should be converted into their Cauer counterparts which already have all their thermal capacitances connected to the thermal ground, i.e. ambient, hence their elements can be assigned some physical meaning. For a limited number of RC stages such an operation is numerically stable and can be carried the algorithm suggested in [10].

The conversion results obtained for the considered hybrid circuit with natural convection cooling at 1 A emitter current are presented in Table 1. As can be seen the time constant values range from 134  $\mu$ s to over 80 s. The first three stages of the model can be related to the transistor package and the remaining ones to the heat flow through the aluminium base plate to the ambient. When cooling conditions are changed, it is necessary only to adjust the element values in the last stage. For example, the time constant and the resistance values become 46 s 3.96 K/W for the air velocity of 4 m/s. However, when the dissipated power is varied the element values in the second stage also have to be changed because of varying package thermal properties.

 Table 1: RC Cauer ladder compact thermal model element

 values for natural convection cooling at 1 A emitter current.

Time constant $\tau(s)$	Resistance R <sub>th</sub> (K/W)	Capacitance C <sub>th</sub> (J/K)
1.34E-4	7.06E-1	1.90E-4
2.50E-3	2.77E+0	9.01E-4
3.26E-1	3.14E+0	1.04E-1
3.41E+0	1.67E+0	2.05E+0
8.05E+1	6.93E+0	1.16E+1



Figure 10: Comparison of measured and simulated transient curves with forced air cooling at 1 A emitter current.

#### 6 Conclusions

The experimental results presented in this paper confirmed that the value of the heat transfer coefficient in air cooled electronic circuits might indeed strongly depend on surface temperature what affects the device operating temperature. Therefore, adequate models should be developed allowing accurate thermal simulations of such circuits.

However, the variation of the heat transfer coefficient with temperature might not be the only source of nonlinearities since they might result also from some changes of internal package component thermal properties, which depend on the dissipated power level.

Therefore, thermal analyses should not be based only on the measurements of junction-to-ambient thermal resistance but they should allow also the proper determination of all partial resistances in the heat flow path as well as their temperature dependence.

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**01 Fabrication and Characterization of Microscale Heat Sinks** Gábor Takács, György Bognár, Enikő Bándy, Gábor Rózsás, Péter Gábor Szabó *Budapest University of Technology and Economics, Hungary* 

## 02 Reliability assessment of Wafer Level Chip Scale Package (WLCSP) based on Distance-to-Neutral point (DNP)

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03 Investigation on Solder Voids in Flip-Chip Light-Emitting Diodes Using Thermal Transient Response

Byungjin Ma<sup>1</sup>, Chang Wan Kim<sup>2</sup>, Kun Hyung Lee<sup>3</sup>, Won-Bae Suh<sup>3</sup>, Kwanhun Lee<sup>1</sup> <sup>1</sup>Korea Electronics Technology Institute, Korea, Republic of (South Korea); <sup>2</sup>CTL, Inc.; <sup>3</sup>Shinhan Trade

- **04 Digital Thermal Sensor Based on Ring-Oscillators in Zynq SoC Technology** Charles-Alexis Lefebvre, Leire Rubio, Jose Luis Montero *IK4-Ikerlan*
- **05 Peltiér Cells Cooling System for Switch Mode Power Supply** Giovanni Casano, Stefano Piva *Universita' di Ferrara, Italy*
- **06 Dynamical Phase Transitions on Nanoscale** György Kocsis, Ferenc Márkus Budapest University of Technology and Economics, Hungary

#### 07 Cost-efficient In-situ End-of-life Prognostics of Power Dies and LEDs by Junction Temperature Measurement Sergey Sheva<sup>1</sup>, Raul Mroßko<sup>1</sup>, Jens Heilmann<sup>2</sup>, Bernhard Wunderle<sup>2</sup>, Gusztáv Hantos<sup>3</sup>, Sander Noijen<sup>4</sup>, Jürgen Keller<sup>1</sup> <sup>1</sup>AMIC Angewandte Micro-Messtechnik GmbH, Berlin, Germany; <sup>2</sup>Technical University Chemnitz, Germany; <sup>3</sup>Budapest University of Technology and Economics, Hungary; <sup>4</sup>Philips Applied Technologies, Einhoven, the Netherlands

## 08 Electronic Module for the Thermal Monitoring of a Li-ion Battery Cell through the Electrochemical Impedance Estimation

Marco Ranieri, Diego Alberto, Hélène Piret, Viviane Cattin CEA - Grenoble, France

#### **09 Multi-objective Optimization of Fin Array Heat Sinks** Reijo Karvinen, Kaj Lampio *Tampere University of Technology, Finland*

## 10 Improved Method for Logi-Thermal Simulation with Temperature Dependent Signal Delay

Lázár Jani, András Poppe Budapest University of Technology and Economics, Hungary

#### 11 Modelling of the Thermoelectrical Performance of Devices Based on VO<sub>2</sub> Soma Ur, János Mizsei, László Pohl

Budapest University of Technology and Economics, Hungary

## 12 Influence of the Photoactive Layer Thickness on the Device Parameters and their Temperature Dependence in Thin Crystalline Silicon Photovoltaic Devices

Balázs Plesz, János Mizsei Budapest University of Technology and Economics, Hungary

POSTERS

13 A Study of Electrolytic Capacitors Thermal Conductivity, Behavior and Measurement Zhigang Na

Lenovo, People's Republic of China

- 14 Effect of Flow and Geometry Parameters on Performance of Solar Air Heater Ram Subhash Maurya, Zaid A J Ansari Sardar Patel College of Engineering, India
- 15 Mathematical Modelling of Coupled Heat and Mass Transport into an Electronic Enclosure

Zygimantas Staliulionis<sup>1</sup>, Mirmasoud Jabbari<sup>1</sup>,<sup>2</sup>, Jesper Henri Hattel<sup>1</sup> <sup>1</sup>Technical University of Denmark, Denmark; <sup>2</sup>University of Warwick, United Kingdom

16 Simulation of the Thermal Behavior of a Composite Conductive Adhesive Stéphane Lefèvre, Aylin Yuksel-Gungor, Séverine Gomès

Centre d'Energétique et de Thermique de Lyon, France

- **17 Modelling of Thermal Processes in Heat Flux Sensors** Alexander Kozlov *Omsk State Technical University, Russian Federation*
- 18 Fabrication, Performance and Reliability of a Thermally Enhanced Wafer Level Fan Out Demonstrator with Integrated Heatsink André Gil Cardoso<sup>1</sup>, Hugo Barros<sup>1</sup>, Gusztav Hantos<sup>2</sup>

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## **Fabrication and Characterization of Microscale Heat Sinks**

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#### Abstract

In the field of thermal management, engineers are well aware of the challenges posed by the increasing level of dissipation. Among the many possible solutions to counter the threat of overheating, one is dealing with the usage of microscale heat exchangers, where the forced air or liquid cooling solution is integrated into the electronic package itself. As the System-on-Package integration is not a straightforward task, many fabrication steps have to be fully developed before a successful chiplevel cooling system is ready to be used. In this paper, as one of these many steps, we present a refined manufacturing technology which gives the possibility to create the microscale heatsink integrated together with the electronic devices. With the refined manufacturing technology several channel patterns can be created easily. Nevertheless, only a simple channel pattern is presented now which is tested with the enhanced thermal characterization method developed for microchannel based cooling structures last year.

## 1 Introduction

As a result of the increasing level of integration on a single chip and the cutting edge packaging technologies (3D packaging, System-on-Package) the thermal management issues of electronic devices are still a hot topic. As the macroscale air-cooling techniques are on the limit of their efficiency, new designs are investigated in order to be able to cope with the increasing heat flux and to keep the semiconductor die temperatures in an acceptable range. One of the proposed solutions of the next generation of cooling systems uses integrated microscale channels formed in the semiconductor substrate by either wet- or physical-etching (e.g.: reactive ion etching) directly [1], [2], [3].

In case of wet etching multiple anisotropic etchants can be employed, including potassium hydroxide (KOH), ethylenediamine-pyrocatechol (EDP) and tetramethylammonium hydroxide (TMAH). The use of TMAH solutions are gaining popularity because of their low toxicity and no alkali metal ion contamination issues. Diluted solutions have a good selectivity, low etching rate of even silicon dioxide masking layers and at the same time high silicon etching rates can be reached also in case of longer processes needed for higher microchannel depths [4].

If these channels are formed in the back side of the die which contains integrated circuits then we can speak of an integrated microscale heat exchanger which may either use gas or fluid as a coolant. The main benefit of the integration of the cooling solutions is the lower thermal resistance between the dissipation area (junction) in the substrate and the ambient which directly involves lower operational temperature [5], [6].

In the first approach these structures were used only for cooling purposes, but in several cases it could be applied also in thermal management solutions (e.g.: homogenization of the temperature distribution along the die surface or between dies in a stacked die structures). This kind of management is essential in some cases, due to the fact that the main source of functional errors in digital integrated circuits is the temperature inhomogeneity, and because the delay of standard digital cells is varied by the temperature change [7], [8], [9]. In case of clock distribution networks (CDN) of modern processors [10], [11] the dynamic clock skew minimization demands temperature changes within the smallest possible range. In case of 3D packaging (e.g.: stacked dies) this problem is even more serious.

In our earlier papers we have presented the development of an enhanced thermal characterization method [12] which is based on thermal transient testing [13] which also forms the basis of a JEDEC standard test method [14]. The method is cross verified with analytical calculations and CFD simulations as well. In addition a simplified semi-analytical model was created and presented in our earlier papers [6], [15] to determine the  $R_{th_{MC}}$  thermal resistance value between the walls of the channel(s) and the fluid (which represents the ambient). It was stated that the resistance depends on the properties of the fluid (viscosity, specific heat, etc.), the channel geometries and the flow type (turbulent, laminar).

In our previous papers we have investigated several samples consist of 48 channels integrated directly into the silicon substrate. As a coolant air was applied. Several characterization measurements were performed, but only laminar flow type could be investigated due to the limits of the mass flow controller. For the presented microscale heat sink, the results of our analytical calculations, thus the model were also compared to the measurement results and the standard deviation was around 5%.

In order to investigate the changes of  $R_{th\_MC}$  in the region of transition and turbulent flow, then the overall cross-sectional area should be decreased. It can be realized by decreasing the number of channel with the similar dimensions used earlier.

In this paper the manufacturing and measurement of the new type of microscale heat exchangers will be presented. Through several experiments and runs, the fabrication of the microchannels became more accurate, which means that newer equipment is being involved as well as more sophisticated methodologies of fabrication. The channel pattern of the new cooling structures is determined by analytical calculations, but its efficiency is still to be compared against our expectations. Accordingly, the new samples have to undergo the characterization steps presented in [5], [12]. After the characterization process, the measurement results were compared with the results of the extended model (valid for laminar and turbulent flow types).

In case of integrated microscale channel heat sinks with trapezoidal cross-sectional shape our measurements proved that changing from laminar to turbulent flow type (when the mass flow rate is increased) happens earlier than suspected (much less than Re=2400 that is considered in case of macroscale channel structures). The created model is in good agreement with t phenomenon and at high flow rates the equations for turbulent flow type achieves smaller deviation from the measurements results than the analytical calculations for laminar flow type.

#### 2 Fabrication

The goal of our experimental work was to manufacture several new microchannel geometries and patterns, and find the most suitable for further characterization purpose (turbulent flow, etc.). All etching experiments were carried out on n-type (100) orientation Cz-Si wafers with bulk resistivity between 5-10  $\Omega$ ·cm. After the standard cleaning procedure, the masking layer growth was performed, followed by patterning of the thermally grown silicon dioxide. The commercially available 25wt.% (percentage by weight) TMAH solution was diluted with deionized(DI) water to 5wt.% and the microchannel etching process was performed at elevated temperature (92°C) in order to reach higher silicon etching rates. Metal ion-free strong oxidizer ammonium peroxydisulfate was added to the etchant every hour in order to increase the etching rate uniformity, stabilize the etching rate over time and eliminate hydrogen bubble formation [4]. The summarized flowchart of the fabrication process and lithographic mask drawing is presented in Figure 1 and Figure 2.



Figure 1: Flowchart of the fabrication process

Using the same etching setup and parameters on additional silicon wafers through-silicon holes with proper positioning above the microchannels were fabricated for air inlet and channel sealing purposes. Using wafer dicing  $15 \text{ mm} \times 15 \text{ mm}$  chips were obtained and wafer bonding was employed in order the gain the final samples suitable for measurement.

## 3 Characterization

As it was mentioned, the characterization method is based on thermal transient testing [13] which forms the basis of a JEDEC standard test method [14]. By using the thermal transient testing followed by structure function analysis [13] the junction to ambient or junction to case thermal resistance can be determined, together with the partial thermal impedance of every single element in the main heat path. When this method was applied to characterize non-integrated microchannel heat sinks [15], [17], a dissipative element was mounted over a heat spreader and the cooler device, while the bottom side of the cooler is interfaced to a cold plate. This way the one dimensional heat flow path could be measured and the thermal parameters of each layer can be determined.



Figure 2: Lithographic mask drawings

In the past years the original measurement setup has undergone several enhancements to decrease the measurement error and the effect of unwanted secondary effects like the stirring of the air at the outlet [5], [6], [12]. The resulting, so called enhanced measurement setup can be seen in Figure 3 and Figure 4. While Figure 4 shows the equipment connected to central structure, Figure 3 presents this measurement structure in more detail by indicating each essential element and disturbance around the sample holder.



*Figure 3:* Schematic of the setup connected to the thermal transient tester [6], [12]

## 4 Results

The characterization is focused on the samples with one transversal channel, which means two (half-length) radial channels with two outlets at the corners and one inlet at the center (Figure 5) thanks to the closing lid bounded over it. As a consequence of the opening, etched in the lid, we were able to measure the dimensions of the microchannel by optical microscopy. By inspecting the masks of the wet etching and the images obtained by the optical inspection an average silicon etching rate of  $1.4 \,\mu$ m/minute was obtained. Obviously, the measurements were carried out on several points of the channels. After that, the roughness of the channel sidewalls was examined. These values and measures are very important to create a valid thermal model of the microscale channels.



Figure 4: Realized structure connected to the thermal transient tester [6], [12]



Figure 5. Etched and diced silicon chips

The results were in concordance with the expectations, smooth sidewalls and silicon cavity bases were obtained, the standard deviation between channel depths was under 1 $\mu$ m with a measured depth value of ~100 $\mu$ m. The horizontal dimensions of the channel can be seen in Figure 6 and Figure 7 where the smoothness of the sidewalls can also be observed.

The heat transfer efficiency was preliminary measured at different flow rates using the aforementioned thermal transient testing method. At lower flow rates the total thermal resistance of the cooler device was much higher than 100 K/W, so the thermal insulation of the measurement setup was critical in order to keep the measurement error in an acceptable range.

In Table 1 and Figure 8 the measured thermal resistances of the microchannel heat sink against the flow rate (standard liters per minute) are presented together with the expected values which come from the model presented in [6].



Figure 6. Microscopic image of the channel - bottom side



Figure 7. Microscopic image of the channel - top side

*Table 1. Thermal resistance of the microchannel heat sink at different flow rates* 

Thermal resistance of the microchannel heat sink [K/W]			
Flow rate [slpm]	Measurement	Model	Difference
0.1	516.1	514.1	0%
0.2	266.5	259.7	-3%
0.3	194.4	179.3	-8%
0.4	132.7	141.6	7%
0.5	114.3	123.9	8%
0.6	91.2	104.7	15%
0.7	83.8	90.8	8%
0.8	72.2	80.3	11%
0.9	65.9	72.1	9%
1	60.5	65.4	8%

Figure 8 clearly shows that the measured results are in good agreement with results of our model. An elevated difference can be observed between 0.6-0.8 slpm, which is due to the model inaccuracy in the transition region.

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Figure 8. Comparison of calculated and measured results

It can be seen in Table 1. that the average deviation is around 6%, and the highest difference between the measurement and calculated results is 15% at 0.6 slpm. Up to 0.6 slpm the type of the fluid flow is laminar, and over 0.8 slpm the flow type is clearly turbulent. Between 0.6...0.8 slpm the high difference between the measured and the model results shows that the fluid flow type is in the transition region (Figure 8). In this region it is hard to determine the proper Nusselt number (and as a consequence the heat transfer coefficient) because there are no exact analytical equations in the literature [18].

#### 5 Conclusions

The fabrication of the new samples raised many questions which were dealt properly. The manufactured microscale heat exchangers are measured by using the previously designed and enhanced measurement setup. The results are compared against the analytical calculations and as expected they are in good agreement with one another. Future developments should focus on the investigation of other samples and the application of different coolants (e.g. distilled water, alcohol).

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## Relibability Assessment of Wafer Level Chip Scale Package (WLCSP) based on Distance-to-Neutral Point (DNP)

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## Abstract

Wafer Level Chip Scale Package (WLCSP) is one of the most compact packages which provide good electrical and thermal performance depending on the reliability of the solder joint interconnections to the printed circuit board (PCB). Due to rapid advancements in integrated circuit (IC) fabrication, lower cost per die is achieved when the die count per wafer is high. With the number of IOs (input/output) per die increase which induces the die size and distance to neutral point also increases. Board-level reliability is always a main concern for WLCSP especially without underfill (UF). A common failure mechanism would be solder joint fatigue due to the coefficient of thermal expansion (CTE) mismatch. This would become worse by increasing the distance-to-neutral point (DNP). To improve the reliability, understanding of DNP limitation is necessary. In this paper, different wafer level package configurations are analysed through thermo-mechanical finite element method (FEM) simulation and validated with the thermal cyclic test.

## 1 Introduction

Wafer level chip scale package (WLCSP) provides smallest form factor and high performance for mobile and handheld electronic application which is widely used in semiconductor industry. The coefficient of thermal expansion mismatch between the materials is the main concern on board level reliability. The characterization life cycle decreases when the I/O count increase which in term of larger distance-to-neutral point (DNP) effect. Optimizing the DNP would be a simple but effective method to improve and enhance WLCSP reliability. This paper, lead-free solder constitutive laws of Anand's viscoplasticity model is utilized in the finite element method (FEM) calculation. The calculated fatigue parameters of lead-free solder joint, SACQ, are presented and used to predict the effect of DNP and die clearance [1, 2].

To have a realistic assessment and modelling setup of WLCSP, the thermal cycle test and thermo-mechanical simulation correlation was carried out to determine the fatigue parameters, A and k. Two-parameter Weibull distribution model is applied to test fatigue failure results. After correlation, the effect of DNP would be studied by modelling various array patterns of solder joints and die size (i.e. square and rectangular shapes) with qualify inputs from correlation. The optimal DNP and scribe line width would be investigated by statistical analysis.



Figure 1: Package outline design of WLCSP.

#### 2 Methodology

Two commercial WLCSP products, 342 WLCSPs (18 ×19 arrays) and 361 WLCSP (19 × 19 arrays), were subjected to thermal cycling measurements. Both WLCSP packages, the ball pitch is 0.35 mm and the solder joint diameter is 210 $\mu$ m for 342 WLCSP without underfill and 250 $\mu$ m for 361 WLCSP with underfill. The two-parameter Weibull distribution is in use to characterize failure distribution. Finite element analysis (FEA) is to confirm the observation of the characterization life cycles at 63.2% with 3 thermal cycles in the range of -40°C to +85°C at 7 min. ramp time and 23 min. dwell time. The corner solder joints would be our concern as it always shows the highest plastic strain and in WLCSP structure design, solder joints play a significant role on reliability.

Volume averaging method was used for plastic work density calculation to minimise the sensitivity of meshing and the correlation of Morrow's energy based model with low cycle fatigue model was proposed by Che and Pang [3].

$$W_{ave} = \frac{\sum_{i} \Delta W_{i} \times V_{i}}{\sum_{i} V_{i}}$$
(1)  
$$\Delta W = W_{ave}^{n} - W_{ave}^{n-1}$$

$$N_{f}(63.2\%) = \left(\frac{A}{\Delta W_{p}}\right)^{k}$$
(2)

 $V_i$  is the volume of i<sup>th</sup> solder element at the thickness of 25µm and  $W_i$  is the inelastic strain density of the i<sup>th</sup> solder element. n is total number of thermal cycling. N<sub>f</sub>(63.2%) is the characteristic life at 63.2% failure.  $\Delta W$  is calculated by FEM to correlate to the measurement and determine a fatigue ductility coefficient (MPa), A, and a fatigue constant,

k, of SACQ solder (92.443Sn4.0Ag0.5Cu8.0Bi0.05Ni0.007Ge) by linear regression. The inelastic strain energy density of the critical solder joint is calculated at the  $2^{nd}$  cycle (i.e. n - 1) and  $3^{rd}$  cycle (i.e. n) due to the balance of computation time and thermal cycling stabilization [2].

## 2.1 Thermal Cycling

The thermal cycling test (TCT) were initiated from the room temperature and used electrical test (resistance measurement) for monitoring resistance by multi-meter . Failure ranges of the solder joint are defined between 782 to 956 cycles for 361 WLCSP and 1323 to 1373 cycles for 342 WLCSP. The main failure mode is solder crack at the corner on UBM or PCB side. The Weibull distribution model of WLCSP characterization life at 63.2% is 1359 cycles and 868 cycles for 342 WLCSPs and 380 WLCSP, respectively.



Figure 2: Board configuration of 361 WLCSP for TCT [7].



Figure 3: Daisy chain pattern of 361 WLCSP for TCT [7].

## 2.2 Correlation

The FE models of 342 WLCSPs and 361 WLCSP were built by using ANSYS Workbench. The initial stress-free temperature is set at room temperature (i.e.  $T_A = 25^{\circ}$ C). The inelastic strain energy density would be used as a fatigue indicator. Higher the inelastic strain energy density, worse on solder joint reliability. Cycle 2 and cycle 3 of inelastic strain energy density would be collected to calculate the volume-average of inelastic strain energy density with 25µm thickness of solder. A typical geometry of FE model is shown in Figure 4.



Figure 4: A FE model of quarter model, 361 WLCSP. The dimension of PCB is double of package size (PCB size = package size  $\times$  2)

For SACQ, Anand's viscoplastic constitutive law applied on the solder joints and the 9 material constants of Anand's viscoplasticity:  $s_0$ , Q/k, A,  $\xi$ , m,  $h_0$ ,  $\hat{S}$ , n and a, are in Table 1.

s <sub>0</sub>	0.405	h <sub>0</sub>	3521.56 MPa
Q/k	13509 K	Ŝ	0.638 MPa
А	2.45E08 1/s	n	0.0056
ξ	0.068	а	1.243
m	0.36		

Table 1: Anand's	viscoplasticity	contants of SACQ.
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The fatigue parameters A and k were determined by linear regressions of the logarithm of life cycle vs. logarithm of volume-averaged inelastic strain energy density based on logarithmic form from Zhao [2]:



Figure 5: BLR simulation result of 361 WLCSP (a) contour plot of inelastic strain energy density of solder joints and (b)  $25\mu$ m thick of critical solder joint at the end of third loading step (85°C).

The results of two FE models and the Weibull Analysis of BLR lifetime are tabulated in Table 2. The largest inelastic strain energy density is identified at the corner, critical solder joint. Figure 5 shows the case of the 361 I/Os WLCSP. The relative error, which is defined as (N<sub>Weibull</sub> – N<sub>f</sub>)/N<sub>Weibull</sub> is below 1 % for both cases. The fatigue constants would be applied on the distance-to-neutral point and scribe line width investigations.

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Package	Weibull Analysis: Cycles at 63.2%	Calculated N <sub>f</sub> (63.2%)
342 WLCSP	868	867
361 WLCSP	1359	1358

Table 2: Correlation of the characteristic lifetime with A = 1.8527E+5 and k = 0.5041.

## **3** Board Level Reliability (BLR)

#### 3.1 Distance-to-Neutral Point (DNP)

Thermal cycling experiment and FEM models were carried out and the fatigue parameters of WLCSPs with SACQ solder joint were defined by Equation (3). Various geometries of WLCSPs with 0.35 mm ball pitch and  $250\mu$ m ball diameter were modeled and applied the fatigue parameters parameters from correlation is applied to investigate the significance of DNP.

Square Package	No. of I/Os	DNP mm	Rect. Package	No. of I/Os	DNP mm
$6 \times 6$	36	1.24	$12 \times 6$	72	2.11
$12 \times 12$	144	2.72	$16 \times 12$	192	3.25
$16 \times 16$	256	3.71	$20 \times 16$	320	4.24
$20 \times 20$	400	4.70	$24 \times 20$	480	5.22
$24 \times 24$	576	5.69			

Table 3: Information of square-shape and rectanuglar-shape packages.

The characterized life cycle results are shown in Figure 6. It is clear that the DNP has significant influence on the life cycle in both square-shape and rectangular-shape packages. By comparing the percentage difference between  $20 \times 20$  and  $24 \times 24$  square-shape packages, it could reach 18.7%.



Figure 6: Effect of DNP without scribe line for square-shape and rectangular-shape packages.

SUMMARY OUTPUT

Regression S	itatistics
Multiple R	0.9851764
R Square	0.970572538
Adjusted R Square	0.960763385
Standard Error	310.3688583
Observations	9
	Coefficients
Intercept	8846.716696
I/Os	15.27507515
DNP -2874.646	

Table 4: Regression analysis result.

In Table 4, R Square shows 0.97 which is a very good fit. 97% of variation in life cycle is explained by the independed variables I/Os and DNP. It shows a strong relationship and influence from I/Os and DNP. Also, the linear regression equation of life cycle involved I/O and DNP could be approximately:

Life cycle=8846.72 + 15.28(I/Os) - 2874.65(DNP)

In other words, for each unit increase in DNP, the life cycle decreases with 2874 cycles. For each unit increase in I/Os, the life cycle increase with 15 cycles. Compared to I/Os, DNP has much more influence on the characterized life cycle.

#### 3.2 Scribe Line Width

During the wafer level manufacutirng process, die singulation would be carried out before pick-and-pakce by scribe-and-break, mechanical saw or laser dicing method [4]. The width of scribe line has to be sufficiently large enough to saw the wafer safely without damaging the integrated circuits. Shrinking the die size by reducing the scribe line width could maximizing cost reduction but tighter the control on defect size [5]. Following section would present the influence of scribe width to the board level reliability (BLR) on WLCSP.



Figure 7: Effect of scribe line width.

An important observation is that the larger the scribe line width, the lower of life cycle. Another observation from Figure 7 is that the irregular scribe line width ( $D2 \neq E2$ ) is up to 5% worse than constant scribe line width (D2 = E2). It shows insignificant influence with constant or irregular scribble line width setup. However, if increasing the constant scribe line width by every 0.15 mm, the characterized life cycles would be reduced about 8%. If increasing the irregular scribe line width from 0.05 mm to 0.25, the characterized life cycle would be reduced 4% to 6%. The scribe width line plays an important role on board level reliability.

## 4 Conclusion

- Thermal cycle test and FE models were used to calibrate and predict the characterized life cycle of solder joints of WLCSP. Two commercial products were used and corresponding FE models were built to deduce the fatigue constants, A and k.
- Various square- and rectangular-shape packages were modeled to investigate the effect of DNP which shows that DNP plays a significant role on board level reliability.
- Another topic about scribe line width, it definitely affect the life cycle while keeping the DNP constant. Larger the scribe line width, lower the characterized life cycle.

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## Investigation on Solder Voids in Flip-Chip Light-Emitting Diodes Using Thermal Transient Response

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## Abstract

In order to reduce the cost of the LED packages and to minimize the thermal budget, the chip-on-board (COB) packages and the chip-scale package (CSP) LEDs, based on flip-chip die bonding process, have been developed. Although the flip-chip die bonding process for the COB and the CSP LEDs is useful to decrease the thermal resistance, a precise process control for minimizing voids in solder joint and an in-line inspection for bonding quality check are needed for reliability. We proposed a simple in-line void inspection method based on the thermal transient response of LED junction temperature. In order to carry out the feasibility test, we made three LED package groups showing different solder void qualities. By measuring voltages at two points in time domain, we could distinguish the LED packages showing a poor solder void quality.

## 1 Introduction

Because of their promising advantages over conventional light sources, light-emitting diodes (LED) have been widely used in many applications such as mobile, display, and lighting. However, the competition among LED companies has been intense due to the excessive supply of the LED products, and a need for cost-reduction has been increased, simultaneously.

It is well known that the lifetime of the LED packages is determined by the optical degradation and that main stress origin of the optical degradation is heat generation from the junction of the semiconductor LED chips in the LED packages [1-6]. Therefore, the thermal management is becoming more and more important in LED industry [7-8].

In order to reduce the cost of the LED packages and to minimize the thermal budget for reliability simultaneously, the chip-on-board (COB) LED packages and the chip-scale package (CSP) LEDs, based on flip-chip die bonding process, have been developed. In contrast with conventional LED packages such as injection-molding lead-frame packages, the COB and the CSP LEDs have less thermal interfaces and thus the quality management of the thermal interfaces is more and more in significance.

The flip-chip die-bonding process for the COB and the CSP LEDs is useful to have lower thermal resistance. However, the precise process control for minimizing voids in the solder joint between the semiconductor LED chip and the board in the COB LEDs or between the semiconductor LED chip and the module in the CSP LEDs is needed for reliability. In addition, another problem is on the in-line inspection in mass production of the LED packages. Although the in-line screening for bonding failure is very in significance, there is

no effective and fast method in the LED industry until now. In this paper, we present a simple and fast inspection method for the solder void check in the LED packages.

## 2 Methodology

Until now, the solder-joint quality of the LED packages has been checked as a sample test in mass production by X-ray and acoustic microscopy. In these method, besides throughput issue, the resolution limit in xy-plane for the solder voids, located between the semiconductor LED chip and the board, and no spatial distinction ability in z-direction have been main obstacles against the in-line all-inspection for the solder voids in the LED packages.

In order to solve these problems and to realize the in-line inspection system for mass production, many research groups have studied intensively using their specified algorithms, based on the thermal transient responses [9-14]. In contrast with a conventional thermal transient method [15], in which time-consuming procedures for k-factor and structure function analysis were essential, their inspection methods were simple and rapid for the solder joint analysis between the LED package and the MCPCB.

In principle, we followed the previous inspection methods but we focused on the first thermal interface between the semiconductor LED chip and substrate by flip-chip process. Indeed, the flip-chip process has become a key process for the high efficient and cost effective LED packages in these days. Over 50 % LED packages for back-light unit in display are direct-attach CSP structure and made by using the flip-chip direct bonding process. On the basis of a precise timeconstant analysis for the reference LED package showing a good solder void quality, we set two points of voltage measurement time (t1 and t2) related to the solder void. The t1 and t2 are the specific measurement points before and after the heat, generated at the pn-junction in LED chip, spreads to the solder position. Of course, although the transient voltage means the temperature transient, we do not need to know the real temperature for in-line inspection system. Therefore, we also do not need for the time-consuming procedures for a kfactor, a continuous voltage measurement, and a structure function analysis.

## 3 Experiment and results

In order to carry out the feasibility test, we made three groups of 3535 COB LED packages according to the solder joint quality as shown in Fig. 1. To make a poor bonding quality on purpose, we controlled the temperature of the flip-chip bonder as shown in Fig. 1(b). Using a high resolution X-ray, we could scan the void images as shown in Fig. 2. The LEDs in A group, as a reference, had less than 10% void and had the strength of ~ 2 kgf in die shear test (DST). The strength of 2 kgf was upper limit of our strength tester (Dage4000). On the other hands, as shown in Fig. 3, B and C groups showed about 50% and 90% voids and strengths of ~ 2 kgf in DST. X-ray was very useful to observe the void at sample test, but it was not adequate for a high-speed all-inspection system.



(b) Temperature profile for flip-chip bonding





(a) A group



(b) B group



(c) C group





Figure 3: Die shear test (DST) results of flip-chip package LEDs

In order to observe the flip-chip solder point, we carried out the manual shear test by adding the strength until the LED chips were broken. Figure 4 shows the residues of the electrodes in the LED chips onto the ceramic substrates. The area of the square black region in the figure 3 was proportional to the bonding quality.



(c) C group

Figure 4: The residues of electrode in the LED chip after manual die shear test as a barometer of the bonding quality

LED sorters have been used to screen out the LED packages showing a poor solder quality at the last step in LED production line. In general, an operation voltage and a reverse leakage current of the LED packages have been used to sort out the poor LED packages. Figure 5 (a) shows the operation voltages of three LED groups. Although B group has ~50% void in solder region, there is no difference in the operation voltage between A group and B group. Several LED packages in C group, showing ~ 90 % void, shows nearly same operation voltages as A and B groups. Optical powers of three LED groups were plotted in Figure 5 (b). In common with the electrical property, the optical property like the optical power cannot distinguish the LED packages showing a poor bonding quality from the good LED packages.

Figure 6 shows the thermal transient responses of three LED groups in cooling mode. A T3ster (Mentor graphics Inc.) had been used to characterize them. Absolute value of the sensing



Figure 5: Electrical and optical properties of three LED groups according to bonding quality



(b) Normalized transient response of sensing voltages

Figure 6: Thermal transient response of three groups of LED packages ( $A \rightarrow$  blue,  $B \rightarrow$  red,  $C \rightarrow$  green)

voltage had no distinction ability for the void quality. However, relative value of the transient sensing voltage in three LED groups, normalized to the voltage at 0.1 ms, shows the dramatic difference in shape. The more solder void increases, the more voltage change increases in the same time region. Since we knew that the thermal specific time for the LED chip and the flip-chip solder joint of our LED packages by thermal time-constant analysis, we could determine the two measurement points (t1 and t2) of 0.1 ms and 0.1s, respectively. Figure. 7 shows the voltage differences (V(t2)-V(t1)), measured at t2 and t1 for A, B, C LED groups. Compared to the value of A group, the LED packages in B and C groups showed the higher voltage differences clearly. Since at least 3 LED packages in a second should be measured in-line inspection system in mass production,  $\sim 0.3$ s will be time reference for this system. We prospect that our algorithm will meet the time requirement for the real application.



Figure 7: Voltages differences between 0.1ms and 0.1s for three LED groups

## 4 Conclusions

As a useful tool for the in-line solder void inspection, we proposed a very simple and fast method based on the thermal transient response. Without a continuous measurement of transient junction temperature, only a two-point voltage measurement in time domain was enough to distinguish the LED packages showing the poor solder qualities from the normal LED packages.

For real application, we need to refine the algorithm by adding a heating procedure and by synchronizing the measurement times using a general-purpose current driver.

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## Digital Thermal Sensor Based on Ring-Oscillators in Zynq SoC Technology

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## Abstract

The impact of the temperature is one of the most critical issues when designing an industrial embedded systems. Plenty of them are centered on a System-on-Chip, composed of a programmable logic similar to a FPGA and a processing system with one or more processors. Ring oscillators are often used to measure physical parameter such as the temperature in a FPGA. Therefore, this paper presents a ring-oscillator-based digital temperature sensor implemented as an AXI-Lite Intellectual Property on a Xilinx Zynq Z-7020 28 nm System-on-Chip. Both the impact of the measurement time and the number of gates are studied with the objective of getting a fast sensor to give the chip a fast thermal protection. The sensor is then calibrated with a thermal chamber. As a conclusion, even though its architecture is somewhat different from past works, the designed sensor was found to be functional for the targeted application.

## 1 Introduction

Programmable System-on-Chips (SoC) are getting more and more used in an industrial context to build powerful and adaptable embedded systems. Xilinx introduced in 2011 the Zynq-7000 SoC, designed in a 28 nm technology and equipped with a Programmable Logic (PL), and a Processing System (PS) which includes a dual-core ARM Cortex-A9. Since the Zynq has become the core of many industrial systems, it has been used in hostile environments and may endure strong temperature conditions and attacks. While the Zynq comes with a built-in sensor to measure the global temperature, a way to monitor the temperature of a precise region (e.g. an area implementing a critical function) is required.

Digital temperature sensors based on ring oscillators have been known for nearly 30 years and implemented in Field Programmable Gate Arrays (FPGAs) for 20 years. The advantages of such a technology have been identified as the ability to place the sensor in custom programmable logic areas and to instantiate as many sensors as required. While past publications [1], [2] have used old FPGAs series such as Virtex 5/6 in 40 nm, no tests led on a Zynq SoC have been published to our knowledge.

In this paper, experiments with ring-oscillator-based sensors are presented on a Zynq Z-7020 with the aim of getting a fast-response sensor in order to protect the chip against a fast increase of the temperature. The main contribution consists in implementing a configurable sensor on a Xilinx Zynq-7000 chip with an unusual architecture and studying its behavior following the configuration.

The rest of this paper is organized as follows. Section 2 presents the state-of-the-art of the digital temperature sensors based on ring-oscillators. The designed sensor and the tests realized are described in section 3. Section 4 exposes the results obtained and the conclusions are given in Section 5.

## 2 Background

According to the number of contributions [1-7], the area of digital thermal sensors for FPGAs using ring-oscillators is a hot topic. The advantage over integrated analog sensor has always been identified as the possibility of reconfiguration. The basic architecture is structured around a ring-oscillator which frequency depends on the temperature as explained in section 3. The other required logic is a counter to measure its frequency and a logic block to control the operations. Unlike [3, 4], in this paper, the frequency of the ring is not directly measured. This architecture was tested, with no success. Instead, the signal was synchronized by the main clock of the system. Similar to [1, 3], the sensor exposed in section 3 was calibrated with a thermal chamber.

The behavior of these sensors observed in the past publications is nearly the same. Nevertheless, a difference is noticed following the power voltage required by the technology. If on older technology like Virtex (powered under 2.5V), a linear relation between the frequency and the temperature is reported [3], this is not the case anymore on newer FPGAs like the Virtex-5 or 6, powered under 1V [1, 5].

Nevertheless, none of the past publications aimed at implementing a digital thermal sensor on a Zynq-7000. The most recent works found on this topic are [4], led on a Altera Cyclone IV and [2] led on a Xilinx Virtex-5. That is why an actualized study on the Zynq-7000 series is proposed in this paper.

## 3 Methodology

The design of the sensor is explained in section 2.a, the study of the influence of design factors is exposed in section 2.b and a calibration is proposed is section 2.c.

#### 3.1 Design

The architecture of the sensor implemented in this paper is given in Fig. 1. A ring oscillator was designed in VHDL by looping an odd number of NOT gates and positioning one gate per LUT (a Zynq slice contains 4 six-input LUTs and 8 Flip-Flops). The frequency of such an oscillator is given by

$$f = \frac{1}{2N\tau} \tag{1}$$

with N, the number of gates and  $\tau$  the propagation delay for a single gate, and depends on the temperature as widely proved in the literature [3, 6] or more theoretically deepen in [7]. The ring can be activated or deactivated thanks to an enable signal to avoid self-heating. To get the oscillator's frequency, the output f<sub>RO</sub> is synchronized by the rising-edge detector and increments the Counter during a fixed delay. This design supposes that "clk" is the sampling clock of the system and thereby respects the Shannon's condition on frequencies:

$$f_{clk} \ge 2f_{RO} \tag{2}$$

Therefore, the sampling system is constrained by the maximum clock speed. A Final State Machine was designed in the Control Unit to manage the measurement process.



Figure 1: Architecture of the sensor used

The sensor was then wrapped into a 32 bits-register-access AXI-Lite Intellectual Property (IP) to make it enable to communicate with the PS once instantiated in the PL. Three registers are used in the presented design. The first one for the outputted value; the second to program the initialization time and to control the sensor; the last to program the capture time. The number of gates in the oscillator can be chosen when instantiating the IP.

## 3.2 Adjustments

Two design factors influence the performance and the precision of this type of sensors: the number of gates in the ring and the measurement time adjusted by the Control Unit. These parameters were made adjustable and configurable and different sensor configurations were tested to observe the effects. The number of gates was implemented as a "generic" type and therefore was configured when instantiating the IP. As for the measurement time, it was configured through a register as explained in Section 3.1.

For the evaluation, each sensor was instantiated on the same location in the PL, and put into a thermal chamber regulated at  $50^{\circ}$ C. The relative standard deviation was used to compare all the tested sensors. This quantity gives the precision of the sensor. The results are presented in Fig. 3.

## 3.3 Calibration method

A ring-oscillator-based sensor depends on multiple physical factors (voltage, device's silicon, place and route in the PL) and therefore needs to be calibrated. For that purpose, the temperature inside the thermal chamber was gradually increased by 5°C every 10 minutes on the interval [30 °C ; 65°C]. For each temperature step, 120 samples were recorded and averaged, and plotted. The temperature was measured by the internal analogue temperature sensor and by a K-thermocouple stuck on the surface of the Zynq. In order to obtain the same conditions for both sensors, the IP was instantiated in the PL, as close as possible to the internal sensor. The placement is exposed in Fig. 2. As the accuracy of the built-in sensor is  $\pm 4^{\circ}$ C, the accuracy of the presented sensor could not have been studied more precisely. During this process, a good thermal repartition in the chip was assumed. The calibration curve and its linear and polynomial approximations are given in Fig. 3.



Figure 2: Placement of the sensor inside the Zynq Z-7020

## 4 Results

All the tests were led on a Zedboard, equipped with a commercial version of the Zynq Z-7020 chip whose temperature range is  $[0^{\circ}C; +85^{\circ}C]$  and powered under 1V. The sensor was clocked at 250 MHz. The communication with the computer to retrieve data was set up with Ethernet and a software was developed for both the computer and the PS part of the Zynq.

As explained in section 2.a, a first test aimed at measuring the ideal number of gates for different measurement times  $T_m$ . Seven sensors from 5 to 45 inverter gates were tested, each one for 4 different  $T_m$  between  $2^{17}$  (557 µs) and  $2^{27}$  (537 ms) clock ticks. Thirty measures, each one separated by 10s, were recorded and the relative standard deviations of each serie were studied. As showed on Fig. 3, a high deviation was observed between 5 and 17 gates, due to the non-respect of the Shannon's sampling condition (2) in this

interval, and then tended to stabilize with at least 23 inverters. Therefore a 23-gate-based oscillator was used for the following experiments. The influence of the measurement time can be noticed too: the faster the sensor, the higher the error. As getting a fast sensor was an objective, the calibration was led with the smallest measurement time (557  $\mu$ s). Moreover, a small measurement period avoids self-heating.



Figure 3: Relative standard deviation against the number of logic gates for different capture times (in clock ticks @250MHz) at 50°C on the surface of the chip

In order to obtain a usable sensor, it was calibrated following the method given in section 2.c. As expected, the output of the counter (representing the frequency) decreased with the temperature. However, the calibration curve showed in Fig. 4 is not linear as others past experiments with higher voltages and different technologies [3]. This result is in line with [6] and is attributed to the low-voltage (1V) of the Zynq 7-7020. A linear approximation is therefore nearly impossible and a second-degree polynomial expression should be used. This polynomial expression was used to obtain the accuracy, following the method described in section 2.c.



Figure 4: Calibration curve of the studied sensor

A maximum error of  $\pm 5^{\circ}$ C of the sensor was calculated by searching the maximum difference between the maximal and the minimal value of the counter for each temperature.

## 5 Conclusion

In this paper, a configurable ring-oscillator-based sensor with an architecture where the ring and the counter are dissociated was proposed and implemented on a Xilinx Zynq Z-7020 SoC. The effect of the number of gates and of the measurement period was studied and a fast sensor was obtained with a measurement time of 557 µs for 23 gates. Neither the non-linear behavior nor the ±5°C error measured prevent a quick measure of the temperature to protect the chip. Therefore, this sensor may be used to protect an area of the Zyng. Finally it used 56 LUTs and 59 Flip-Flops (0.1% of the resources available) and is small enough to create as much instances as required for every area of the Zynq to monitor. Our future work will focus on dissociating the system clock and the sampling clock to obtain lower measurement times. The impact of the voltage will be studied too.

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## Peltier Cells Cooling System for Switch Mode Power Supply

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## Abstract

The results are presented of an experimental investigation in a liquid cooled Switch-Mode Power Supply (SMPS). The target is a quantitative analysis of the performance of a cooling system designed to dissipate the heat generated by the active and passive electronic components of this SMPS, in order to limit its maximum operational temperature. The active components are cooled with a liquid cold-plate. The passive components are cooled with an air flow. The temperature of this airflow is controlled with Peltier cells coupled to the cold-late. Measurements are made of temperature and of electric efficiency of the SMPS. The cooling system is placed in an experimental tool where it is possible to measure and control the cooling liquid flow. A detailed analysis of the thermal behaviour of this cooling system is given. Finally, the practical significance of the problem is discussed.

## 1 Introduction

Nowadays, in power supply electronics when high efficiency, small size and low weight are required, switching regulators are used as replacements for traditional (linear) regulators [1]. A Switch-Mode Power Supply (SMPS) is an electronic unit incorporating a switching regulator to convert electrical power efficiently. Unlike more conventional power supplies, a SMPS minimizes the wasted energy and ideally dissipates no power. This higher efficiency in power conversion is an important advantage of SMPSs, commonly coupled to smaller size and lower weight than a linear supply, due to smaller size and lower weight of the transformer.

High electric efficiency and reduced cooling requirements are thence the main characteristics of SMPSs [2-3]. However, as usual in power electronics, compactness means larger power; for high power the heat release is large again and thus efficient cooling systems are needed. Liquid cooling can then become an interesting solution, also because it allows a significant size reduction of equipments in line with the requirements of electronics design [4].

Actually liquid cooling is obtained with cold-plates, consisting of a plate, usually in aluminium, on which are fixed some electronic components and within which one or more hydraulic circuits are obtained for their cooling with water flowing in forced circulation [5]. While it is easy to collocate the active components on a cold plate, the large passive components of a SMPS, like condensers, transformers and coils, need to be placed on a printed circuit board (PCB). It is difficult with a cold plate to maintain both PCB and passive components at the design temperature, because they are originally developed for air cooling.

In a recent paper we presented [6] the results of a thermal analysis in a liquid cooled SMPS for digital TV power amplifiers. Since this SMPS was characterized by high power and high compactness, thereby making the standard cooling techniques difficult to be used, a new cooling system was developed, using water and air as the cooling media. In particular, the active components (MOSFETs) were cooled with a liquid cold-plate, the passive components (condensers, transformers, coils) with an air flow. The air flow was cooled in a large finned surface, in turn cooled with the cold-plate. Finally, the water was cooled with a low cost external heat exchanger.

Unfortunately, this solution is limited by the ambient air temperature, fixing the lower bound to the temperature distributions. When the ambient air temperature is high it can result the need to distribute the air on the passive components at a lower temperature. To obtain this result a new configuration was developed, where the air flow is still cooled in a large finned surface, the latter being cooled with the cold-plate through a set of Peltier cells. The utilization of Peltier cells in power electronics is not a new; a large review of these applications is given by Zhao and Tan [7]. However, our proposal [8] is outside of the traditional schemes of application of the Peltier cells, because we do not use them to directly cool the power components, but to integrate liquid and air cooling.

In the present paper we present the results of an experimental investigation of the performance offered by this new cooling system specifically designed to dissipate the heat generated by the active and passive electronic components in a SMPS, in order to understand how to limit its maximum operational temperature.

## 2 Experiment

In [6] the experimental set-up is described in full details. For this reason here just a short description of its main characteristics is given. On the opposite, a detailed description of the new test section is reported.

## 2.1 Experimental set-up

The experimental set-up consists of a hydraulic testing

circuit where we can insert a test section, in this case the cold plate holding the SMPS to be tested. The operating conditions of the SMPS were simulated with a dummy load connected to the output. To identify the components thermally stressed, twenty-five thermocouples were placed in the most significant points of the apparatus. To qualify the performance, both the thermal power exchanged with the cooling water and the electric power dissipated in the dummy load, consumed from the electricity network and absorbed by the thermoelectric modules, were measured. The data acquisition of temperature, flow rate and electrical parameters was carried out with a multimeter Agilent HP34970A. This multimeter was connected to a notebook by means of a GPIB-USB interface. The data acquisition was carried out by means of a software developed in Labview environment.

#### 2.2 Test section

The SMPS (3 kW,  $+25 \div 50$  V) accommodates a mix of surface mount and traditional technology components to reduce the space occupied as far as possible. The SMPS is protected in temperature and current. It was originally designed for air cooling. Nevertheless, just a limited number of modifications was necessary to place the SMPS on a cold-plate. The modifications were particularly simple, because the active components (MOSFETs) were originally placed on the finned vertical sides of the SMPS. We dismounted the fins and placed the MOSFETs in direct connection with the cold-plate. A top view of the cold plate with its PCB is shown in Figure 1.

The cold plate is used as the base of a closed enclosure where a flow of air is maintained by a pair of fans. Sides and cover of the enclosure are in transparent polycarbonate. The forced flow is used to cool by forced convection the passive components placed on the PCB. They are characterized by a significant volume occupation and cannot be directly cooled on the cold plate. Among the passive components, the ones that mostly contribute to heat release are: a transformer, three coils and two large electrolytic capacitors.

The cold plate (of "press-fit" type) is the same used in [6], consisting in an aluminium plate (thickness 10 mm) where a cooling circuits is manufactured with a copper pipe (external diameter 6 mm) pressed in a channel machined on the surface of the plate. The pipe runs longitudinally along the sides of the plate. Inlet and outlet are on the same side

(Figure 1). On the opposite side, the pipe is bent to form a coil (Figure 2). Over the coil an aluminium finned heat sink is placed (base  $151 \times 157$  mm). The fins (31) are 30 mm high, 135 mm long, 1 mm thick and are separated by a 3 mm throat.

Between the finned heat sink and the cold-plate 12 Peltier cells are inserted to cool the flow of air. The cells were chosen with a rectangular shape (50 x 25 mm), so as to follow the development of the pipe and overlay as much as possible the pipe itself, with a limited protrusion over the plate, as shown in Figure 2. A thin thermal interface is placed between Peltier cells, heat sink and cold plate. The main characteristics of the commercial Bismuth Telluride-based Peltier cells (Kryotherm TB-195-1.0-0.8) are: I<sub>max</sub> = 5.8 A, V<sub>max</sub> = 24.1 V, Q<sub>max</sub> = 86 W. In the thermoelectric cooler (TEC) the Peltier cells are carranged in four groups of three in series; the four chains are then in parallel. The current in each cell is thence one forth of the total.

In front of the finned heat sink two fans (external sides  $50 \times 50$  mm) collect the warm air from the passive components of the PCB and push it into the finned cooling surface.

Compared to the version described in [6], besides the use of Peltier cells, some further changes have been made.The PCB was rotated of 180° for reasons of electrical layout. Furthermore, to better ventilate the thermally stressed components, the perforated wall directing the airflow on the PCB was modified by reducing the number of holes, now concentrated into a smaller area (Figure 1). For these reasons a direct comparison of the temperature data shown here with those reported in [6] is not possible.

The passive components (capacitors, inductances and electric transformers) were instrumented with "T type" thermocouples, in order to evaluate the maximum temperature in the SMPS. Two armoured "T type" thermocouples were placed upstream and downstream of the finned heat sink to measure the temperature of the internal air flow. Two armoured "T type" thermocouples were placed upstream and downstream of the cold plate to calculate, together with the complementary data gathered with an ultrasonic flowmeter, the total heat released by the SMPS

The values of electric power absorbed by the SMPS, by the Peltier cells and dissipated in the dummy load were measured in order to evaluate the efficiency of the SMPS and the EER of the thermoelectric cooler.



Figure 1: Top view of the cold plate with the PCB and the cooling system.

on Thermal Investigations of ICs and Systems ]]





Figure 2: Top view of the Peltier cells distributions on the cooling system of the cold plate.

The efficiency is calculated as the ratio of the useful power output to the power absorbed from the electric grid. EER is calculated as the ratio of the cooling power to the power absorbed by the Peltier cells.

Since on the cold plate insist both the thermoelectric cooling system and the active components, a set of preliminary measurements was performed to evaluate separately the cooling power of the MOSFETs and that exchanged with air in the finned heat sink.

#### 3 Results

The cooling system has been tested for different working conditions which are consistent with the manufacturer's operational conditions. The investigation was directed to obtain useful information on the temperature distribution in the thermally stressed components of the device and to establish the optimum working conditions of the cooling system.

In the whole set of tests the voltage of the SMPS is maintained regulated at 45 V, corresponding to its design condition. The experiment were executed in the late spring, in a room with a quite constant ambient temperature.

In Figure 3 the distributions are shown of efficiency of the SMPS and EER of the thermoelectric cooler for three data sets characterized by different values of the power absorbed in the grid by the SMPS. The data are shown as a function of the current absorbed by the TEC. These distributions can be well interpolated by power functions. EER decreases for increasing values of current, and thence of the power absorbed by the Peltier cells. Also efficiency decreases for increasing values of current. Both parameters show lower values for lower values of power absorbed by the SMPS.

This parameters are not particularly decisive in the design of the cooling system because if it is trivial that high efficiency and high EER are desired, it is also evident that these para-

Figure 3: Efficiency of the SMPS and EER of the cooling system.

meters seem to be at the best when the cooling system is off. For this reason further parameters need to be analyzed in order to individuate the best performances of the system.

In Figure 4 the distributions are shown of the maximum temperature on the passive components (in this SMPS this is the temperature on the surface of the transformer) for three data sets characterized by different values of the power absorbed in the grid by the SMPS. The data are shown as a function of the current absorbed by the Peltier cells. These distributions can be well interpolated by second order polynomials. Higher values of temperature on the transformer are reached for low and high currents for the Peltier cells. A minimum of temperature is well evident for a current of 6.0 - 6.5 A, depending on the power. This minimum of the maximum temperature is a good candidate for the optimum design condition of the TEC.



Figure 4: Maximum temperature in the passive components and temperature difference between water and internal air.

In Figure 4 the distributions are also shown of the temperature difference between the water in the inlet of the cold plate and the air leaving the finned heat sink. These distributions are useful to characterize the cooling effect of the TEC. Also these distributions can be well interpolated by second order polynomials. A maximum of  $\Delta T$  is well evident for a current of 9.0 – 9.5 A, depending on the power.

The different points of optimum of the two temperature distributions shown in Figure 4 are due to the power absorbed by the Peltier cells and discharged in the cold plate. While the cooling power needed by the SMPS is constant for constant power conditions, the power absorbed by the TEC increases in order to obtain higher  $\Delta T$ .

The maximum cooling effect on the airflow occurs for values of efficiency and EER lower than in the case of minimum of the maximum temperature. For this reason the TEC current able to assure the minimum of the maximum temperature can be chosen as the proper design condition. This values of TEC current can also be slightly reduced so as to obtain higher values of efficiency and EER with acceptable values of maximum temperature.

## 4 Concluding Remarks

Electronic equipment are often placed inside enclosures to protect them from environmental influences such as temperature, moisture and contaminants. Contrary to what, in our proposal an enclosure becomes the way to cool those electronic components difficult to be cooled with a cold plate, like electrolytic capacitors and magnetic components. A detailed analysis of the thermal behaviour of a cooling system specifically designed is given and the practical significance of the problem is discussed. The efficacy of the cooling system is demonstrated; the trends of efficiency and temperature are evidenced. A strong dependency of the thermal power dissipated by the SMPS on the electric operating conditions is clearly evident.

Based on these data it is possible to suggest some lines of development of this cooling system.

The utilization of a TEC can be a proper solution if the ambient air temperature is high, because it is able to create an environment at a proper temperature. However, for a complete exploitation of the TEC an accurate design of the system on the base of the parameters affecting its performance is required. Differently, the risk to dissipate power without a corresponding cooling effect exists.

Furthermore, as already suggested in [6], the internal air circulation can be modified to obtain a more efficient flow on the critical components. This can be obtained with

different fans and/or with a different distribution of air over the passive components. Due to the limited available spaces, the system "fans and fins" is not particularly efficient. This system can be redesigned for a better distribution of air between the fins.

## Acknowledgements

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#### **Dynamical Phase Transitions on Nanoscale**

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#### Abstract

On nanoscale, many transport characteristics of the matter differ from the macroscopic ones as quantum effects play role in the propagation of charge and heat carriers. Extensive research had been conducted to reveal the distinct transport behaviour for charge carriers, however, novel investigations have shown that heat carriers (i.e. phonons) are also subject to new transport phenomena. In the study, we estimated possible propagation modes for the dual phase lag model proposed by Anderson and Tamma with additional boundary effects on propagation of heat carriers in a nanoscale silicon layer. Furthermore, if the heat conductivity coefficient's dependence of size (via Knudsen-number) is taken into consideration then the A-T model predicts new ballistic transport mode along the well-known diffusive behaviour. We were able to confirm the existence of new transport modes for heat carriers in nanoscale systems theoretically. The results are not only important from a physical perspective but can be a ground for several technical developments where heating and cooling of the material is crucial (e.g. microprocessors).

#### 1 Introduction

Generally, in classical macroscopic media, the heat transport is modeled by Fourier's law. Combining the constitutive equation with the balance equation results the well-known heat equation:

$$\frac{\partial T}{\partial t} - \frac{K}{c\rho} \frac{\partial^2 T}{\partial x^2} = 0 \tag{1}$$

Despite the simplicity of the model, it has an inherent inconsistency: propagation of action is infinite within the medium. The discrepancy of the model has been pointed out by Maxwell. Later, Cattaneo and Vernotte proposed (similarly to Maxwell) an additional - thermal inertial - term to the heat equation. The additional part resolves the contradiction; however the equation is not aligned with the 2<sup>nd</sup> law of thermodynamics [1]. Various authors proposed extensions to the MCV model [2], [3] to deal with the inconsistency. This paper provides analysis on the model proposed by Anderson and Tamma which incorporates thermal inertia as well as size-effects on the heat carriers with the dual-phase lag term:

$$j_{E} + \tau \frac{\partial j_{E}}{\partial t} = -K \left[ \frac{\partial T}{\partial x} + \tau_{b} \frac{K_{F}}{K} \frac{\partial}{\partial t} \left( \frac{\partial T}{\partial x} \right) \right]$$
(2)

In Eq. 2, the second term  $\tau$  refers to thermal inertia and  $\tau_b$  to the temperature relaxation on the boundaries.

#### 1.1 Mathematical background

The governing equations of the model (along with Eq. (2)) are balance equation

$$\frac{\partial \rho_E}{\partial t} + \nabla j_E = 0, \tag{3}$$

and boundary condition equation proposed by Alvarez and Jou [4]

$$\tau_b \frac{\partial T}{\partial t} + T = T_h - j_E R, \qquad (4)$$

which is based on phonon reflection and scattering on the boundary layer (see Table 1 for detailed description of the physical quantities involved).

The equations are transformed into a dimensionless form in Fourier-space. Then, fluctuation-dissipation theorem is applied to the transformed equations which give the Anderson-Tamma spectrum (see further [5]).

$$S_{b}(k,\omega) = \left[ \left( 1 + \sigma\tau_{b} - \rho c \frac{\omega}{k} \right)^{2} + \left( \tau_{b}\omega + \frac{\rho cR\sigma}{k} \right)^{2} \right] \times \frac{K(Kn)k^{2}}{\left( \frac{K(Kn)}{\rho c \tau} k^{2} - \tau \omega^{2} \right)^{2} + \left( 1 + \frac{\tau K_{F}(Kn)}{\rho c} k^{2} \right)^{2} \omega^{2}}$$
(5)

The corresponding correlation function can be estimated with inverse Fourier transform.

#### 1.2 Anderson-Tamma spectrum

The Anderson-Tamma model incorporates both size-effects and boundary effects and numerous parameters are involved in the governing equations.

Table 1: Physical quantities in the A-T spectrum (eq. (5))

Quantity	Name	Empirical values
с	Specific heat	710 J / kg·K
ρ	Density	2230 kg/m <sup>3</sup>
K	Bulk heat conductivity	149 W/m·K
K <sub>F</sub>	Heat cond. retardation	10 W/m·K
τ	Relaxation time	10 <sup>-8</sup> s
$\tau_{\rm b}$	Boundary relax. time	$5 \cdot 10^{-10}  s$
l <sub>free</sub>	Phonon MFP	200·10 <sup>-9</sup> m
L	Sample length	60·10 <sup>-9</sup> m
R	Thermal contact resistance	$10^{-8}10^{-6} \text{ m}^2\text{K/W}$
σ	Damping factor	10 <sup>-8</sup> 1/s

## 1.3 Size-dependent thermal conductivity

In classical thermodynamics the thermal conductivity is usually assumed to be constant with respect to the size of the sample. On nanometre scale, thermal conductivity will depend of the characteristic length of the sample.

The mathematical description of the effect was formulated by Alvarez and Jou based on the phonon Boltzmann equation that is able to capture the phonon-boundary scattering [7]. The dependency can be expressed by the compact term of

$$K'(Kn) = \frac{K}{2\pi^2 Kn^2} \left( \sqrt{1 + 4\pi^2 Kn^2} - 1 \right), \tag{6}$$

where K refers to the bulk heat conductivity and Kn is the Knudsen number, which is the ratio of the mean-free path and the characteristic length of the system.

#### **1.4 Dynamic phase transition**

Dynamic phase transition refers to a phase transition in the dynamical properties of the system which is a broader concept than the general thermodynamic term. Most common quantities, which could undergo of dynamical phase transition, are transport coefficients, relaxation rates and correlation functions. Generally, these quantities depend on the equations of motion and cannot be determined by equilibrium distributions at a given point of time. Transport coefficients can be measured directly, or can be obtained by scattering experiments [6].

During phase transition - near to the critical point - the system can exhibit anomalous behaviour with respect to its dynamical properties (similarly to its static properties).

Various experimental results, numerical computations and analytic investigations [4] show that dissipative irreversible transport can exhibit explicit wave-like ballistic propagation along with the well-known diffusive transport on nanoscale domain. This effect can be demonstrated through the transition of the correlation function.

#### 2 Results

The Anderson-Tamma spectrum shows a dynamic phase transition of heat transport within a nanoscale silicon sample.

For lower wavenumbers without boundary effects the spectrum reveals diffusive behaviour (fig. 1).



Figure 1: Spectrum for A-T model without boundary effect  $[k = 1000 \ 1/m]$ 

However, if boundary effects are turned on the structure of the spectrum differs (Fig. 2).



Figure 2: Spectrum for A-T model with boundary effect  $[k = 1000 \ 1/m]$ 

The plateau for higher wavenumbers refers to altered transport behaviour; (however it can be observed on very small timescales:  $\sim 10^{-10}$ s).



Figure 3: Correlation function A-T model without boundary effect  $[k = 1000 \ 1/m]$ 

The altered transport characteristics can be seen on the correlation plots (Fig. 4). Along with the diffusive behaviour an oscillatory effect can be observed.



Figure 4: Correlation function A-T model with boundary effect [k = 1000 1/m]

The plots are generated with Mathematica and MATLAB using realistic physical values seen in Table 1.

#### 2.1 Small Knudsen-number limit

In small sized samples, the boundary-dependent Anderson-Tamma model provides ballistic heat transport characteristics. On the other hand, the model should approach to bulk (i.e. only diffusive) solution if the sample size increases. As the Knudsen-number is defined as the ratio of the phonon mean-free path and the sample characteristic length this limit equivalent to the Kn  $\rightarrow 0$ .

However, the spectrum for different large sample size shows different behavior, see Fig. (5). Instead of approaching to the bulk curve, the second plateau becomes even more dominant; contradicting to the expectations, as a more dominant plateau implies more distinguishable oscillatory effect.



Figure 5: Spectrum for different sample sizes: 100 nm [blue], 400 nm [black] and 800 nm [yellow]

Thus, the assumption of a constant thermal contact resistance parameter does not seem to be valid.

One possible resolution of the problem is the introduction of a size-dependent thermal contact resistance (i.e. R(L)) function. The below ad hoc formula is suitable for a smooth transition of the spectrum when the sample size becomes larger:

$$R(L) = R_0 \exp(\min(-\frac{L - L_0}{a \cdot L_0}, 0)), \qquad (1)$$

where  $R_0$  is the constant thermal contact resistance,  $L_0$  is the original sample size and a is a scaling parameter.



Figure 6: Spectrum for different sample sizes: 100 nm [blue], 400 nm [black] and 800 nm [yellow] (modified R value)

On Fig. 6 it can be seen that the size-dependent thermal contact resistance function ensures that the spectrum approaches to the expected one as the second plateau disappears by the increase of the sample size. Thus correlation function shows similar characteristics to Fig. 3.,

which can be interpreted as the ballistic transport mode is fading out and only diffusive transport is occurring in the sample (i.e. dynamic phase transition).

## 3 Summary

In this paper, a dual-phase lag model for heat carriers was investigated with respect to the altering transport behaviour for small sample sizes. As dynamical phase transition is defined as the sudden change in the transport coefficients of the system measured through correlation functions, it can be concluded that heat carriers governed by the Anderson-Tamma model could undergo such a transition. Furthermore, the microscopic-macroscopic transition was investigated and a new functional form was proposed to the thermal contact resistance due to the inconsistent results from macroscopic sample.

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## Cost-efficient in-situ end-of-life prognostics of power dies and LEDs by junction temperature measurement

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## Abstract

Lifetime (or health) monitoring in modern power electronics & luminaries continuously gains in importance, especially if safety-relevant applications are in the focus. Moreover, technology development of such devices requires fast and if possible continuous assessment of structural integrity. This work proposes a simplification of transient thermal testing (TTA) of LEDs by condensing measurement data analysis into one characteristic value to be stored and compared to successive or previous measurements for damage evaluation. Our custom-built in-situ monitoring system is based on microcontroller (uC) functionalities and can be used as stand-alone solution for reliability testing without any other electronic equipment. For quantitative assessment of measurement system performance we used Luxeon Z LEDs with different thermal interface materials. Pre-calibrated samples were inspected for structural integrity before and after cycling tests by X-Ray inspection. Measurement concept as detection for failure at thermal interface or die attach was qualitatively proven by correlation with structure function.

## 1 Introduction

Reliability problems due to cyclic thermo-mechanical loading, especially in power electronics, are still a big subject of scientific research. Due to alternating operation conditions like ambient temperature, humidity or mechanical stresses interconnects will undergo fatigue failure over time, which can finally lead to fatal failure within the bulk of the material (e.g. cracks) or at the interface (i.e. delamination) [1]. Conventional inspection methods like scanning acoustic microscopy (SAM) [2, 3] or 3D X-Ray scan [4] are time-honoured methods, which are able to detect failures during product qualification or lifetime model validation. But modern complex systems often require online health monitoring of components at risk to prevent total system damage during field operation or qualification.

An eligible health monitoring system must be ideally applicable to a wide variety of components, enabling a fast evaluation result referring to a chosen failure criterion and lifetime model (see figure 1). Further crucial requirements are miniaturization, minimum electric power consumption and ultra-low cost. Such measurement units are also expected to be a scalable solution for integration into security and safety systems with high reliability requirements. In recent years a variety of publications have already shown several prognostics and health monitoring solutions in power electronics. A review of the methods can be found in [5].

Speaking of switching power modules like MOSFETs, the frequency response of the output voltage and subsequent

spectrum analysis using Volterra series can be applied to determine the state of health. The self-driving signal of MOSFETs could be used to extract the degradation characteristics [6].

Lifetime estimation for high power LEDs can be performed using light output measurement for pre-defined operation temperatures [7]. However the light measurement techniques require specialized measurement set-ups and time consuming data analysis, which is usually not suitable for online health monitoring during operation.



Figure 1: Exemplified device status evaluation by monitoring of a failure-correlated observable (failure indicator) for a defined failure criterion and lifetime behaviour. The value for the failure criterion (conservative, relaxed) is set by the application.

As mentioned above, a most critical failure mode in power electronics is die attach degradation, which has a direct impact on heat dissipation within the device. Thus, Transient thermal analysis (TTA), based on transient thermal impedance measurement, can be also applied for in-situ health-monitoring of power modules. It was already shown, that the method is suitable for thermal interface characterization [8] as well as for failure detection *within interface* (e.g. cracks of solder joint) or *on the boundary area between layers* (e.g. delamination of a LED die) [9]. Thus TTA makes it possible to detect the failure location with respect to a single interface and analyse this failure qualitatively in terms of Rth-value changes.

Nevertheless TTA or methods, described in [6-7] usually require expensive hardware and/or time-consuming calculations, based on large datasets. In this work we propose a *scalable* (realization can be also done a single IC with excitation and evaluation functionalities) *stand-alone solution* for in-situ health monitoring of power die and LEDs. The health monitoring solution overcomes cost- and time-consuming data acquisition techniques by well-defined simplifications, which will be described in the next section.

## 2 Concept and State of the Art

According to the Physics of Failure-based approach to health monitoring there are three basic approaches for IC (see figure 2) [10].



Figure 2: Health monitoring methods based on Physics of Failure. A) Data Logger with LCU; B) pre-calibrated lifetime sensor; C) Technology-immanent monitor structure [11]

The first one is *Data Logger with Life Cycle Unit* (LCU) [11] (figure 2A), which records stresses or loads (e.g. temperature, moisture, mechanical stress) in a form of condensed information. A LCU can be a highly integrated component, which is responsible for calculations. Thus, the information collected by a Data Logger will be evaluated by LCU according to a given implemented lifetime model which allows immediate calculation of the number of cycles to failure  $N_{\rm f.}$  LCUs can nowadays be integrated without problems into a complex functional system.

Another approach is the pre-calibrated lifetime sensor (figure 2B), which is integrated in a system and undergoes failure according a known lifetime model. The measurement information can be also collected by an LCU which can be external and is only connected to the system within certain maintenance intervals.

The third approach is the technology-immanent monitor structure (see figure 2C), which is also applied for this work. In this case the failure detection is performed by evaluation of a structure mounted within the device by the same processes as for other components. This may be any critical structure sensitive to fatigue loading, like a bond wire, solder bump or die attach. The component to be monitored can either be an active or a dummy component, depending on which kind of load (active or passive) one needs to take into account. According to this idea, we propose an in-situ health monitoring system which is based on junction temperature changes caused by thermal interface degradation or degradation of other adjacent functional layers.

## Measurement concept based on TTA

As mentioned above, TTA seems to be the only powerful method suitable for in-situ thermal characterization of multilayer semiconductor devices, as it is based on electrical signal analysis without any other optical and/or destructive interventions. Originally the approach was introduced by Szekely und Bien 1988 [12] and nowadays, with rising demand on non-destructive test methods, constantly gains in significance in the area of semiconductor thermal management. Based on TTA and corresponding analytical models a standardized routine for thermal resistance measurement of thermal interface materials was developed and distributed by JEDEC [14].

The measurement for TTA is usually performed in two steps (exemplified on cooling curve measurement for a LED): 1) internal heating of the Device under Test (DUT, in this case the LED) with a pre-defined power step. 2) Recording the forward voltage with a smaller sensing current during the cooling down phase. Thus, the cooling curve is characteristic for a specific device layer assembly and single layer properties, as it depends on heat capacity C<sub>th</sub> and thermal resistance R<sub>th</sub> of each component. A special algorithm [12-14] can be then applied to calculate a characteristic structure function, which represents the heat path of the device as cumulative C<sub>th</sub>- and R<sub>th</sub>-values. This function acts as a thermal fingerprint of the heat path of the component from junction to ambient and will be used in this work as a confirmation for assumed failure modes. But again this method is less suitable for a fast online monitoring, as it requires strict compliance with test conditions (e.g. active cooled heat sink, which temperature must be measured) and time-consuming complex calculations [12-14].

The measurement method for this work is similar to TTA: The DUT is heated up by a short heating current pulse (a few hundred of milliseconds, which is less intrusive for tested device). This saves time and power consumption. Afterwards we switch fast (in the range of 1  $\mu$ s) from the heating current to a smaller sense current (in the range of a few mA, depends on package size to avoid self-heating), which acts as sensing signal for cooling behavior measurement. As a result the measured LED forward voltage can be depicted as graphs for propagating damage of solder joint or thermal interface material (TIM) (see figure 3).


*Figure 3: Exemplified failure detection concept based on junction temperature measurement on the component.* 

As shown in figure 3 transient voltage (voltage values at short times after switching down to sense current) decreases with propagating solder joint delamination. By means of LED as a NTC (typical for a semiconductor) forward voltage decrease corresponds to temperature increase caused by degraded thermal conductance on the way from the heat source (e. g. recombination area for LED) to the heat sink (e. g. Insulated Metal Substrate (IMS) board) as shown in figure 4.



*Figure 4: Temperature gradient schematic exemplified of a LED die on a substrate* 

Generally the transient voltage decrease acts in our concept as a measure for degradation state. According to the mentioned simplifications failure position cannot be extracted precisely in opposite to the structure function method. However at real application conditions it is usually not required to provide an extensive analysis of single device layers. Rather fast and reliable information whether the DUT is damaged or not should be made available. This information can be used to decide if the device is in a critical state and must be replaced by a new one. In this work we provide a method to extract this kind of information. In order to obtain reliable evaluation results the measured values must be referenced to the actual test conditions like applied heating power step and ambient temperature. The ambient temperature creates the gradient between heated and cold areas and impacts directly on measured values. Thus temperature changes outside the DUT act as an offset, which can be subtracted from the reference measurements. It has to be noted that in case of LEDs the temperature coefficient (k-factor) aging due to the structural changes after cycling tests must be also considered [15].

# **3** Experimental Setup

The measurement routine as such is derived from commonly applied routine of TTA for LEDs. An active heating with a high drive current (in the range of 1A, depends on maximum operation values) is applied followed by a smaller sense current (from 1mA to 10mA). During measuring the forward voltage, which depends on device and ambient temperatures (cooling curve) is monitored. The value of sense current must be defined according to package type and size to avoid self-heating during measurement. As shown in figure 5 the basic circuit concept includes two functional parts: *Stress Unit* and *Evaluation Unit*.



Figure 5: First concept for in-situ health monitoring circuit

As the name suggests, *Stress Unit* is responsible for excitation signal conditioning. A simple MOSFET-circuitry allows to switch between heating & measurement currents very quickly (<1 $\mu$ s). Measurement current source is realized by a simple linear regulator and delivers 10mA *sense current*, which is suitable for the tested samples. The *heat current* is provided by supply voltage, which is regulated to 1A by a simple voltage divider. A monostable multivibrator switches between heating and sense signals.

The *Evaluation Unit* includes multiple comparators enabling the comparison of the DUT forward voltage with predefined reference voltage levels (realized by potentiometers) directly after switching off heating current. Thus, by using 5 rising/falling reference levels with adjustable step value it is possible to assess the actual degradation percentage according to a lifetime model. Flip-flops are responsible for evaluation results storage and adder finally sums the results of single comparator outputs into a single analog value, which can be used as device health indication.

Figure 6 shows the set-up of the first concept. Powering by a 9V Pb-battery allows avoiding disturbance from mains supply and increasing signal-to-noise ratio. Battery voltage is stabilized and reduced to 6.3V by a conventional voltage regulator for appropriate supply of the whole circuit.



stress unit

evaluation unit

Figure 6: First prototype of in-situ health monitoring circuit

The evaluation of the proposed health monitoring system was carried out with Luxeon Z LEDs (LUMILEDS<sup>®</sup>) attached to IMS boards. Two different die-attach materials were used: standard SnAgCu(SAC)-solder (figure 7A) and a newly developed sinter silver adhesive (figure 7B).



Figure 7: Luxeon Z LEDs on IMS board (LUMILEDS<sup>®</sup>). A) LEDs with standard SAC-solder as die attach; B) LED with newly developed sinter silver adhesive.

The Luxeon Z LEDs with SAC solder (figure 7A) were aged in 2 groups by:

- Temperature Cycle Test (TCT) for 1000 thermal cycles from -40°C to 150°C
- Accelerated Humidity Test (AHT) for 1000 hours at 85°C and 85% relative humidity

The Luxeon Z LEDs with sinter silver adhesive (figure 7B) were aged by

• Power Cycling with 1A for 5s at each cycle

### 4 Results

Luxeon Z LED samples (figure 7) were used to evaluate the performance of TIM degradation detection.

Figure 8 shows the cooling curves of the SAC solder samples after a short heating pulse (250ms at 1A).



Figure 8: Luxeon Z LED forward voltage vs. time after a 250ms heat pulse (SAC-solder samples); black curve: unstressed reference sample; red curve: sample aged for 1000 thermal cycles from -40°C to 150°C; green curve: sample aged by accelerated humidity test for 1000 hours at 85°C and 85% relative humidity

The measured forward voltage represents the junction temperature  $T_j$ . The decrease of the forward voltage ( $T_j$  increase) after 1000 thermal cycling tests (TCT) can be interpreted as TIM degradation, which is also confirmed by CT-scan (see figure 9A). The detected deviations between reference and TCT samples are about 10mV. This goes along with an approx. 60% delamination of the TIM layer.

For the AHT aging there is no significant degradation effect detectable. CT also shows no indication of degradation or delamination (figure 9B).



Figure 9: Computer tomography (CT) scan of thermal interface layer for aged samples; A: TCT, B: AHT

In addition to CT-scan the integral structure functions (see figure 10) were calculated (method described in [12-14]) based on equivalent measurement data as used for the graphs in figure 8.



Figure 10: Integral  $C_{th}$ -structure functions according to measurements shown in figure 8.

The calculations generally show shift of  $R_{th}$ -values for measurement after cycling at the plateau corresponding to the TIM. Increased  $R_{th}$ -values in this area also confirm the assumption of TIM degradation. Here it has to be noted that additional DUT structural aging is also effecting forward voltage deviations. Thus k-factor aging was included during data generation [15].

Samples with lower adhesion (according to figure 7B) were used for fast degradation growth. In this case power cycling shows to be a fast method.

Result before and after power cycling in 50 cycles steps are shown in figure 11. The junction temperature increases during power cycling similar to results for SAC-samples, whereby deviations up to 10mV from the reference signal were detected.



Figure 11: Luxeon Z LED (sinter silver adhesive TIM) forward voltage from 0 to 200 power cycles (1 A & 5 s heating for each cycle) in 50 cycles steps

In this case the results also imply TIM degradation. This was confirmed by cross-section (see figure 12).





Figure 12: Cross-section of power cycled Luxeon Z LED sample with sinter silver adhesive as TIM

As shown in figure 12 the TIM layer is partially delaminated from Ag metallization of the IMS board. This fact is supposed to be the main reason for junction temperature increase. For further confirmation integral structure functions were calculated (see figure 13).



Figure 13: Integral  $C_{th}$ -structure functions according to measurements shown in figure 11

As in the case for SAC-samples the shift of  $R_{th}$ -values at TIM related plateau can be observed.

### 5 Conclusions and Outlook

#### Conclusions

The developed in-situ health monitoring system successfully indicates TIM delamination under LED dies. For the analyzed test vehicles deviations of up to 10 mV from the values of unstressed devices were observed. This approximately corresponds to 5 K junction temperature increase compared to the reference. TIM delamination was confirmed by CT scans and cross-sections. The results of the in-situ health monitoring system were compared and verified with structure function calculations.

Summarized it can be stated that the proposed in-situ health monitoring system was suitable for LEDs by compliance with important test conditions (applied power step, ambient temperature, etc.). It was proved, that the proposed method makes it possible to give a fast and reliable assessment of a TIM degradation state as indicator for Luxeon Z LED aging propagation. Therefore only the LED forward voltage during cooling down after a short heat pulse with respect to ambient temperature was used as data source. K-factor aging as important degradation effect for LEDs was applied for measurement calibration.

#### Outlook

Although the first circuit version could provide sufficient evaluation results with respect to such requirements as measurement data evaluation speed and cost-efficiency, the smart part (self-calibration, automated calibration routine and/or calibration data storage) is not included. However it is required for fast adjustments of test and evaluation conditions (heating and cooling time, transient voltage time point, etc.) with respect to a variety of DUTs. Thus it was decided to build up the second prototype of health monitoring circuit with calculation and evaluation functionalities. As shown in figure 14 the 2<sup>nd</sup> circuit concept includes two functional parts similar to the first concept: Stress Logic part and Control & Evaluation part. As the name suggests, Stress Logic part is responsible for excitation signal conditioning. Again a simple MOSFET-circuitry allows to switch between heating & measurement currents very quickly (<1µs). Measurement current source is realized by the same linear regulator and delivers 10 mA sensing current. Moreover Stress Logic Unit contains additional parts for signal preparation and stabilization like appropriate decoupling capacitors.



Figure 14: End-of-Life monitoring circuit concept based on uC-functionalities

The *Control & Evaluation* unit, including a microcontroller, represents the *smart part* of the concept, which offers a great variety of automated measurement possibilities. While the ADC is responsible for signal acquisition, general purpose digital outputs control the switching logic. It is also possible to modify measurement settings by Operation Control or extract extended evaluation information to PC by COM interface.

As shown in figure 15 Control & Evaluation Unit is stacked on the Stress Logic Unit. This also minimizes noise and save place for the whole prototype setup.



Figure 15: Measurement setup for in-situ health monitoring as stand-alone solution (powered only by a 12V Pb battery)

For further development an ASIC could replace most of the used components to provide the needed stress logic, evaluation and data storage functionalities.

Measurements made by this prototype show a similar resolution as for previous circuit of about 1 mV (ca. 0,5 K regarding to Luxeon Z LED temperature coefficient), which is sufficient with respect to the observed deviations between different cycling states and common ambient temperature deviations.

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# **Electronic Module for the Thermal Monitoring of a Li-ion Battery Cell through the Electrochemical Impedance Estimation.**

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#### Abstract

Electrochemical impedance is a not directly measurable parameter of the Li-ion cells that can be exploited to retrieve useful information about the state of the cell itself, such as the State of Charge or the internal temperature. This complex parameter depends on the frequency, which means that its real and imaginary parts change in function of the frequency at which the cell is activated. Nowadays impedance is mainly measured using laboratory equipment as part of dedicated benchmarks, requiring expensive facilities and relatively long procedures. In this paper we propose a new solution to get the impedance value of a Li-ion cell by using both an efficient approach minimizing the test duration, and an innovative electronic solution suitable for automotive embedded needs. The electrochemical impedance is then analysed to deduce the cell's internal temperature with experimental results.

### 1 Background

The miniaturization of the analog and digital electronic components is leading the technology of embedded systems towards a higher level of both integration and complexity. The reduction of complexity is the main objective of the "3CCar" (Components for Complexity Control in affordable electrified Cars) European project [1], to which the CEA is contributing. At the same time, new applications in transport and energy storage require the use of Li-ion batteries. Advanced battery management systems (BMS) including electrochemical impedance measurement are studied for the determination of the state of the battery, the prediction of the autonomy and the failure and safety management. Joining these two domains, one of the main research axes developed in 3Ccar is the study and the integration of a Smart Cell. This term usually refers to a Li-ion battery cell to which a certain amount of electronics is coupled and integrated into the same sealed case. The aim is to enhance its interactions with the external world and to make it capable of self-measurement, self-protection and powerline communication.

One of the most substantial parameter that can be implemented into a Smart Cell is its electrochemical impedance estimation, often called EIS for Electrochemical Impedance Spectroscopy. This quantity is known to provide significant information on some most critical parameters of a Li-ion cell, i.e. the State of Charge (SoC[%]), the State of Health (SoH[%]) and especially the cell's internal temperature (T[°C]) [2, 3, 4]. Nevertheless, even though the EIS of Li-ion battery cells is widely used in laboratories, in test centres and production, its potential for embedded applications is hardly exploited. That is mainly because the EIS procedures are often time consuming and energy consuming for the cell under test, as well as inaccurate and not easy to be put in relation with only one physical phenomenon occurring inside the cell.

With the ambition to find a new path for the electrochemical impedance measurement application, in "3Ccar" the knowledge of this not directly measurable parameter is exploited for the prediction of the thermal state of the cell and the prevention of its thermal runaway. Thus, a sensorless temperature measurement method based on the continuous estimation of its impedance, as proposed by the Technical University of Eindhoven (TU/e) [5], is applied with the purpose to perform it within a completely embedded system developed by the CEA.

### 2 Methodology

A method for the impedance estimation suitable for an embedded application is studied. Our approach, based on two technical breakthroughs, provides a good trade-off between measurement accuracy and test duration. Our innovative system was tested on the benchmark described below using a QinetiQ Li-ion cell [6] (QinetiQ is a member of the "3Ccar" consortium, UK). It is a 12 Ah poached cell, NCA-type (Lithium Nickel Cobalt Aluminium Oxide, LiNiCoAlO2), with an energy density of 220 Wh/Kg.

#### 2.1 Wide band cell activation

We firstly chose to focus on the development of wide band frequency identification method [7] to estimate the cell impedance. This approach is generic, reliable and requires low computation means as it is based on Fast Fourier transform [8]. The choice of the frequency band to address depends on the application: for the internal temperature estimation we focused on the part of the impedance that is mainly affected by the temperature more than by the other cell's parameters, that is 80 Hz to 2 kHz for the used sample cells. To excite the system, a *Pseudo Random Binary* 

Sequence (PRBS) [9] is applied as current input (*Figure 1*), which simplifies electronics. The PRBS is characterized by a flat power spectral density on a precise frequency band adjusted in function of the frequency area required for the thermal monitoring.



*Figure 1: Electrochemical impedance estimation with galvanostatic approach.* 

#### 2.2 Embedded hardware for galvanostatic activation

We secondly developed an embedded electronic analog module capable to switch a controlled current from the cell (galvanostatic activation) on a controlled load during the measurement of the voltage variation of the cell. The switched current can follow any kind of time-shaped signal, allowing the smoothing of the current shape if required for the cell preserving. The onboard amplification of the cell's parameters provides optimal use of the conversion range of the ADC of a microcontroller, improving the accuracy of the estimation [10]. It is important to point out that all the embedded electronics, microcontroller included, are designed to be supplied by the cell itself without affecting the result of the impedance estimation. As the development of the software of the digital part of the embedded electronics will not be available before mid-2017, the acquisition and computation steps were implemented into a specific benchmark, to evaluate the performances of the analog electronics and assessing the reliability of the sensorless temperature measurement through the impedance estimation.

### 2.3 Benchmark

The test chain we used is depicted in the block diagram of *Figure 2*.



Figure 2: Schematic description of the benchmark used to perform the impedance estimation with the embedded analog electronics at different temperatures.

The meaning of each block of this benchmark is:

- 1. Li-ion cell, with 4-point connection to electronics (recommended for low-resistance measurements).
- 2. Analog electronic embedded circuit, power supplied by the cell itself. It consists on:

- i. a linear system controlling a resistive load connected to the cell, switching a precise amount of current depending on the amplitude of the voltage control applied at its input;
- ii. a high-pass high-gain amplifier for cell voltage;
- iii. a differential amplifier measuring on a 0.1  $\Omega$  shunt the current delivered by the cell.
- 3. OROS OR36 high resolution input/output system, recording the output of the two amplifiers and applying the voltage which controls the switched current.
- 4. PC controlling the whole benchmark, retrieving the recorded data from the OROS OR36 and performing impedance computation.
- 5. Tektronix AFG3102 waveform generator, playing a 12.6 ms-long PRBS in loop.

The functions represented by the blocks n. 3, 4 and 5 will be enclosed in the embedded microcontroller software as a part of a further development.

Moreover, the Li-ion cell and the analog electronics were put inside a Vötsch VT4010 climatic chamber. A thermocouple was taped on one side of the cell, measuring its surface temperature.



Figure 3: Benchmark prepared for tests in temperature.

For every temperature reached by the climatic chamber, 10 minutes were waited in order to let the cell reach a stable thermal state. Thus the temperature measured by the thermocouple on the side of the cell could be assumed to be the same as the temperature inside the cell.

By bringing the cell at known and fixed States of Charge and keeping it at a constant State of Health, many measurements at different temperatures were carried out, highlighting the relationship between the electrochemical impedance of the cell and its internal temperature. We assumed that the SoH of the cell was 100% (brand new cell, no affected by ageing) and no cycle was applied to the battery in order to preserve this value, except once to lower its SoC from 100% to 29.1%. The SoC change was deduced by coulomb counting, practically making the cell deliver a fixed amount of current on a controlled load for a precise time [11, 12].



Figure 4: Prototype of the analog electronic circuit (upper board) for Electrochemical Impedance Estimation coupled with a digital microcontroller platform (lower board, software expected by mid-2017).

# **3 RESULTS**

Electrochemical impedance values were obtained for each temperature from 5°C to 55°C, with a 10°C step, at two different SoC (100% and 29.1%). Each measurement was repeated 20 times for statistical purposes, thus giving 20 impedance estimates for each tested temperature and SoC.

The thermal information of the internal state of the cell is carried out by studying the frequency where the imaginary part (Im(Z)) of the estimated impedance (as the impedance phase) is null. In other words, this corresponds to determining at which activation frequency (also known as the 'zero cross frequency') the cell's output impedance behaves as a pure resistive load. The bandwidth covered by the PRBS used as activation signal was set with the purpose of addressing the frequencies at which the zero cross may occur.



Figure 6: Impedance represented on a Nyquist diagram, where the point at which the imaginary part is null was marked.

A temperature increase causes a decrease of the zero cross frequency. The results are illustrated in *Figure* 6, where this frequency, computed from the estimated impedance, is

plotted as a function of the cell's surface temperature for the two tested SoCs. Only one averaged zero cross frequency value is plotted from the 20 measurements performed at the same temperature and SoC. The worst standard deviation observed among measurements performed at the same temperature and SoC was equal to 0.85 Hz, measured at 35°C and with a SoC of 29.1%.

Our results highlight that the relation between the zero cross frequency of the imaginary part of the impedance (obtained with our embedded analog electronics applying a PRBS as activation sequence) and the cell's internal temperature can be approximated with a second order polynomial law, with a Coefficient of Determination ( $R^2$ ) above 0.9992 in the worst case (at SoC=29.1%).

We also observed that even if the SoC difference between the first and the second series of tests is very large (>70%), its influence is very limited: in the worst case (at 55°C), the difference between the zero cross frequency at SoC=100% and SoC=29.1% is of 52 Hz. This implies that even without taking into account the SoC of the cell, we could be able to determinate its internal temperature with an error lower than 2°C. We deduce this by considering that if we approximate the relationships reported in Figure 6 with a linear interpolation, we get a variation of about -20 Hz for every °C of temperature increase. Furthermore, if the SoC is also known by the standard BMS of the vehicle, as it is supposed to be in any automotive application, the internal temperature estimation becomes even more precise, as we demonstrated that the standard deviation among 20 measurements is lower than 1 Hz, corresponding to an error in temperature of 0.05°C.



Figure 5: Impedance imaginary part zero-cross frequency vs. cell's temperature for the two tested SoCs; the dotted lines represent their second order polynomial approximations, whose equations are specified in the graph.

To model the relation between the zero cross frequency estimation and the internal temperature of the cell, a second order polynomial function represents a good compromise between the model complexity and the goodness of fit. With this choice, by setting the a, b and c coefficients with the values shown in *Figure 6*, the relationship can be analytically expressed by:

$$Freq[Hz] = a \cdot T[^{\circ}C]^2 + b \cdot T[^{\circ}C] + c \qquad (1)$$

This function can be easily reversed to deduce the cell's internal temperature from the zero cross frequency estimation:

$$T[^{\circ}C] = \frac{-b - \sqrt{b^2 - 4a(c - Freq[Hz])}}{2a}$$
(2)

## 4 Conclusions

The proposed cell-powered circuit and temperature estimation method give reliable and repetitive results, opening a promising path for a useful application of the electrochemical impedance estimation as a technique to implement sensorless internal temperature measurement. Moreover, all the system is dedicated to an embedded low power application for the automotive industry. This achievement was reached by implementing two innovative techniques: the wide band PRBS-based cell identification method and the embedded cell-powered galvanostatic activation and amplification system. After finalizing the embedded software, more enhanced tests will be possible, e.g. the assessment of the performances of different timeshaped signals and the exploitation of different parts of the power spectrum, extending the use of impedance information to the monitoring of other parameters of the cell.

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# **Multi-Objective Optimization of Fin Array Heat Sinks**

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#### Abstract

A method is presented to determine the temperature field of an electronics cooling heat sink. The method is based on calculation of heat conduction in a solid numerically with the finite volume method and on solving fluid convection from analytical equations. The model is suitable for forced and natural convection heat sinks, and it uses solutions of a parallel plate channel for the friction factor and the convection Nusselt number. The validity of the method is verified by comparing its results to measured data and to CFD calculations. After verification, two practical multi-objective optimization examples are given. The first one, an industrial application, is a forced convection heat sink composed of nine heat generating components at the base plate. Then, natural convection optimization is performed on a reference array with two components. In both cases, mass is minimized, the other criterion being the maximum temperature for forced convection case, and the heat sink outer volume for natural convection case.

#### 1 Introduction

A typical electronics cooling heat transfer problem consists of many discrete surface or flush mounted components, which are cooled by heat sinks. A typical heat sink in Fig. 1 is composed of fins and a base plate. The main criterion is to maintain component temperatures below fixed values to prevent overheating. If the fins are far apart, heat transfer analysis can be based on single fin behavior, but practical applications often require calculation of flow and heat transfer in a channel. Isothermal arrays with optimum channel width have been studied [1], but if we want to minimize mass or size, we must resort to non-isothermal analysis. For forced convection, flow can be laminar or turbulent but laminar for natural convection. Because the temperature distributions of a solid and fluid must be solved simultaneously, this is a typical conjugated heat transfer problem.

With fin arrays, single fin optimization results do not generally correspond to optimal fin shapes. However, these shapes can be used as a good initial guess to optimize the array geometry. Optimal solutions of single fins are presented in the literature, e.g., in [2, 3]. The optimum shape of a single fin with a constant mass has also been studied in [4], and easy-to-use analytical formulas for optimal fins shapes have been established for forced and natural convection cases when the fin base temperature is constant. Recently, a simple analytical solution was discovered by Matti Lindstedt and Reijo Karvinen [5] for constant heat flux at the fin base. The method is based on the results of a uniformly heated flat plate to calculate analytically the maximum temperature of a fin. The solution can be used to optimize a single fin.

This paper presents a quick and easy method to calculate the temperature field of a heat sink cooled by forced or natural convection, and the use of this method in the optimization of heat sinks. Two examples are shown on how optimization can reduce the size and mass of a heat sink.

#### 2 Theoretical background

The heat transfer analysis of the heat sink in Fig. 1 can be done with CFD, but in optimization the use of CFD requires plenty of time. Thus an alternative way to calculate heat sink performance in forced and natural convection is presented. It combines a numerical solution of conduction in a solid and an analytical treatment of fluid convection, thereby being many orders of magnitude faster than CFD. However, first analytical results of single fins are presented.



Figure 1: Schematics of a heat sink with plate fins and components at the base plate (m = 6.65 kg).

#### 2.1 Optimal shape of a single fin

The total heat transfer of the fin in Fig. 2 is obtained from the equation

$$\phi = \eta \phi_{\rm i} \,, \tag{1}$$

where  $\phi_i$  is the heat transfer of an isothermal fin, easily obtained from the correlations of an isothermal plate, and  $\eta$  is

the fin efficiency. The efficiencies of fins with different geometries can be presented for *forced convection* using the non-dimensional variable

$$X_{*} = \frac{1}{C} \frac{kt_{0}}{k_{f} l^{2}} \frac{L}{\text{Re}^{m} \text{Pr}^{n}},$$
(2)

where the coefficients for a laminar boundary layer are C = 0.332, m = 1/2, and n = 1/3; and for turbulent boundary layer C = 0.0296, m = 4/5, and n = 3/5. For instance, the efficiency of a rectangular fin in Fig. 2 (p = 0) takes the form

$$\eta = (mX_*)^{1/2} \tanh(mX_*)^{-1/2}.$$
 (3)

In the case of natural convection, the corresponding variable in (3) is

$$X_{*} = \frac{1}{C^{4}} \frac{\upsilon^{2}}{g\beta \operatorname{Pr}} \frac{1}{\theta_{0}} \left(\frac{kt_{0}}{k_{f}l^{2}}\right)^{4} L.$$
 (4)

From (3), it is easy to find the fin geometry to maximize heat transfer for a fixed fin volume. For an idea of how flow type and fin shape affect the total heat transfer rate, some results are given in Table 1 [4].

Table 1: Dimensions and characteristics of optimal aluminum fins with laminar and turbulent boundary layers in air flow. Fixed volume =  $1 \times 10^{-6} \text{ m}^3$ ,  $u_{\infty} = 10 \text{ m/s}$ ,  $\theta_0 = T_0 - T_{\infty} = 60 \text{ }^\circ\text{C}$  and fixed fin thickness  $2t_0 = 1 \text{ mm}$ .

p laminar	$\phi/\phi_{\rm ref}, \phi_{\rm ref} = 5.1 \ { m W}$	η	L	l
0	1	0.79	0.0505	0.0396
1/2	1.23	0.79	0.0742	0.0404
1	1.41	0.78	0.1	0.04
2	1.52	0.75	0.1573	0.0381
p turbulent	$\phi/\phi_{ m ref}$	η	L	l
0	1.18	0.91	0.084	0.0238
1/2	1.61	0.91	0.1313	0.0229
1	2.00	0.91	0.1874	0.0213
2	2.63	0.87	0.3	0.02

#### 3 Treatment of a fin array

In Fig. 1, heat conduction in the fins and base plate is governed by the energy equation

$$\frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2} + \frac{\partial^2 T}{\partial z^2} = 0, \qquad (5)$$

which is solved numerically using the finite volume method. Fins are here treated as two dimensional, because their temperature gradient is negligible in the fin thickness direction. In the base plate, conduction must be considered in all three directions. The details can be found in refs. [6,7,8]. To solve convection between the fins and the flow, the mean velocity and flow temperature in the channel of Fig. 3 are necessary to know.



Figure 2: Geometry of plate fins



Figure 3: Schematics of a channel

#### 3.1 Mean flow velocity in a channel

For *forced convection*, the mean velocity is obtained either from the known volumetric flow rate or by solving the operating point from the fan and system characteristics

$$\frac{1}{2}\rho V^2 \left(4f\frac{L}{d_{\rm h}} + \sum_{\rm i}\zeta_{\rm i}\right) = \Delta p , \qquad (6)$$

where  $\zeta$  is the minor loss coefficient,  $\Delta p$  is the pressure loss in a sink, and *f* is the apparent friction factor. For a laminar flow, *f* can be calculated as [9]

$$f \operatorname{Re} = 3.44 (x^{+})^{-0.5} + \frac{\frac{0.647}{4x^{+}} + 24 - 3.44 (x^{+})^{-0.5}}{1 + 0.000029 (x^{+})^{-2}}, \quad (7)$$

where the dimensionless length  $x^+ = x/(\text{Re}d_h)$  and hydraulic diameter  $d_h = 2d$  is used in the Reynolds number. For turbulent flow, we can use, for instance [10],

$$f = 0.0791 \left(\frac{2}{3} \operatorname{Re}_{d_{h}}\right)^{-1/4}, \qquad (8)$$

In the case of *natural convection*, the flow is created by buoyancy, and mean velocity is calculated from the force balance between the wall friction and buoyancy

$$V = \frac{g\beta d_{\rm h}}{2\nu(f\,{\rm Re})} \left(T_{\rm avg} - T_{\infty}\right),\tag{9}$$

where  $T_{\text{avg}}$  is the fluid average temperature in the channel. It is obtained from the local mean temperature

$$T_{\rm avg} = \frac{1}{L} \int_0^L T_{\rm m} {\rm dx} \,. \tag{10}$$

In (9), *f*Re is the friction factor times the Reynolds number, which is obtained for a laminar natural convection from (7). The mean velocity must be iterated with the fluid average temperature  $T_{\text{avg.}}$ 

#### 3.2 Mean flow temperature

The channels between fins are discretized, and the change in the fluid mean temperature is calculated for every cell in the channel. The flow is assumed one-dimensional in each segment, and the temperature change in a segment is

$$\frac{T_{\mathrm{m,out}}(x, y) - T_{\mathrm{w}}(x, y)}{T_{\mathrm{m,in}}(x, y) - T_{\mathrm{w}}(x, y)} = \exp\left(\frac{-4h(x, y)\Delta x}{\rho c_{\mathrm{p}} V d_{\mathrm{h}}}\right), (11)$$

where  $\Delta x$  is the cell length,  $T_{m,in}$  and  $T_{m,out}$  are the mean temperatures entering and exiting the current cell, and h(x,y) is the local heat transfer coefficient. For *laminar flow*, the local heat transfer coefficient is [9]

$$Nu = \frac{h(x, y)d_{h}}{k} = 7.541 +$$

$$6.874 (1000x^{*})^{-0.488} e^{-245x^{*}}$$
(12)

and for *turbulent flow*, the mean value is adequate and calculated from [11]

Nu = 
$$\frac{hd_{\rm h}}{k} = \frac{\frac{f}{2} (\text{Re} - 1000) \text{Pr}}{1 + 12.7 (\frac{f}{2})^{1/2} (\text{Pr}^{2/3} - 1)}$$
 (13)

Conduction from the fin surface to flow is coupled as

$$q(x, y) = h(x, y)[T_{\rm m}(x, y) - T_{\rm w}(x, y)]. \quad (14)$$

#### 3.3 Solution algorithm

Forced convection heat sink

1. Obtain a mean velocity V from fan curve equation (6) or use a given fixed value.

2. Initial guess of the  $T_w(x)$  distribution.

3.  $T_{\rm m}(x)$  from (11), for which h(x) is obtained from (12) or (13) if the flow is laminar/turbulent.

4. A new  $T_w(x)$  distribution by solving conduction in the fins and in the base plate using the finite volume method and combining it with the heat flux from fins to fluid from (14). 5. If the  $T_w(x)$  distribution differs from the previous value, calculation is repeated starting from point 3.

#### Natural convection heat sink

1. Initial guess of the average fluid temperature  $T_{avg}$  and the  $T_w(x)$  distribution.

- 2. The mean velocity *V* from (9), fRe from (7).
- 3.  $T_{\rm m}(x)$  from (11), for which h(x) is obtained from (12).

4. A new  $T_w(x)$  distribution by solving conduction in the fins and in the base plate using the finite volume method and combining it with the heat flux from fins to fluid from (14).

5. Updating the average fluid temperature  $T_{avg}$  from  $T_m(x)$  values using (10).

6. If  $T_{\text{avg}}$  differs from the previous value, calculation is repeated starting from point 2.

#### 3.4 Accuracy of the proposed model

The model was tested for *forced convection* by comparing the results to the experimental data of a plate fin heat sink with one heating element [7, 8]. The agreement was excellent. Verification of a *natural convection* case with a similar type of heat sink has been made by comparing our results to analytical results of an isothermal case in [12] and to CFD results in a non-isothermal case [13]. The agreement was not as good as in the case of forced convection but sufficient for design engineering purposes in optimization.

### 4 Multi-objective optimization

In multi-objective optimization, more than one conflicting criterion is minimized at the same time. As a result, a set of solutions, called Pareto-optimal solutions, are obtained. In contrast to single objective optimization, where only one optimum point is found, all Pareto-optimal solutions are mathematically equally good compromises. After multiobjective optimization, the decision maker chooses the final compromise design.

Multi-objective optimization may be performed with several different methods. In the weighted sum approach, the criteria are combined into a single objective function with different weights, and depending on the weights, a single Paretooptimal point is found. The problem here is that not all Paretooptima are accessible with this method. The constraint method is another method where only one criterion is minimized and where the other criteria are set as constraints. With this method, one Pareto-optimal solution can be found at a time. This is the method used to optimize a *forced convection* array in this paper. A faster method is to use multi-objective optimization algorithms, such as genetic or particle swarm optimization, to obtain all the Pareto-optimal solutions at once. This is the method used to optimize a *natural convection* array in this paper. These evolutionary algorithms can usually deal with discrete variables, such as number of fins, with no extra problems.

The heat sink design is constrained by volume or mass, locations and power of the heat sources, and in the case of forced convection also by fan power. Two optimization cases are presented below. First for *forced convection*, an industrial case is optimized in Fig. 1 by minimizing its mass and maximum temperatures. The fin cross section is also subject to variations between rectangular, triangular, and trapezoidal shapes. Another case, in Fig. 5, deals with *natural convection*, where the effect of the mass and volume of the array is shown.

#### 5 Results

In the case of *forced convection*, the mass of the array in Fig. 1 was 6.65 kg and the number of fins N = 41. With plate fins, the optimized mass is 3.41 kg, and component locations are changed and N = 48. The best result is obtained if also trapezoidal fins are selected. Fig. 4 shows the optimized array geometry: mass is 2.75 kg, N = 53, and component maximum temperatures are the same as in Fig. 1.

Another example shows how optimization reduces the mass and volume of a *natural convection* array in Fig. 5 by maintaining the same maximum temperatures of the components. The final result can be seen also in Fig. 5 on the right, where the mass was reduced by about 50 % and the outer volume by about 40 %.



Figure 4: Optimized heat sink with trapezoidal fins, m = 2.75 kg.

### 6 Conclusions

A method is presented to calculate the temperature field of a heat sink where typically the maximum temperature is the most interesting design factor. The method calculates temperatures many orders of magnitude faster than CFD, and it can be applied to industrial case optimization, where CFD would be too time consuming. The optimization that we have presented here shows that in some cases the current industrial heat sinks deviate considerably from optimum design.



Figure 5: Original array (left) and optimized (right).

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# **Improved Method for Logi-Thermal Simulation With Temperature Dependent Signal Delay**

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#### Abstract

Evolution of the semiconductor manufacturing allows integrating more components on a single die which further increase the complexity of the chips and introduce new design challenges. Power dissipation density has reached the limits of current cooling solutions, thus thermal-aware decisions must be taken into account during the design process. Co-simulating the logic function and thermal behaviour of the design can help to evaluate the performance of the system at various stages of the design process. Logi-thermal simulators use the switching activities of the system to predict the dissipated power and calculate the temperature distribution across the chip. The temperature dependence of certain parameters (such as delay) can also be considered during the co-simulation. This paper presents an improved method for temperature dependent signal delays compared to previous solutions. Our approach is based on mixed abstraction level logic simulation, which reduce the simulation time while the temperature distribution and the calculated delays remain accurate.

## 1 Introduction

As the continuous evolution of the semiconductor technology allows the manufacturing of more and more complex ICs, power dissipation and thermal management become design bottlenecks. The temperature and power dissipation wall enforce the designers to implement sophisticated thermal management policies. Electrical and thermal behaviour of a circuit can be co-simulated with electro-thermal simulation method, but this approach works on transistor level circuit descriptions, thus it is not viable for analysing the thermal behaviour of complex digital circuits due to the excessive computational requirements.

Logi-thermal simulation paradigm is based on the so-called *simulator coupling* technique: a logic simulation engine and a thermal simulation engine are connected in a loop [1]. Power dissipation of the IC is predicted based on the switching activity of the logic gates. Gate level logic description combined with the layout of the circuit and an appropriate energy model can be used to determine the power dissipation distribution of the chip. This dissipation map is used as an input for the thermal simulator which calculates the corresponding temperature map. Temperature values are then back annotated to the logic engine thus the temperature dependent parameters can be updated. After this update, the logic engine can advance the simulation time.

### 2 Previous work

Previous implementation logi-thermal simulation called *Celltherm* uses standard cell libraries in conjunction with EDA tools to achieve the co-simulation of logic functionality and thermal behaviour [2]. As this simulator uses gate level circuit description, the resulting temperature distribution is accurate on the level of standard cells, thus the calculated dissipations and signal delays are accurate [3], [4]. This was

verified by Spice simulations on transistor level. In this paper we consider the gate level logi-thermal simulation as baseline and the results of RTL logi-thermal simulations are compared to the corresponding gate level ones.

An alternate approach, which coupled an in-house unique logic simulation engine and a fast thermal simulator was described in [5] and [6]. This solution supports multilevel of abstraction but the unique logic engine was a main disadvantage (the circuit had to be re-implemented to perform logi-thermal simulation). This issue was solved by changing the logic engine to an industry standard hardware description language [7].

The logi-thermal framework used in the present work can be considered as an evolution of the concept described in [5], [6] and [7], but major improvements were made which increase the flexibility of the tool. Fundamental differences between previous implementations and the current solution is the new adapter approach towards the logic and thermal engines, which allows the seamless integration of any logic and thermal simulation engines.

Another approach by Bouhadiba et al. for co-simulating the thermal behaviour and logic functionality works with high abstraction level models [8], [9]. SystemC TLM functional models were used, which allows to evaluate the software behaviour from thermal aspects. The power models used in this approach cannot be evaluated exclusively from the specification transaction level models, UPF and measurements on implementations are also needed. Another system level approach for thermal aware design space exploration called Ctherm was described in [10]. Ctherm uses area, timing and power estimation tools to estimate the necessary input data for the co-simulation of the thermal and logic behaviour. These tools can only estimate the parameters of common structures in existing circuits, unique IP cores cannot be analysed.



Figure 1: Co-simulation frameworks in the design flow

Figure 1 depicts a simplified design process with logic and thermal co-simulation frameworks on the corresponding abstraction levels. The *LogiTherm* framework used in our work can accommodate gate level and RTL circuit descriptions as well.

# 3 Logi-thermal simulation on different abstraction levels

The basic functionality of our framework can be seen in Figure 2. Generic interfaces for the logic simulator and thermal simulator engines were designed which provide the flexibility to integrate any simulator engine in LogiTherm. Adapters for SystemC and Verilog hardware description languages, and SUNRED [11] and 3D-ICE [12] thermal simulator engines have been implemented.



### Figure 2: LogiTherm framework

Co-simulating the functional and thermal behaviour of a system requires not only the functional description (e.g. gate level netlist, RTL model) but information about the physical

arrangement of the system (e.g. layout) and dissipation model which predicts the dissipated power during the simulation as well.

Early, gate-level trial implementations of logi-thermal simulation [1] identified the different temperature dependent properties of different logic gates (standard cells) based on the SPICE simulations of their transistor level netlists. In everyday practice, details of transistor level realization of different logic gates as standard cells are not available. Instead, for a given standard cell library, the database of the process design kit (PDK) can be used to extract the required data, such as area information and predict the dissipation density of the circuit. On register transfer level however, these data must be estimated. In our present approach we use the result of a preliminary synthesis to estimate the area and dissipation of the RTL components in the design.

#### 3.1 Multiple linear regression based RTL power model

Power models used in logic and thermal co-simulation have to meet certain requirements. Fast evaluation of the logic components' power dissipation obligate small computational overhead. Large designs can comprise numerous RTL components, thus the parameters of the power model must be determined automatically. Multiple linear regression based power model introduced in [13] fit these requirements, thus we used this method of power estimation in our simulation framework.

In our approach we observe the switching activity of the ports of the logic components as the variables of the power model (1):

$$\hat{P}_d = P_0 + \sum_{j=1}^m \alpha_j P_j \tag{1}$$

where  $P_{0..}P_m$  denote the coefficients of the linear regression model, *m* is the number of ports of the component and  $a_j$  is the switching activity of the corresponding port.

The process to determine the coefficients of the power model can be automated. The characterization process is comprized by the following steps:

- Using the gate level netlist obtained by a preliminary synthesis, a power dissipation trace for every component is generated.
- The switching activity of the logic components' ports is recorded by applying the same stimuli used to produce the power dissipation trace.
- The coefficients of the power model are determined.

We used uniformly distributed random numbers as input during the characterization process. For this a test system composed by four simple processor core was used. The processor had 16-bit wide 3-address instruction set, 8-bit wide datapath and a register file with 16 entries. The size of one processor core was  $535\mu$ m× $559\mu$ m. Its structural RTL model was implemented and its gate level netlist was created by synthesis.

During a single cycle, the error introduced by the linear regression model can be up to 30%, but the expected value of the RTL and gate level power dissipation differs less than 2% as illustrated in Figure 3.



*Figure 3: Power dissipation estimation error* 

#### 3.2 Gate level and RTL logi-thermal simulations

Logi-thermal simulations were performed both on gate level and with RTL models with the same boundary conditions and parameters. As it can be seen in Table 1, logi-thermal simulation of the gate level model is by an order of magnitude slower than the RTL model.

*Table 1: Logi-thermal simulation time of RTL and gate level models.* 

Simulated time	Gate level	RTL
10 s	13857 s	1529 s

Relative temperature maps shown in Figure 4 illustrate the temperature distribution across the chip.



*Figure 4: Relative temperature maps of RTL and gate level implementations* 

During the simulations, uniform power dissipations were considered on every component, thus the higher level of abstraction introduced an error:

$$D[\%] = \left(\frac{T_{RTL}}{T_{GL}} - 1\right) \cdot 100 \tag{2}$$

where  $T_{RTL}$  and  $T_{GL}$  denotes the RTL and gate level relative temperature maps respectively. The worst case scenario, which was obtained by comparing every temperature map during logi-thermal simulations can be seen in Figure 5.



Figure 5: Difference of the two relative temperature maps

The maximal temperatures of the gate level and RTL implementation of the test system's ALU components can be seen in Figure 6.



*Figure 6: Maximal temperature of the ALU component on RTL and gate level and the error* 

The small difference between the RTL and gate level temperatures allows to consider temperature dependent parameters not only on gate level, but RTL as well, and perform mixed abstraction level (implementation which contains RTL and gate level components as well) logi-thermal simulations.

### 4 Temperature dependent signal delays

The database of standard cells, stored in Liberty file format in the process design kit contains the delay information of standard cells for pre-defined *process, voltage, temperature* (PVT\* corners. Actual delays are calculated by the synthesis tools and saved in *standard delay format* (SDF) files to enable post-mapping and post-layout simulation. The delays stored in such files are valid only in the PVT corners provided in the PDK, thus a database for temperature dependent signal delays must be built to perform accurate delay modeling for logithermal simulation.

Temperature dependent delay of a NAND20 standard cell can be seen in Figure 7. We obtained the delay information with series of Spice simulations, similarly the method described in [14].



Figure 7: Temperature dependent delay of NAND20 standard cell

# 4.1 Mixed level logi-thermal simulation with temperature dependent delay

In synchronous system a local datapath is represented by two registers which are in connection through combinational circuit. The datapath which has the largest delay is called critical path. Static timing analysis can determine the delay of the critical path at any design corner, but post-synthesis and post-mapping simulations with extracted delays are usually performed to analyse the circuit dynamic behaviour. Logithermal simulation allows to model the delays of the datapaths more accurately by considering the changing temperature of the IC.

Executing such logi-thermal simulations on models implemented on gate level can take several hours, and may be unnecessary. Instead of using the gate level implementation of the system, we used the result of the static timing analysis to identify the paths with the largest delay and only these paths were simulated on gate level to consider their temperature dependent delays, the rest of the test system were modelled on RTL.



Figure 8: Critical path of the test system

The start-point of the critical path is the instruction code register, and the end-point is the Z flag (see Figure 8). The

ripple carry chain in the arithmetic and logic unit is responsible for the largest part of the delay of the critical path even in this test system, which has only 8 bit wide datapath.

This method has significantly reduced the logi-thermal simulation time (see Table 2), while the error of the calculated delay illustrated in Figure 9 is under 3%.

Table 2: Logi-thermal simulation with temperaturedependent delay modelling



Figure 9: Delay of the critical path

## 5 Conclusion

In this paper we presented a method to speed up the logithermal simulation of digital designs with temperature dependent delay modelling. The multilevel abstraction capability of our logi-thermal simulator framework allows the thermal aware analysis of designs on RTL or on gate level. Simulation time can be significantly reduced by mixing the two abstraction levels and modelling only the critical parts of the system on gate level.

We are implementing a larger test system to further investigate the possible benefits and drawbacks of mixed level logi-thermal simulation.

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# Modelling of the Thermoelectrical Performance of Devices Based on VO<sub>2</sub>

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#### Abstract

By reaching the limits of conventional silicon-based integrated circuits, more and more effort is done to develop new devices for integrated circuits. A promising structure is based on the semiconductor-to-metal phase change of vanadium-dioxide at about 67°C. In these circuits the information is carried by combined thermal and electrical currents. Thermal effects cannot be separated so well in thermal-electronic circuits as electrical effects in electronic circuits thus, accurate distributed electrothermal simulation is mandatory. This paper presents three VO<sub>2</sub> material models, the algorithmic extension of an electrothermal field simulator to be able to handle the hysteresis of VO<sub>2</sub> and the modelling of VO<sub>2</sub> based devices. The paper compares measured and simulated device characteristics.

#### 1 Introduction

In the recent years Moore's law started to slow down as transistor sizes get near to atomic levels. Gordon Moore predicted in 2015 that the rate of progress of transistor counts would reach saturation in a decade [1]. By reaching the limits of conventional silicon-based integrated circuits, more and more effort is done to develop new devices for integrated circuits. The most promising exploratory beyond-CMOS technologies are aimed to replace the existing CMOS structures (electronic, ferroelectric, straintronic, orbitronic, spintronic devices) [2].

Another approach can fill the gap in existing and beyond-CMOS devices. This is the application of CMOS technology compatible new devices in a supplementary circuit layer over the CMOS circuits. The thermal-electronic logic circuit (TELC) is based on a thermal-electronic device: the phonsistor (a portmanteau of "phonon transistor") [3]. The physical phenomenon behind the phonsistor is the semiconductor-to-metal transition (SMT) effect shown by certain materials, for example vanadium-dioxide (VO<sub>2</sub>). This effect allows an electric resistance change in three to four orders of magnitude induced by thermal or electrical excitation [4].

#### 2 Methodology

Thermal effects cannot be separated so well in thermalelectronic circuits as electrical effects in electronic circuits thus, accurate distributed electro-thermal simulation is mandatory. Special electro-thermal properties i.e. nonlinearity and sharp electric resistance change of VO<sub>2</sub> cause problems in simulations. Some measurements show hysteresis nature for VO<sub>2</sub> [5]. Hysteresis modelling is a challenge for simulators because of the memory effect of the material. Our finite volumes method based field-simulation algorithm [6] is extended to handle these problems. The validity of simulated results is investigated by comparison of measured and simulated device characteristics.

The applied hysteresis model uses broken line function. The question is whether a continuous function model would give better results. Thus, a continuous function  $VO_2$  model is introduced without hysteresis, and it is compared to a broken line model without hysteresis and to the hysteresis model.

#### **3** Hysteresis simulation

Resistivity of vanadium-dioxide can show hysteresis in the characteristics and changes three to four orders of magnitude by increasing/decreasing temperature. This change is in the 55 to 75°C interval. Starting and finishing temperatures, steepness and hysteresis width depends on deposition properties of VO<sub>2</sub>, structure and material of the substrate, presence and proportion of V<sub>6</sub>O<sub>13</sub>, etc. [5] A typical VO<sub>2</sub> temperature-resistivity characteristics is shown in Fig. 1.



Figure 1: Resistivity as a function of temperature of (100) VO<sub>2</sub> [5]

For simulation we use our Finite Volumes Method (FVM) based field solver which uses the Successive Network Reduction (SUNRED) algorithm to solve the FVM equation [6]. Material model of SUNRED supports different types of nonlinearity (e.g. exponential, power function, diode equation, broken line, etc.), all of them are single-valued functions. Hysteresis function is a multivalued relation with memory effect, this requires a new material model.

The most challenging problem of hysteresis is the memory effect. If we use only "normal" nonlinear materials, i.e. without hysteresis, the next iteration in a DC calculation or the next step in a transient simulation requires

- the values of the state variables (temperatures, voltages) of the former step, and
- the material characteristics equations

to determine the state variable values of the actual step. In case of hysteresis materials, a phase-change happens in the material, and if the direction of the temperature-change is changing, the phase-back change does not start at the same temperature. The material model must remember

• the rate of the phase-change.

The new material model applied in SUNRED can be seen in Fig. 2. The model woks as follows:

- The model uses broken line function. Before and after the hysteresis domain this is a single valued function which consists of a linear segments. The hysteresis domain is parallelogram-shaped and if there is no phase-change in a step, the resistivity is constant.
- If the temperature is continuously increasing, the resistivity of the material changes along the *T0-T1-T2-T4-T5* curve. If the temperature continuously decreases from *T5*, the resistivity changes along the *T5-T4-T3-T1-T0* curve.
- The phase-change occurs in the *T2-T4* or in the *T3-T1* section. The rate of the change is 0% at *T2* and 100% at *T4* during heating and 100% at *T3* and 0% at *T1* during cooling.
- If the temperature increases from T0 to  $T_{push2}$  and then it starts to decrease, the resistivity remains constant until the temperature reaches  $T_{push1}$  (the "push line" will be the actual curve), the rate of phase-change does not change. From  $T_{push1}$  the curve will be  $T_{push1}$ -T1-T0. In the  $T_{push1}$ -T1 section the rate decreases to 0%.
- If the temperature decreases from *T5* to *T<sub>push1</sub>*, and then it increases back to *T5*, the actual curve will be *T5-T4-T3-T<sub>push1</sub>-T<sub>push2</sub>-T4-T5*.

Because of the strong nonlinearity and hysteresis of  $VO_2$  more than one stable operating point has the same simulated structure. Which operating point is established? It depends on the history of the system, and it is also affected by the heat capacitances of the structure. Thus, DC simulation is not encouraged, transient analysis can provide appropriate results.



Figure 2: Hysteresis model in SUNRED

The phase-change of VO<sub>2</sub> requires  $236,5 \cdot 10^6$  J/m<sup>3</sup> heat. This is modelled by increased heat-capacitance in SUNRED. The heat-capacitance is automatically increased during phase-change for each FVM cell (control volume).

Transient simulation is done in discrete times. This could cause the skipping of the whole hysteresis domain that could bring false simulation results. This is handled with an automatic process in the SUNRED algorithm: if the algorithm detects that the state of any of the FVM cells has changed (a) from normal domain to hysteresis domain or (b) from hysteresis domain to normal domain, and this change would result more than 10% phase-change, or (c) the whole hysteresis domain would be skipped, the algorithm steps back to the previous simulation time point, and recalculates with a smaller time step. The time step is set to an estimated 5% phase-change. If the simulated result exceeds 10% phase-change rate and the step-back algorithm required deep changes in the solution algorithm.

### 4 Continuous function model

A semi-empirical expression has been developed for better modeling of the resistance-temperature function (R(T)) of the metal-insulator transition (MIT) materials

$$R = \left( -a \frac{T-b}{\sqrt{(T-b)^2}} \frac{(T-b)^c}{(T-b)^c + d} + a \right) \exp \frac{e}{T} + g \quad (1)$$

In that model *a* is related to the range of the resistance drop at the phase change temperature marked by *b*. The temperature interval of the phase transition process and the slope of the curve are determined by *d* and *c*. The activation energy of the resistance-temperature function in the semiconductor state is taken into account by *e*, which is related to the forbidden bandgap of MIT material in semiconductor state. The exponential function describes strong temperature dependence, as it is typical of thermally activated processes. The resistance does not depend strongly on temperature in the metallic state at higher temperatures, it is described by *g*.

The function used in the simulations is shown in Fig. 3., where the R(T) function is plotted with  $a=10^{-6}$ , b=335 K,

*c*=2, *d*=0.01, *e*=4500 K (which corresponds to ~0.8 eV activation energy in semiconductor state),  $g=1.54 \text{ m}\Omega$ . The replotted curve is very similar to the original one, thus (1) properly describes the VO<sub>2</sub> behaviour.



Figure 3: R(T), measured curve of Fig. 1. and broken line model

#### 5 Results

The (1) function can be used in the SUNRED algorithm as is: a single-valued function. We will compare simulation results that use three different material models: (a) hysteresis model of Section 3, (b) the R(T) function of (1) and (c) a single-valued broken line model that fits well to the R(T) function.

#### 5.1 Temperature-voltage results

A simple model was developed for SUNRED simulations to gain temperature-voltage curves, see Fig. 4. On a  $32 \times 32$  mm<sup>2</sup> silicon die, an L shaped,  $12 \times 12$  mm<sup>2</sup> sized VO<sub>2</sub> formation was created. The vertical leg of the L was 5 mm, the horizontal leg was 4 mm. A  $6 \times 6$  mm<sup>2</sup> heat source was placed in the opposite corner of the die. The ambience of the dye was modelled with still air that had 10 W/m<sup>2</sup>K HTC.

The hysteresis model is defined with the following resistivity values:  $T0 = 20^{\circ}$ C: 5  $\Omega$ cm,  $T1 = 58^{\circ}$ C: 1.85  $\Omega$ cm,  $T2 = 64^{\circ}$ C: 1.85  $\Omega$ cm,  $T3 = 63^{\circ}$ C: 1.54 m $\Omega$ cm,  $T4 = 69^{\circ}$ C: 1.54 m $\Omega$ cm,  $T5 = 95^{\circ}$ C: 1.54 m $\Omega$ cm. The broken-line function is defined with four points: 27^{\circ}C: 6.54  $\Omega$ cm, 61.35°C: 1.37  $\Omega$ cm, 63.35°C: 1.54  $\Omega$ cm, 95°C: 1.54 m $\Omega$ cm.

The VO<sub>2</sub> structure was excited by 1  $\mu$ A current that resulted <6 nW extra dissipation which is negligible. Transient simulations were made with 1500 sec. heating time and 1500 sec. cooling time. The heating power was 1.5 W.



Figure 4: SUNRED model for temperature-voltage curves



Figure 5: SUNRED simulated temperature-voltage curves

Fig. 5. shows the simulated results. Both the voltage and the temperature were measured in the center of the anode.

It can be observed that not only the hysteresis VO<sub>2</sub> model produces hysteresis in the simulation, but also the R(T) function model and the broken line model. The gap between the up and down curve is about 2°C for both. The gap in the simulated curve of the hysteresis model is about 8°C, two degrees wider than the width set in the simulation (6°C). The explanation might be the difference between the paths of heat flux at heating and cooling. We will investigate it with other simulation structures in the future.

Some of our measurements show that the vanadium-dioxide has no hysteresis. This simulation proofs that hysteresis can be measured even if the material actually does not have hysteresis properties.

#### 5.2 Voltage-current results

A 200  $\mu$ m × 20  $\mu$ m area sized VO<sub>2</sub> resistor with 500 nm thickness, deposited on a silicon substrate was characterised in our laboratory, see Fig. 6. (a). The measured temperature to resistance diagram is shown in Fig. 6. (b). This structure was SUNRED modelled, see Fig. 7. (not to scale). A  $32 \times 32 \times 8$  resolution FVM grid was applied on the model. The resistor had a width of 4 grid cells.



Figure 6: (a) Photo of the experimental lateral TELC device (b) Measured resistance of the VO<sub>2</sub> resistor. [7]



Figure 7: SUNRED model for voltage-current curves

The hysteresis model is defined with the following resistivity values:  $T0 = 30^{\circ}$ C: 2.4  $\Omega$ cm,  $T1 = 57^{\circ}$ C: 1.2  $\Omega$ cm,  $T2 = 65^{\circ}$ C: 1.2  $\Omega$ cm,  $T3 = 65^{\circ}$ C: 1.2 m $\Omega$ cm,  $T4 = 73^{\circ}$ C: 12 m $\Omega$ cm,  $T5 = 95^{\circ}$ C: 12 m $\Omega$ cm. The R(T) function and the broken-line function model could not be used because the simulation started to oscillate because of the big slope of the functions. This problem may be eliminated by decreasing the transient time steps. At present this caused unacceptably long running times. We plan the development of the SUNRED algorithm with automatic runtime time step definition for optimal running times.

Fig. 8. shows the voltage to current measurement and simulation results of the VO<sub>2</sub> resistor. In the transient analysis the driving current was increased by 0.25 mA in each 10 ms until 20 mA, and then decreased to 0 mA. The results show an acceptable agreement with the measurement results, the difference is due to the low resolution of the model and broken line approximation function of the VO<sub>2</sub> model. In the simulation a one cell wide channel formed.

Two other SUNRED model was developed for more precise simulation results. A low resolution model with  $32 \times 32 \times 4$  cells where the resistor had a width of 12 grid cells, and a high resolution model with  $256 \times 256 \times 4$  cells with a 96 grid cells width resistor ( $3 \times$  and  $24 \times$  of the previous model). The results can be seen in Fig. 9. In the low res. simulation, a one cell wide channel forms at elbow (1) that starts to change to a two cell wide channel from elbow (2) at higher currents. (The channel is a low resistance part of the VO<sub>2</sub> where the VO<sub>2</sub> changed to metallic phase from semiconductor phase, and where the major part of the current flows.) In case of the high detail model the channel immediately becomes several cells wide at elbow (1) which further widens from elbow (2) to the top of the figure.



Figure 8: Measured and simulated voltage-current curves



Figure 9: Detailed model simulated voltage-current curves

In case of decreasing current, the channel begins to shrink at elbow (3) until it fully closes at elbow (4).

#### 6 Conclusions

New VO<sub>2</sub> electro-thermal models for the SUNRED algorithm were presented in this paper. Our simulations demonstrate that one-value functions can show hysteresis properties. We found that the discretization is a problem even in case of high detail models. However, measured and simulated curves show similar nature. More measurements and simulations are needed to clear the models real usability in TELC simulations. The development of the simulator is planned for better transient calculations.

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# Influence of the Photoactive Layer Thickness on the Device Parameters and their Temperature Dependence in Thin Crystalline Silicon Photovoltaic Devices

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#### Abstract

One of nowadays crucial questions with crystalline silicon solar cells is the reduction of manufacturing costs. One possible concept of reducing cost is to produce solar cells with thin photoactive layers, in order to use less amount of good quality and thus expensive raw material. In addition photovoltaic devices are one of the most obvious solutions for on-chip energy harvesting. There are basically two approaches: the monolithically integrated photovoltaic devices, and photovoltaic devices that are attached to the chip surface and connected to the integrated circuit. These devices also feature a thin photoactive layer in the majority of the cases. This paper aims to investigate the influence of the photoactive layer thickness on the on the photocurrent and the spectral response. It was found that the temperature dependence of these parameters increases with decreasing photoactive layer thickness. A possible explanation for this phenomenon is also presented.

#### 1 Introduction

One of nowadays crucial questions of crystalline silicon solar cells is the reduction of manufacturing costs. One of many concepts to reduce costs is to produce solar cells with thin photoactive layers, to use lower amount of high quality and thus expensive raw material. In 2014 The International Technology Road Map of Photovoltaics predicted a thickness if only 20 microns for the thinnest available technologies for the year 2024 [1], see Fig. 1.



Figure 1: Prediction of the development of the wafer thickness for crystalline silicon solar cells till 2014 [1]

There are basically two methods to reduce the amount of solar grade silicon in the cell structure. The first is to reduce the entire wafer thickness and reduce slicing waste by using smart cut or alternative kerfless wafering technologies [2, 3]. The other is to use low quality crystalline silicon with a solar grade epitaxial layer [4, 5]. In other studies even cheaper substrates such as ceramics [6], glass [7] or even metal [8] were considered.

In addition photovoltaic devices are one of the most obvious solutions for on-chip energy harvesting to power autonomous sensors or other small MEMS-based devices. Many different solutions and suggestions to incorporate PV devices into integrated circuits have been published. There are basically two approaches: monolithically integrated photovoltaic devices [9, 10, 11], and photovoltaic devices that are attached to the chip surface, and connected to the integrated circuit [12, 13, 14]. These devices also feature a thin photoactive layer in the majority of the cases. This paper aims to investigate the influence of the photoactive layer thickness on the photocurrent and spectral response and to give a qualitative explanation for the differences in their temperature dependence.

#### 2 Sample preparation and measurement methods

Investigations were performed on two types of samples. The first type of samples were monocrystalline silicon solar cells with a photoactive layer thickness of 10, 17, 24 and 31  $\mu$ m (for the schematic cross section of the samples see Fig. 2).



Figure 2: Cross section of the monocrystalline samples

These samples were fabricated by a special sample preparation method that is based on the EpiWE (Epitaxial Wafer Equivalent) approach [5]. Supplementary to the EpiWE approach all sample cells were prepared on the same wafer and different photoactive layer thicknesses were achieved by etching back the epitaxial layer locally with different etching times. Due to this it can be assured that the samples differ only in the thickness of the photoactive layer. All samples pass through the same processing steps in the same run, thus technological variations are minimized.

The second type of samples were p-i-n cells made from microcrystalline silicon. In these samples the thickness of the intrinsic absorber layer was altered, the samples had an absorber layer thickness of 2, 3, 5 and 6  $\mu$ m.

#### 2.1 Measurement method

The samples were investigated by the means of temperature dependent I-V curves and spectral response measurements. In both cases the samples were investigated in the temperature range of 10-85 °C, where the measurements were performed in steps of 1°C. The measurements were conducted in a climate chamber with a fixed temperature of 25 °C and fixed relative humidity of 30 %. This ensured that no condensation that could change optical properties was present on the samples at lower temperatures. The temperature of the sample was controlled by an external liquid thermostat that set the temperature of the measurement chuck. For data acquisition the temperature of the measurement chuck was measured.

The measurement was automatically controlled by a LabView program that set the temperature of the thermostat, started the measurement after the measurement chuck reached the desire temperature, and switched the illumination unit. Data acquisition (I-V curves and short circuit currents) and illumination were controlled over a data acquisition card.

For the measurement of the I-V curves the samples were illuminated with halogen lamps. The samples were investigated at different light intensities of 200, 398, 589, 792, 976, 1118 and 1268 W/m<sup>2</sup>. For the spectral response measurements the illumination was assured by LED-s with the following different wavelengths: 443, 504, 530, 638, 663, 742, 861, 968 nm.

### 2.2 Processing of measurement data

For the evaluation of the measurement results a curve of the form

$$I = \frac{R_{sh}}{R_{sh} + R_s} (I_{ph} + I_0) - \frac{U}{R_{sh} + R_s} - \frac{nU_T}{R_s} \cdot W \left( \frac{R_s \cdot I_0}{nU_T} \cdot \frac{R_{sh}}{R_{sh} + R_s} \cdot e^{\frac{R_{sh}}{R_{sh} + R_s} \frac{U + R_s(I_{ph} + I_0)}{nU_T}} \right)$$

was fitted to each measured I-V curve. The equation above represents the Lambert W function based explicit 5-parameter single diode model of a solar cell, so the fitting parameters are the photocurrent ( $I_{ph}$ ), the reverse saturation current ( $I_0$ ), the diode ideality factor (n) and the parasitic series ( $R_s$ ) and shunt ( $R_{sh}$ ) resistances, respectively. From these parameters all significant parameters of the solar cells can be calculated. The investigated photocurrent was extracted as one of the fitting parameter. After the extraction of the parameters from the I-V curves the temperature dependence was evaluated and the average temperature dependence was calculated for each sample and each light intensity.

#### 3 Results and Discussion

The temperature dependence of the photocurrent of the monocrystalline samples at 972 W/m<sup>2</sup> can be seen in Figure 4. It can be seen that the temperature dependence of the photocurrent increases with decreasing sample thickness.



Figure 4: Temperature dependence of photocurrent of the monocrystalline cells at 976  $W/m^2$ 

The same tendency can be seen from the average temperature coefficients of the samples at different light intensities, listed in Table 1.

Table 1: Average temperature coefficients of the photocurrent of the monocrystalline cells at different light intensities (%/ $^{\circ}C$ )

Light intensity	Sample thickness			
Light intensity	10 µm	17 µm	24 µm	31 µm
200 W/m <sup>2</sup>	0,263	0,264	0,239	0,236
398 W/m <sup>2</sup>	0,256	0,256	0,236	0,232
589 W/m <sup>2</sup>	0,252	0,251	0,232	0,228
792 W/m <sup>2</sup>	0,253	0,249	0,230	0,226
976 W/m <sup>2</sup>	0,250	0,245	0,226	0,221
1118 W/m <sup>2</sup>	0,242	0,236	0,218	0,212
1268 W/m <sup>2</sup>	0,239	0,232	0,215	0,209

To be able to give an explanation for the change in temperature dependence with photoactive layer thickness, the temperature dependence of the spectral response was also investigated. As it can be seen in Figure 5 the temperature dependence is mainly dominated by the components in the near infrared region, above 700 nm.



Figure 5: Temperature dependence of the spectral response of a monocrystalline sample cell

For the monocrystalline samples the average temperature coefficients of the spectral responses at each investigated wavelength are summarized in Table 2.

Table 2: Average temperature coefficient of the spectral response of the monocrystalline samples at different wavelengths  $(\%^{\circ}C)$ 

Wavelength	Sample thickness			
wavelength	10 µm	17 µm	24 µm	31 µm
443 nm	-0,05	-0,06	-0,03	-0,01
504 nm	-0,06	-0,07	-0,05	-0,03
531 nm	-0,04	-0,05	-0,04	-0,03
638 nm	0,06	0,05	0,04	0,03
668 nm	0,10	0,07	0,05	0,05
742 nm	0,24	0,20	0,17	0,16
862 nm	0,54	0,51	0,49	0,47
969 nm	0,82	0,86	0,87	0,86

From Table 2 it can be seen that the increase in temperature dependence with decreasing sample thickness is mainly due to higher temperature dependences in the near infrared region. This can be explained by temperature dependence of the absorption factor of the crystalline silicon and the incomplete absorption at higher wavelengths. Thicker photoactive layers can absorb more light, thus the excess photogeneration caused by the temperature rise is lower. Since the absorption factor of silicon decreases with wavelength, this higher temperature dependence is more significantly present in the infrared region. The fact that the photocurrent of the investigated samples increases with sample thickness supports this theory.

In case of the microcrystalline samples the I-V curves could be only evaluated at 200 W/m<sup>2</sup>, due to high contact resistances. However, due to the used data processing method this high parasitic resistance did not affect the extracted results. The temperature dependence of the photocurrents of the microcrystalline samples can be seen in Figure 6 and the average temperature coefficients for the photocurrent are summarized in Table 3.



Figure 6: Temperature dependence of the photocurrent of the microcrystalline samples at 200  $W/m^2$ 

The photocurrent of the microcrystalline samples partly shows similar behaviour than in case of the monocrystalline cells: the temperature dependence increases and the photocurrent decreases with decreasing absorber layer thickness (see Fig. 6).

Table 3: Average temperature	coefficients of the photocurrent
of the monocrystalline cells at	<i>different light intensities (%/°C)</i>

Light intensity	Sample thickness			
Light intensity	2 µm	3 µm	5 µm	6 µm
200 W/m <sup>2</sup>	0,083	0,076	0,089	0,099

However, there are also some differences: above a certain absorber layer thickness the temperature rises again and the photocurrent starts to decrease. The explanation for this could be that above a certain absorber thickness the diffusion length of the charge carriers will be lower, than the absorber layer thickness, and higher recombination losses will occur, i. e. the device turns from a narrow base diode into a wide base diode. This assumption is supported by the change in the reverse saturation current of the devices and the decrease of their spectral response in the visible region with increasing absorber layer thickness (Figure 8).



Figure 8: Spectral response of the microcrystalline samples at 25  $^{\circ}\mathrm{C}$ 

The temperature dependence of the spectral response of the microcrystalline cells shows the same behaviour than in case of the monocrystalline cells: the temperature is mainly present in the infrared region (see Figure XVII and Table 4).



Figure XVII: Temperature dependence of the spectral response of a microcrystalline cell

This leads to the assumption, that the temperature dependence can be explained by the same mechanisms than is case of the monocrystalline cells. However the overall temperature dependence is much lower than in case of the monocrystalline samples, and temperature dependence is present only at higher wavelengths. This is assumed to be caused by the higher absorption factor of microcrystalline silicon [15] compared to crystalline silicon [16].

Table 4: Average temperature coefficient of the spectral response of the microcrystalline samples at different wavelengths  $(\%^{\circ}C)$ 

Wayalangth	Sample thickness			
w avelength	10 µm	17 µm	24 µm	31 µm
443 nm	-0,05	0,01	0,04	0,03
504 nm	-0,06	0,00	0,03	0,01
531 nm	-0,04	0,00	0,03	0,01
638 nm	0,06	0,01	0,02	0,01
668 nm	0,10	0,02	0,02	0,01
742 nm	0,24	0,05	0,05	0,04
862 nm	0,54	0,13	0,10	0,11
969 nm	0,82	0,28	0,23	0,23

### 4 Conclusions

From the result it could be seen that with decreasing photoactive layer thickness the temperature dependence of the photocurrent rises. Spectral responses showed that the temperature dependence is mainly present in the infrared region. This can be explained mainly by to temperature dependence of the absorption factor of silicon that causes excess photogeneration if temperature rises. In case of the microcrystalline samples the temperature dependence was significantly lower. Thus in applications where the temperature dependence is important and the photoactive layer thickness is limited, the use of microcrystalline silicon photovoltaic devices could be advantageous. In case of high operating temperature the lower temperature dependence could also be an advantage. It can also be concluded that in case of the microcrystalline cells the thickness of the photoactive layer has to be chosen carefully, since after a certain thickness the temperature dependence will start to rise again due to increased recombination losses if the photoactive layer thickness exceeds the diffusion lengths of the charge carriers.

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# A Study of Electrolytic Capacitor's Thermal Conductivity, Behavior and Measurement

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#### Abstract

Electrolytic capacitors are widely used in electric circuits, and their durability is an important contributor for the entire lifespan of an electric device. In order to devise an adequate cooling solution to prevent the electrolytic capacitor from overheating or even burning, the thermal designer needs to completely understand the capacitor's thermal characteristics. In this study, the conductivity of electrolytic capacitor is calculated referring to capacitor's structure and material. Then, capacitor's heat exchange model is set up and all boundary conditions of this model are identified, capacitor's thermal behavior is studied by varying each boundary condition one by one. Furthermore, best point for capacitor temperature measurement is determined in this study. All outcomes of this study are helpful for capacitor's thermal solution design and verification.

#### 1 Introduction

Usually, electrolytic capacitor's lifetime can be estimated referring to its temperature data, for example:

$$L_{x} = L_{0} \times 2^{\frac{T_{0} - T_{1}}{10}} \times 2^{\frac{\Delta T_{0} - \Delta T_{1}}{10}}$$
(1)<sup>[1]</sup>

Where:  $L_x$  = Estimated life at working temperature  $T_1$  (hour)

 $L_0$  = Guaranteed life at temperature  $T_0$  (hour)

 $T_0$  = Maximum allowable working temperature (°C)

 $T_1$  = Actual working temperature (°C)

 $\Delta T_0$  = Internal temperature rise under maximum ripple current (°C)

 $\Delta T_l$  = Actual internal temperature rise (°C)

According to (1), a 10°C temperature rise, either ambient or internal temperature, will degrade the lifetime of the capacitor to 50%.

Due to the constraints of the capacitor working principle, it is very difficult to heat a capacitor with an accurately known power. It is also challenging to accurately measure the capacitor internal temperature.

Computational Fluid Dynamics (CFD) simulation is a major asset for this type of study. When coupled with real sample tests, CFD can be used to verify key results to ensure the overall accuracy of the study.

#### 2 Heat exchange of a capacitor on PCB

### 2.1 Heat exchange model

When a capacitor is mounted to a PCB, PCB joins the heat exchange of the capacitor. From a heat transfer point of view, heat is exchanged between the capacitor, PCB, and the ambient air. The heat transfer modes include conduction, convection, and radiation.

Figure 1 illustrates the heat transfer mechanisms. A thermal resistance network model can also be used to represent this. Since this study was focused on a forced convection system, the effect of heat radiation was ignored because it has very little effect on heat transfer due to the relatively low temperature of the capacitor.



Figure 1 Heat exchange model of a capacitor on PCB

#### 2.2 Heat transfer boundary conditions

From Figure 1, the ambient temperature; air velocity; and PCB temperature impact at least one heat transfer mode in this system, and so they are all boundary conditions for heat exchange of the capacitor.

Since the capacitor is a heat source, generating a certain amount of heat and heating itself. Referring to capacitor working principle, assuming all power loss converts to heat, and then the power loss of capacitor is also a boundary condition.

Meanwhile, the PCB was treated as a heatsink in the system, as it has much bigger thermal mass than the capacitor. The impact caused to the final result by this treatment can be ignored.

# **3** Modeling of a capacitor

#### 3.1 Internal structure of electrolytic capacitor

Figure 2(a) shows the internal structure of an electrolytic capacitor. In an actual capacitor, the Anode/Cathode Foil and Isolated Paper are wound together to form many layers.



**Figure 2 Capacitor Structure** 

#### 3.2 Conductivity equation of the winding structure

By using CFD simulation tool, the thermal designer can set up a capacitor model strictly following the actual structure, but this kind of approach is not always recommended, since it won't make the simulation more accurate. Instead, this kind of model increases both the grid density and cell count. A larger grid usually results in a longer solve time and bigger residual.

In order to avoid these issues, the winding structure can be simplified while still retaining the model's accuracy. For this winding structure, if the layers were unwound, the internal structure can be simplified to a stacked structure as shown in Figure 2(b).

Based on this simplified structure, the conductivity of the internal winding layer can be calculated by:

$$K_{r} = \frac{t}{\sum_{i=1}^{n} \frac{t_{i}}{K_{i}}}$$
$$K_{a} = \frac{\sum_{i=1}^{n} K_{i} \cdot t_{i}}{t}$$
(2)

Equation (2) refers to the effective conductivity of multiple objects combined in series and in parallel<sup>[2]</sup>.

In (2),  $K_r$  is the conductivity at radial direction, and  $K_a$  at axial direction. Obviously, the internal winding structure is anisotropic in terms of conductivity.

If the anode foil and cathode foil are made with aluminium (K=180W/m·K), and the isolation paper is a typical material which K=0.035W/m·K, then the capacitor  $K_r$ =0.08W/m·K, and  $K_a$ = 90.02 W/m·K.

In case of a different foil material, such as Tantalum, the capacitor's conductivity can be calculated accordingly.

### 3.3 Comparison of the simplified and original models

As the statement in earlier, the simplified model is much better for solving than the original. The differences are illustrated in figure 3, which also shows the grid of both models.



(a) Simplified model

(b) Original model

Figure 3 Grid of simulation models

Table.1 confirms the simulation parameters comparison, it is clear to see that the original model has a longer solving time and eventually becomes divergent.

	Simplified Model	Original Model
Cell Quantity	141,584	1,790,246
Max Aspect Ratio	7.33	35.10
Number of Iterations	350	750
Residual	1	>10
Residual/ Convergence	Convergent	Divergent
Solving Duration	13m:55s	58m:21s

# Table 1 Comparison of simplified and original models

#### 3.4 CFD model of a capacitor

With the calculated conductivity of the internal winding structure, a capacitor with a PCB CFD model can be set up as Figure 4. This model is used in following study.



Figure 4 CFD model of a capacitor

### 4 Capacitor cooling study

#### 4.1 Solution domain

Based on the study in earlier, the capacitor's power loss, PCB temperature, air velocity, and ambient temperature all impact the capacitor temperature.

The following study verifies how each boundary condition impacts the capacitor temperature. The initial conditions were set to:

- Capacitor power loss = 0.3W
- PCB temperature =  $80^{\circ}$ C
- Air velocity = 1 m/s
- Ambient temperature =  $45^{\circ}$ C.

In total four scenarios were studied. In each scenario, three of these four conditions are held constant, while the other is variable so as to show how this condition impacts the capacitor temperature.

Figure 5 shows the solution domain of this study, a DIP (Dual In-line Package) type capacitor with a piece of PCB is placed in a wind tunnel, air flow in the wind tunnel is perpendicular to axis of the capacitor.



Figure 5 Solution domain

As a heat conductor and also heat source, temperature distribution on the capacitor body is not uniform, so the temperatures of multiple points on the capacitor were monitored in the study, as follows:  $T_{top}$ ,  $T_{core}$ ,  $T_{site}$ ,  $T_{pin}$  (Figure 4).

 $T_{core}$  is the internal temperature of the capacitor so it is one of the key parameters for the capacitor lifetime estimation, but  $T_{core}$  could not be measured in a real system. So  $T_{top}$ ,  $T_{site}$ ,  $T_{pin}$  were monitored also, and temperature differences between core and top ( $\Delta T_{ct}$ ), core and side ( $\Delta T_{cs}$ ), and core and pin ( $\Delta T_{cp}$ ) were also studied.

#### 4.2 Variation in capacitor power loss

The power loss was to vary from 0.2W to 1.2W, and the temperature trend of each monitor point was verified.



(a) Trend of temperature

(b) Trend of temperature difference

Figure 6 Varication in capacitor power loss

Figure 6(a) shows the temperature trend,  $T_{core}$  increases in accordance with the increase of power loss, but  $T_{pin}$  is not impacted by the power loss increase at all.  $T_{site}$  shows a slight change but keeps within a small range (<5°C),  $T_{top}$  has an obvious increase and the trend is very similar to that of  $T_{core}$ .

Figure 6(b) shows the temperature difference trend. It results in  $\Delta T_{ct}$  only has very slight change (<1°C), while  $\Delta T_{cs}$  and  $\Delta T_{cp}$  have obvious change.

#### 4.3 Variation in PCB temperature

The PCB temperature was set to vary from 50°C to 100°C, and then the temperature trend of each monitor point was verified.



Figure 7 Variation in PCB temperature

Figure 7(a) shows the temperature trend, it appears all four points have obvious increases corresponding with the PCB temperature increase. This demonstrates the PCB temperature heavily impacts the capacitor's lifetime by directly conducting heat into the capacitor in some cases.

Figure 7(b) shows the temperature difference trend, it results in  $\Delta T_{ct}$  having a very slight change (<1°C), while  $\Delta T_{cs}$  and  $\Delta T_{cp}$  have obvious decrease with the PCB temperature increase.

#### 4.4 Variation in air velocity

Air velocity was set to vary from 0.05m/s to 1m/s, and then the temperature trend of each monitor point was verified.



Figure 8 Variation in air velocity

Figure 8(a) shows temperature trend, it appears  $T_{top}$  and  $T_{core}$  decreased in accordance with air flow velocity increase. While  $T_{pin}$  and  $T_{site}$  slightly decreased.

Figure 8(b) shows the temperature difference trend. It results in  $\Delta T_{ct}$  is just slightly changing (<1°C), while  $\Delta T_{cs}$  and  $\Delta T_{cp}$  have obvious decrease with air velocity decrease.

#### 4.5 Variation in ambient temperature

Ambient temperature was set to increase from 25°C to 75°C, and then temperature trend of each monitor point was verified.



**Figure 9 Variation in ambient temperature** 

Figure 9(a) shows the temperature trend, it appears ambient temperature impacts the temperature of all points.

Figure 9(b) shows the temperature difference trend. It results in  $\Delta T_{ct}$  is also slightly changing (<1 °C) only, while  $\Delta T_{cs}$  and  $\Delta T_{cp}$  have obvious increase with ambient temperature increase.

#### 5 Temperature Measurement Point Study

In a real system, only the external surface temperature of a capacitor can be measured, while, internal temperature is required for lifetime estimation. So a proper measurement point which has a small deviation from internal temperature needs to be defined.

Traditionally, most capacitor manufacturers recommend measuring pin temperature ( $T_{pin}$  in Figure 4) for a Double In-line Package (DIP) electrolytic capacitor, since pin is a high thermal conductor and is in contact with the capacitor internally. However, according to this study, the temperature difference between core and pin ( $\Delta T_{cp}$ ) is not constant, so that pin temperature could not correctly reflect internal temperature.

Figure 10 shows a capacitor's temperature field of a CFD simulation. In case PCB is hotter than the capacitor, pin temperature  $(T_{pin})$  is also higher than internal temperature  $(T_{core})$ .



Figure 10 Capacitor temperature field in CFD simulation

According to this study, the temperature at the top of the electrolytic capacitor case ( $T_{top}$  in Figure 4) is almost constant when boundary conditions change, so the top of the case is the best measurement point in the case where the airflow pattern is same as shown in Figure 5.

#### 6 Conclusion

This study developed a simplified electrolytic capacitor model for use in a CFD simulation. This simplification can improve grid density and quality in the simulation model, and thus improve the accuracy of the simulation.

This study also identified all boundary conditions that impact the electrolytic capacitor's cooling, and then verified how each boundary condition impacts the capacitor's temperature. Referring to this study, the thermal designer can improve the capacitor cooling solution by optimizing the boundary conditions.

Finally, the top case temperature  $(T_{top})$  was determined as the best measurement point to reflect the capacitor's internal temperature  $(T_{core})$ . Across the range of boundary conditions tested, the temperature difference between top and internal is constant and only around 1°C, so the system designer can easily convert the top case temperature to internal temperature, then perform electrolytic capacitor life time estimation referring to it.

#### Acknowledgements

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# Effect of Flow and Geometry Parameters on Performance of Solar Air Heater

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#### Abstract

Present paper deals with numerical investigation of solar air heater of a specific configuration where different geometrical parameters influencing its performance, is varied and its impact is assessed. The climatic conditions of Jeddah (lat. 21° 42′ N, 39° 11′ E), Saudi Arabia is considered for investigation. The numerical investigation is carried out using commercial CFD software i.e. ANSYS Fluent, as a tool of analysis. The effect of air mass flow rate, various selective coatings on the absorber plate, number of covers, spacing between the covers on the flowing air outlet temperature ( $T_{fo}$ ) and the heater instantaneous efficiency ( $\eta_{inst}$ ) are studied. The study also includes the effect of fins kept in the flow passage of heater. Investigation concludes that a better performance is expected using cobalt oxide (Co-O) as a selective coating material with a daily average of the instantaneous efficiency of about 56%. To ensure the correctness of numerical model the simulated result is validated with the analytical result that had been performed for the heater with a black painted absorber plate under the same climatic conditions.

#### 1 Introduction

Hot air has wide commercial and non-commercial application. Solar air heater ISHA) is one such promising device which is environment friendly and needs a sound design practices in its development. Several efforts have been made by researchers to improve thermal performance of solar air heater. Most of the works are either experimental or theoretical with a number of approximations. Goldstein [1] suggested that by increasing heat transfer coefficient and heat transfer area of the absorber plate, the performance of SAH can be improved. Lansing [2] recommended that the use of porous material inside the collector to enhance the efficiency. The effect of collector aspect ratio on the energy collection efficiency of flat-plate solar air heaters for a constant collector area and different flow rates was investigated theoretically and experimentally by Lin [3]. Yeh and Lin [4], and El-Sawi [5] experimentally studied the issues of lower heat transfer coefficient in flat plate SAH. Investigation of Alok et al. [6] concludes that the formation of viscous sub-layer and low heat capacity of air are responsible for lower heat transfer coefficient. To enhance the heat transfer coefficient in SAH several researchers used different kind of turbulent promoters such as use of fins attached over and below the absorber plate, recycling of the flowing air in double-path solar air heaters, using absorber plates with different types of roughness, using packed bed materials above or under the absorber plate, using absorber plates with V grooves etc. Saini and Verma [7] indicated that the heat transfer coefficient between the absorber plate and air can be considerably increased by using artificial roughness on the underside of the absorber plate. To compare the performance of three design of SAH with different number of glass covers, Martin and Fjeld [8] carried out an experimental investigation where operating

conditions were varied. It was found that the thermal trap collector have a higher operational efficiency than the other collector types and is capable of collecting solar energy for a longer period of time each day.

Investigation done by various researchers concludes that the performance of a SAH depends on a number of factor such as number of glass cover, spacing between glass covers, nature of selective coating, presence of fins, arrangement of fins, air flow rate etc. acting simultaneously. The review literature shows most of the work is either experimental or theoretical which are oriented to few factors only. So the present work intends to carry out a detailed numerical investigation under different key parameters of solar air heater. The study includes the assessment significant flow and geometrical parameters on a finite sized solar air heater. A double glass covered solar air heater of size 1000×1000×180 mm as shown in Fig. 1 is considered for the investigation. The air to be heated flows between absorber plate and the lower glass cover where it gains thermal energy from the absorber plate. Air exit temperature depends

on air mass flow rate; nature of selective coating, glass covers spacing, number of glass covers and fins and their pitch which are a part of present investigation. The objective of the work is to assess the effect of these parameters on SHA.



All dimensions are in mm

Figure 1: A schematic of physical domain of SHA

#### 2 Mathematical Model

The heat transfer process occurring in a solar heater can be mathematically model using appropriate radiation heat transfer model along with generic mass, momentum and energy equation. SAH is modelled as a transient open system with air as an ideal gas getting heated by solar radiation. The flow is driven by pressure gradient existing across the domain and buoyancy force induced by density variation. Viscous forces are negligible but considered in the analysis. There is no property change due to thermal effect. The solar radiation heat flux is assumed uniform over exposed area.

#### **Mass Balance Equation:**

$$div \, \boldsymbol{U} = \boldsymbol{0} \tag{1}$$

**Momentum Equation:** 

$$\frac{\partial U}{\partial t} + div(UU) = -\frac{1}{\rho}\frac{\partial p}{\partial x} + vdiv(grad(U))$$
(2)

$$\frac{\partial V}{\partial t} + div \left( V U \right) = -\frac{1}{\rho} \frac{\partial p}{\partial x} + v div \left( grad \left( V \right) \right)$$
(3)

$$\frac{\partial W}{\partial t} + div \left( WU \right) = -\frac{1}{\rho} \frac{\partial p}{\partial z} + v div \left( grad \left( W \right) \right)$$
(4)

where U, V and W are velocity components and p indicates local pressure. First terms of momentum equation does not indicate transient behavior of the system but they represents time based iteration required for converged solution.

Energy Equation:

$$\frac{\partial T}{\partial t} + div(TU) = \alpha \, div(grad(T)) + S_r \tag{5}$$

where  $\alpha$  and *T* represents thermal diffusivity and temperature. S<sub>r</sub> is radiation source term which is predicted by DO model of radiative heat transfer which takes care of radiation in semi-transparent media.

#### **3** Numerical Implementation

The investigation is carried out using ANSYS Fluent 13.0 as a solver which receive meshed model from ICEM. Mesh is generated using structured blocking algorithm. The solver is pressure based with steady operating condition where gravity effect is neglected. Different cell zone available in the computational domain is shown in table 1. The density, specific heat, thermal conductivity and viscosity of air are modelled respectively by incompressible ideal gas, piecewise polynomial, kinetic theory and Sutherland.

Table 3: Different cell zones

Sr. No.	Item	Zone	Material
1	Glass	Solid	Glass
2	Absorber plate	Solid	Galvanized-iron
3	Air	Liquid	Air

The properties used for glass are, density  $(2400 \text{ kg/m}^3)$ , specific heat (840 J/kg. K), thermal conductivity (1.05 W/m. K), refractive index (1.526), absorption coefficient (200). The absorber plate is made of galvanized iron which has density (7897 kg/m<sup>3</sup>), specific heat (452 J/kg. K), thermal conductivity (73W/m. K)

Boundary condition for the validation of numerical models is taken from El-Sebaii and Al-Snani [9]. Air enters at 313K temperature. The boundary condition used for investigation takes care of specific situation existing at the boundary which is as per the climatic condition of city Jeddah (lat 21° 42' N, Long. 39° 11' E), Saudi Arabia.

Inlet	: Mass flow inlet, 0.005 kg/s
Outlet	: Pressure Outlet, P <sub>atm</sub>
Walls	: Adiabatic and no slip
Top wall	: Radiation and convection

#### 4 Results and Discussion

The investigation of hydrodynamic and thermal behaviour of solar air heater of the present case is carried out under various parametric variations. After grid sensitivity test the validity of the numerical models is done by comparing the simulated result with the analytical result of El-Sebaii and Al-Snani [9]. Figure 2 shows the distribution of temperature of air moving in between absorber plate and glass cover.



Figure 2: Temperature distribution on a vertical plane

Solar radiation transmitted through glass cover and absorbed by absorber plate causes air temperature to rise due to convective and radiative mode of heat transfer. An assessment of different parameters on the performance of SHA is illustrated with analysis.

#### 4.1 Effect of air mass flow rate

To access the effect of air mass flow rate on performance of SAH, it is varied from 0.005kg/s to 0.00234kg/s at different time of the day. The variation is represented in Fig.3. On mid of the day solar flux between 11am to 2pm is high. This leads to higher air outlet average temperature. Lower mass flow rate gives better result.



Figure 3: Variation of air mass flow rate on the outlet temperature

#### 4.2 Effect of selective coatings

Selective coating plays a crucial element in performance of SAH. The use of black paint, Cu-O, Cr–Cr<sub>2</sub>O<sub>3</sub>, Ni–Sn and Co-O is investigated at air mass flow rate of 0.005kg/s. It cab observed in Fig. 4 that values of  $T_{fo}$  are considerably higher for all investigated selective materials compared to that when the black painted absorber is used. These is expected due to the increased amount of solar radiation absorbed by the selective materials (have high  $_p$  values) and the decreased rate of heat transfer by radiation from the absorber plate to the lower glass cover when the selective materials (have low  $_p$  values) are used.



Figure 4: Effect of selective coatings on air outlet temperature

#### 4.3 Effect of glass covers spacing

For the geometry of SHA under consideration the glass cover spacing is varied from 15mm to 55mm when air mass

flow rate is  $_{\rm f}$  =0.005 kg/s. A marginal increase in exit air temperature can be observed with increase in glass spacing which become stronger during mid day when solar heat flux



Figure 5: Effect of glass spacing on outlet temperature

is maximum. This can be attributed to increasing resistance to diffusive heat with larger glass cover spacing.

#### 4.3 Effect of number of glass covers

Three glass covers- single, double and triple, considered for investigation for air mass flow rate,  $_{\rm f}$  =0.005 kg/s and 15mm spacing in between glass cover. Figure 6 shows that two and three glass cover performs better compared to single glass cover.



Figure 6: Effect of glass covers on air outlet temperature

As the number of cover increases, the value of decreases. This leads to reduced heat absorption by the absorber plate. Addition covers decreases the convective heat losses from top sides. This effect can be observed in  $\eta_{inst}$  in the following Fig. 7.



Figure 7: Effect of number of glass covers on instantaneous efficiency

#### 4.3 Effect of fins and fin pitch

Using fins to enhance the heat transfer is a common technique. The effect of fins and the fin pitch (136.9 mm) on double glass covers black painted absorber plate with  $_{\rm f}$  = 0.005 kg/s is shown in Fig. 8 and 9 through velocity and temperature distribution.



Figure 8: Velocity contours along the length of the SAH



Figure 9: Temperature distribution on mid horizontal plane

The outlet temperature with different fin pitch spacing is shown in Fig.10.



Figure 10: Effect of fin pitch on outlet temperature

The presence of fin enhances the heat transfer. An arrangement without fin and with fins is depicted in Fig.10. This may be attributed to increased turbulence in flow due to obstruction produced by fins which leads to better mixing of air.

# 5 Conclusions

Present work successfully investigates the effect of different geometrical parameters on air temperature at the outlet using numerical tools. Some the significant outcome is as follows.

- The best performance is achieved using CoO as a selective coating material due to the decreased rate of heat losses and the increased rate of useful energy.
- Single cover collector is not efficient. High-temperature collectors should have more than one transparent cover. Two glass cover solar air heater system is preferable.
- By using the larger spacing between the glass covers, collector area requirements can be reduced by 2 to 8 per cent.
- The presence of fins in the absorber channel enhances the heat transfer ,ultimately it enhances the thermal performance

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# Mathematical Modelling of Coupled Heat and Mass Transport into an Electronic Enclosure

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#### Abstract

In contrast to high fidelity CFD codes which require higher computational effort/time, the well-known Resistor-Capacitor (RC) approach requires much lower calculation time, but also with a lower resolution of the geometrical arrangement. Therefore, for enclosures without too complex geometry in their interior, it is more efficient to use the RC method for thermal management and design of electronic compartments. Thus, the objective of this paper is to build an in-house code based on the RC approach for simulating coupled heat and mass transport into a (closed) electronic enclosure. The developed code has the capability of combining lumped components and a 1D description. Heat and mass transport is based on a FVM discretization of the heat conduction equation and Fick's second law. Simulation results are compared with corresponding experimental findings and good agreement is found. Second simulation was performed to study the response of temperature and moisture inside an enclosure exposed to the B2 STANAG climatic cyclic conditions.

#### **1** Introduction

The use of electronic devices in climatically harsh environment leads to moisture-related failures, mainly corrosion due to water layer formation as well as leakage currents, short or open circuits caused by electrochemical metal migration [1-5]. These are one of the most important issues found in outdoor electronics applications, e.g. automotive industry and renewable energy sectors. Hence, knowledge of moisture transport into an electronic enclosure under environmental conditions becomes interesting for increasing the reliability of electronic components and devices.

The designs of enclosures for electronics systems are often based on years of experience, rather than scientific knowledge. The main bottleneck is to break this trend and develop a set of more knowledge based modelling tools, which can further support the search for optimal designs and humidity control solutions. Since it is desirable to have fast modelling tools, the computational time is of utmost importance in the whole electronics design, especially in the early product development stage, where all possible design configurations have to be considered. While CFD or FEM are widely used and extremely useful tools in moisture modelling, these methods are too time consuming due to computational effort [6-7]. Therefore it is highly desirable to have a method which has less spatial resolution and would be faster and sufficiently accurate to calculate the moisture response in the electronic systems.

The aim of this paper is to build an in-house code based on the RC approach for simulating coupled heat and mass transport into a closed electronic enclosure under nonisothermal conditions. Then, based on the developed code, the amount of moisture and heat transported via diffusion and heat conduction through a wall into an enclosure will be predicted.

The paper covers an in-house code development based on the RC approach in which a 1D description is combined with a lumped component for describing a polycarbonate (PC) enclosure. The 1D description of heat and mass transport in the wall is based on an FVM discretization of both heat conduction equation and Fick's second law while the lumped capacitance component is used to describe the interior enclosure volume. Simulation results were compared with corresponding experimental findings and good agreement was found. After validation of the code, a second simulation was performed to assess the response of moisture and temperature inside a closed box to changes in B2 STANAG climatic cyclic conditions.

# 2 Moisture and temperature modelling via RC approach

This section outlines the development of an in-house code based on the RC approach for analyzing the response of moisture and temperature under non-isothermal conditions. Here, the RC approach is applied to solve heat and moisture transport based on heat conduction equation and Fick's second law [8-9].

The code is only developed to study a closed electronics box. In reality, the moisture and temperature inside a closed box of air reaches equilibrium relatively fast, therefore the convection is not considered in the code. Moreover, the following is assumed:

• The temperature is considered to be uniform on the outer and inner surface of box and in the air.

• The convection inside the cavity and in the ambient atmosphere is assumed to be sufficient to maintain spatially constant densities of water vapour in each of the two regions.

The next 2.1 subsection relates to the development of the RC model in more detail under the considered assumptions and applied equations.

#### 2.1 Thermal-moisture RC circuit

The closed electronics enclosure in Fig. 1 is used to model the response of moisture and temperature.

An in-house code was developed to combine lumped components (in this study the enclosure interior) and 1D description (here the enclosure walls). The 1D description of heat and mass transport in the wall is based on a FVM discretization of both heat conduction equation and Fick's second law.

Two separate RC circuits are implemented in the code. First, the moisture response inside the enclosure is simulated by using an equivalent circuit consisting of multiple resistors and capacitors (RC hygro-circuit) where the concentration in the air or in the wall is represented as voltage (Fig. 2) [7]. Second, the temperature response is simulated using the same or a different configuration RC circuit (RC thermo-circuit). The temperature is also represented as the voltage. The thermal and moisture resistances of discretized elements are expressed below:

$$R_{element,th} = d_e / DA$$
 and  $R_{element,moist} = d_e / kA$  (1)

The capacity for the moisture is equal to the actual volume of material ( $V_{wall}$  or  $V_{air}$  in Fig. 1) and the thermal capacity is given by the equation below:

$$C_{element,moist} = V$$
 and  $C_{element,th} = \rho c_p d_e A$  (2)

where D – diffusion coefficient for a given temperature, m<sup>2</sup>/s, A – surface area of element perpendicular to the flow of heat or moisture m<sup>2</sup>, d<sub>e</sub> – length of discretized element,  $\rho$  – density kg/m<sup>3</sup>, k – thermal conductivity W/(m·K),  $c_p$  – specific heat capacity J/(kg·K), V – volume kg.



Figure 1: Illustration of the investigated box



Figure 2: RC circuit for modelling temperature and moisture

Then, these two RC circuits are coupled where the thermal field and concentration distribution are coupled via the diffusion and solubility equations shown below [7-8]:

$$D(T) = D_0 e^{\left(\frac{-E_D}{RT}\right)} \tag{3}$$

$$S(T) = S_0 e^{\left(\frac{E_s}{RT}\right)} \tag{4}$$

where  $D_0$  – pre-exponential factor/coefficient,  $m^2/s$ , R – universal gas constant, J/(mol·K),  $E_D$  – activation energy for diffusivity, J/mol, T – temperature, K, S<sub>0</sub> – pre-exponential factor/coefficient, kg/(m<sup>3</sup>·Pa), J/(mol·K),  $E_S$  – activation energy for solubility, J/mol. Furthermore, the material's thermal conductivity is not dependent on the concentration in this study.

In this study, the wall of the box is discretized into three elements and the box interior is considered to be a lumped component (Fig. 2). Here, the same configuration is used for RC thermal and hygro circuits. The coupled thermo-hygrocircuit is solved implicitly (Backward Euler method) [9] in order to use an unconditionally stable scheme allowing for higher time increments. The boundary conditions are implemented as voltage source in the thermo-hygro-circuit.

# 2.2 Discontinuity at the environment and material interface

The concentration of water vapour is discontinuous at the environment-material or material-material interfaces (Fig. 3) [7, 10].



Figure 3: Water uptake into polymers and concentration discontinuity
The water vapour concentration represented by voltage in the RC circuit will be equal in all capacitors or nodes when equilibrium is reached in the diffusion process. Since, different materials have different solubility levels in the real conditions (Fig. 3), the RC hygro circuit has to be normalized using a reference material in order to avoid discontinuity. Therefore, an actual volume of each material is represented by the equivalent reference material volume which store the same amount of water vapour as each actual material. Such modification is broadly discussed in the paper [7]. Usually, the air is chosen as a reference material to normalize the RC hygro circuit.

Capacitance of actual volume is transformed to the equivalent air capacitance using equations below [7]:

$$V_{equivalent} = \frac{M_{water_{in_polymer}}}{c_{air_{sat}}} = \frac{S(T) \cdot p_{H_2O\_sat} \cdot V_{polymer}}{c_{air_{sat}}}$$
(5)

$$ratio_{conc} = S(T) \cdot p_{H_2O\_sat} / c_{air\_sat}$$
(6)

$$V_{equivalent} = V_{polymer} \cdot ratio_{conc} \tag{7}$$

where S(T) – temperature dependent solubility of water in polymer kg/(m3\*Pa),  $V_{polymer}$  – geometric volume of polymer [m<sup>3</sup>],  $V_{equivalent}$  - equivalent air volume for the transformed material [m<sup>3</sup>],  $p_{H20\_sat}$  – water vapour pressure at saturation point Pa,  $c_{air\_sat}$  - water vapour concentration in air at saturation point kg/m<sup>3</sup>,  $M_{water\_in\_polymer}$  – water vapour mass in polymer kg, ratio<sub>conc</sub> – transformation factor relating maximum solubility or water vapour concentration in the polymer and maximum water vapour concentration in air (reference material). Resistors representing diffusion need to be transformed, as well in order to avoid discontinuity [7]:

$$R_{diff\_equivalent} = d / (A \cdot D \cdot ratio_{conc})$$
(8)

After modification, the concentration gradient across the wall (see Fig. 3, bottom curve) is reduced with  $ratio_{conc}$  than the upper curve. Thus, the resistance has to be reduced as well, to gain the same amount of moisture penetrating a wall.

#### **3** Simulation results

#### 3.1 Validation of the in-house code

In order to validate the developed in-house code, the experimental results from Tencer [3] were chosen as validation case, see figure 10 a. A closed box with dimensions (590 mm x 190 mm x 125 mm) was used and the wall was made of polycarbonate material with thickness 6 mm. The box was exposed to environmental conditions of 25 °C and 98 % relative humidity (RH). The initial conditions for the interior were 25 °C and 19 % for the temperature and the relative humidity, respectively. The diffusion coefficient was  $8.06 \cdot 10^{-12}$  m<sup>2</sup>/s and the solubility –



2.78 kg/m<sup>3</sup>. The simulation and experimental results are

compared in Fig. 4.

Figure 4: Validation of simulation results vs. experiments for the interior RH [3]

The comparison showed that the results are in good alignment with the experiments.

# **3.2** Response of moisture and temperature to a changes in environmental cyclic conditions

After validating the developed code with experimental results, an oscillating boundary condition is implemented in the model in order to simulate real environmental conditions. Data for oscillating ambient temperature and relative humidity (RH) are taken from the well-known STANAG B2 climatic conditions (Fig. 5). The EKJB 130 T electronic box made of polycarbonate (PC) material is taken from Fibox with the dimensions of (280 mm x 190 mm x 130 mm).

Table 1: Properties of polycarbonate material

$D_0, m^2/s$	$1.36 \cdot 10^{-5}$
E <sub>D</sub> , J/mol	$36.5 \cdot 10^3$
$S_0$ , kg/(m <sup>3</sup> ·Pa)	$6 \cdot 10^{-10}$
E <sub>s</sub> , J/mol	$36.2 \cdot 10^3$



Figure 5: Boundary conditions taken from B2 STANAG climatic conditions

The initial conditions for the closed enclosure and interior air are 25 °C and 40 % for the temperature and the relative humidity, respectively. The material properties for moisture are described in table 1. Thermal conductivity (k) was 0.2 W/(m·K),  $\rho - 1200 \text{ kg/m}^3$ ,  $c_p - 1200 \text{ J/(kg·K)}$  [11].



Figure 6: Temperature response inside the box



Figure 7: Moisture response inside the box

The results show that the interior temperature inside the box follows almost identically the ambient temperature. However, the moisture response (RH) is slower and the RH magnitude increases exponentially until it reaches steady state conditions (almost after 24 days). This is expected, since the time constant for the thermal response is much smaller than that of the moisture response.

#### 4 Conclusions

- An in-house code was developed, with the flexibility of coupling different circuits for different physics under non-isothermal conditions. It is very fast, less spatial resolution and less time-consuming compared to commercial CFD codes. Moreover, this code will be further developed to include condensation and couple it with evaporation processes.
- The interior temperature responded very quickly to the ambient temperature due to the small thermal time constant. Moreover, depending on the size of the box and

the thickness of the walls, the latter can show a buffer effect in shorter periods.

• The moisture response inside the box is slower since the time constant for the mass transport is larger. As expected, the moisture response is increasing exponentially until it reaches steady state conditions. Moreover, peak-to-peak RH value is increasing, due to the increase of moisture content inside the box.

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# SIMULATION of the THERMAL BEHAVIOR of a CONDUCTIVE ADHESIVE

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#### Abstract

The conductive adhesive material studied is composed with spheres of a polymer core covered with a nanometric thickness of silver and embedded in a polymer matrix. As the spheres are covered with metal of high thermal conductivity, an easy model has been developed based on the thermal resistance network method. Results have been compared with finite element method (FEM) simulations; only for cylinders – i.e. for a 2D problem - from now. The difference induced by the easy modelling compared to FEM simulation is less than 10%. Five different configurations of cylinder arrangement within the matrix were studied. Results have shown that the cylinder configuration is a key parameter to determine the thermal properties of the adhesive.

#### 1 Introduction and context

Electrically conductive adhesives represent an environmental friendly alternative to conventional soldering technology in a variety of electronic applications, eliminating the use of lead and flux cleaning. Other advantages are lower processing temperatures, fewer processing steps, reduced cost and fine pitch capability. However, lower electrical and thermal conductivity represent a limitation in the use of electrically conductive adhesives compared to that of solder. Typically, electrically conductive adhesives consist of an adhesive matrix filled with electrically conductive particles.

We will focus here on an Isotropic Conductive Adhesive (ICA) where the concentration of particles is high and the large degree of inter-particle contacts makes the adhesive electrically conductive in all directions. This ICA utilizes metallized-plated polymer spheres (MPS) as conductive fillers instead of solid metal particles.

Like all materials designed for heat transfer, they need thermal characterization. For ICA, the question of the variability of their thermal characteristic among the configuration taken by the spheres is not clear and must be investigated. This is the aim of this first step concerning a 2D model of parallel cylinders, mechanically in contact, before studying the 3D model with spheres.

The heat conduction in different kinds of solids has already been studied for plain and hollow solids [1] [2] [3] [4], but always with boundary conditions at the pole of the solids. The interstitial matter in between the solids has also been taken into account to estimate the heat flux [5].

Recently, the configuration – i.e. the arrangement of the different solids in space – was studied in a thermal model of the third body in tribology [6] for an unsteady problem, but only for two fixed configurations (cases I and III given in the following).

Nevertheless, it is possible to model the heat conduction in some other configurations with an easy thermal model to

estimate the thermal properties of ICA and to validate the methodology with a classical finite element method (FEM).

#### 2 Description of the adhesive

The composite material (see Fig. 1) is composed with polymeric spheres of radius  $r = 15 \ \mu\text{m}$ . The thickness of the silver film covering these spheres is  $e = 150 \ \text{nm}$ .

We have considered the bulk thermal conductivity  $\lambda_s$ =430 W.m<sup>-1</sup>.K<sup>-1</sup>. Spheres are embedded in a polymer matrix (epoxy) of thermal conductivity  $\lambda_p$ =0.1 W.m<sup>-1</sup>.K<sup>-1</sup>.



Figure 1: Scanning Electron Microscopy image of cross-sectioned ICA sample containing a volume fraction of 56% AgPS. PMMA particles (light grey) with a diameter of 30 µm are coated here with 270 nm thick silver films (white) and embedded in an epoxy matrix (dark grey). The seemly large size distribution is a result of the cross-section cutting through different planes in the randomly dispersed particles [7]. This material is currently developed and improved in the framework of the QUANTIHEAT project. It also constitutes a test material used to compare various thermal characterization tools.

#### **3** Thermal model of the adhesives

The first step of this development has concerned the 2D thermal problem so that we have studied only cylinders from now. All the definitions (heat flux, thermal resistance) referred to an arbitrary depth within a thick adhesive layer.

The adhesive layer is supposed to be semi-infinite. The thermal model has been used to study of the symmetries and the invariances by translation.

A temperature difference  $\Delta T$  is applied on the top and the bottom of the adhesive. The heat flux Q (see Fig. 2) was calculated to obtain the effective thermal resistance  $R_{th}$  of the adhesive layer:

$$R_{th} = \frac{\Delta T}{\dot{Q}} \tag{1}$$

The length *l* and the height *h* of the studied volume are useful to calculate the effective thermal conductivity  $\lambda_{eff}$  of the composite material:

$$\lambda_{eff} = \frac{h}{R_{th}l} \tag{2}$$

The volume fraction of silver was calculated from the volume of silver  $V_s$  and the total volume of the simulation volume  $V_{tot}$ :

$$x = \frac{V_s}{V_{tot}}$$
(3)



Figure 2: Thermal boundary conditions applied to calculate the thermal resistance of the composite adhesive material.

Among all the configurations of cylinder arrangement possible, the five configurations presented in Fig. 3 were considered. For each case, the elementary structure is either a equilateral triangle, either a rhombus, or a square. The first configuration, called case I, is a vertical stacking of cylinders. The third one is a staggering of cylinders, as the fifth one, but the orientation of the elementary triangle is not the same. Configurations II and IV are intermediate configurations between the configurations I, III and V. They are parameterised by an angle  $\theta$  that is between  $\pi/3$  (case III) and  $\pi/2$  (case I) for the case II and between  $\pi/3$  (case V) and  $2\pi/3$  (case III) for the case IV.

If the contact size is small compared to the other lengths of the problem, the thermal resistance of a cylinder in which the heat flux goes through between two physical points separated by an angle  $\theta$  (see Fig. 4) is:

$$R_{\theta} = \frac{r\theta}{\lambda_{s} e} \tag{4}$$

The contacts between cylinders are here considered as perfect contacts, i.e. the thermal contact resistance is null, but it can be easily added in the thermal resistance network.

Thus, this model is based on a thermal resistance network method (TRNM) that can be solved directly by assembling thermal resistances (see Fig. 5). For more complex cases, with thermal contact resistances, the need of the resolution of linear system through matrix inversion, with free software like Scilab for instance should be required.



Figure 3: The five configurations studied.



Figure 4: Definition of the thermal resistance of a part of cylinder.



*Figure 5: Thermal resistance model method applied on the configuration IV.* 

#### 4 Finite element method

The first model based on thermal resistance network neglects the heat flux by conduction in the polymer, either in the epoxy matrix or in the core of the spheres. Nevertheless, the thickness of the silver layer may be sufficiently thin to reach a high thermal resistance in the silver layer.

In order to validate this assumption, a model based on finite element method, taking into account the polymer, was developed with Comsol Multiphysics<sup>®</sup>. Four of the configurations given in Fig. 3 were simulated: cases I, III, IV and V.

The thermal conductivity of the polymer in the matrix and in the core of the spheres was fixed at 0.1 W.m<sup>-1</sup>.K<sup>-1</sup> which is a classical value for polymers.

The thermal contacts between cylinders and between top and bottom cylinders and the boundary limits were ensured with small rectangles of 750 nm length (see Fig. 6) in order to avoid punctual contacts that cause simulation problems when the polymer was removed for test simulations.

### 5 Results

The thermal conductivity versus the volume fraction of silver gives the most significant conclusions (see Fig. 7).

First, the effective conductivity of the adhesive composed by the same number of cylinder slices varies between  $1.9 \text{ W.m}^{-1}.\text{K}^{-1}$  to  $3.4 \text{ W.m}^{-1}.\text{K}^{-1}$  while the volume fraction varies from 1.4% to 1.8%. For the same volume fraction of silver, the thermal conductivity is very dependent on the arrangement of the cylinders.



*Figure 6: Detail of the mesh describing the silver layer, the polymer and the contact at the top of the cylinder.* 

The FEM simulations have confirmed these primary results obtained with the easy thermal resistance model. The TRNM underestimates the effective thermal conductivity for *all* the configurations. The shift is about 0.2 W.m<sup>-1</sup>.K<sup>-1</sup> for the thermal conductivity and -0.008 % for the volume fraction for all configurations. This shift can be explained by the heat conduction in the polymer (matrix and core) and by the reduction of the length of silver in which the heat is transferred due to the contact conditions.

For example for the case I the effective thermal conductivity in the FEM simulation is 2.95  $W.m^{-1}.K^{-1}$  with polymer and 2.8  $W.m^{-1}.K^{-1}$  without polymer, whereas it is 2.74  $W.m^{-1}.K^{-1}$ for TRNM and reaches 2.78  $W.m^{-1}.K^{-1}$  by reducing the path for heat conduction.

These two values are close enough to explain the difference between the two methods. It is possible to conclude that 2/3 of the shift is explained by the heat conduction in the polymer and 1/3 by the different contact conditions. To explain the shift on the volume fraction, the thickness of the silver has not been taken into account in  $V_{tot}$  for the easy model.



Figure 7: Thermal conductivity versus volume fraction of silver for the five configurations.

The highest value of effective thermal conductivity is reached with the case III according to Fig. 7. However, another interpretation can be suggested if we consider that, for industrial needs, only the global thermal effective resistance and the silver mass for an arbitrary surface are relevant. Those two specifications lead to compare the thermal resistance for a same surface of component, so the product  $R_{th}$  *l* and the total mass of silver, proportional to *x h* (see Fig. 8). With these specifications, the case III consuming more silver than the case V, for the same level of thermal effective resistance, even if the thermal contacts with boundaries are not efficient in the case V.

Furthermore, the trend of the case IV has to be explained: for two different configurations with the same volume fraction of silver, the values of the effective thermal conductivity are different. In these two cases, the basic element which is a rhombus is not oriented towards the same direction and one of these directions is more efficient than the other. For a volume fraction *x* equal to 1.45%, the effective thermal conductivity is equal to 2 W.m<sup>-1</sup>.K<sup>-1</sup> or 2.5 W.m<sup>-1</sup>.K<sup>-1</sup>.

Some first thermal characterizations were proceeded [7] on this adhesive for volume fractions between 2.5 and 4.5%. The effective thermal conductivity measured was around 0.3 and 1.2 W.m<sup>-1</sup>.K<sup>-1</sup> which is a bit lower than our results.

The model with spheres instead of cylinders should improve the model.

The classical Maxwell Garnett effective thermal conductivity for silver flakes in polymer matrix:

$$\lambda_{MG} = \frac{x \left(\lambda_s - \lambda_{po}\right)}{\lambda_s + 2 \lambda_{po}} \tag{5}$$

gives a result depending on the volume fraction x around 0.105 W.m<sup>-1</sup>.K<sup>-1</sup>, near the value of the thermal conductivity of the polymer. The effective thermal conductivity obtained with our model is 30 times bigger than the thermal conductivity of the polymer matrix (and the Maxwell Garnett thermal conductivity).

#### **6** Conclusions and perspectives

The model based on TRNM, compared to FEM model gives good results and is easy to use. The difference between the two models is explained by the heat flux through the polymer and the contact boundary conditions.

This easy model confirms that the effective thermal conductivity of ICA is 30 times bigger than the epoxy matrix thermal conductivity for a volume fraction of silver less than 2%. The effective thermal conductivity of ICA is very dependent on the arrangement of the cylinders covered by silver layer in the epoxy matrix, varying from  $1.9 \text{ W.m}^{-1}$ .K<sup>-1</sup> to 3.4 W.m<sup>-1</sup>.K<sup>-1</sup> for 4 slices of cylinders.

Even if the thermal properties of ICA will not be easy to tailor by controlling the arrangement of the cylinders, the knowledge of their structure inside the epoxy matrix by another kind of analysis would be key information to validate thermal characterizations of ICA. To go further, this first thermal model leads us to develop a 3D model for various configurations of hollow spheres.



Figure 8: Thermal performances of ICA. " $R_{th}$  I" is the thermal resistance for any kind of length of adhesive and "x h" is proportional to the mass of silver included in the adhesive.

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### **Modelling of Thermal Processes in Heat Flux Sensors**

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#### Abstract

The method of modelling the temperature and heat flux distribution in the structure consisting of the heat flux sensor and the object with the investigated heat flux is presented. In the structure, the domain of modelling is marked out and is replaced by the equivalent structure with three rectangular regions. For each region, the analytical expression for the temperature distribution is determined using the eigenfunction method. Heat flux densities on boundaries of regions are defined as the sums of orthogonal functions with unknown weighting coefficients. To find the unknown weighting coefficients the boundary conditions on boundaries of the regions are used. In general, the determination of the weighting coefficients is reduced to solving a system of linear equations. The present method is applied to determine the temperature distribution in the structure with the heat flux sensor and the thermally conductive wall and the heat flux densities on their surfaces.

#### 1 Introduction

The control of thermal processes in various objects requires the knowledge of the temperature distribution and heat fluxes in them. The heat fluxes characterise thermal transfers through a surface by conduction, convection and radiation and provide additional information to the temperature measurement. Presently, for measuring heat fluxes the various types of sensors are used [1-6]. Among these sensors the heat flux sensors based on thermopiles are more widely used [1]. For optimum design of these sensors and their correct application is necessary to know the features of thermal processes in them. Experimental investigation of these processes in operating heat flux sensors is very difficult task. The only possible way to solve this problem is using the mathematical modelling to analyze thermal processes in the structure with the sensor and the object under study. The aim of this paper is to present the analytical method allowing one to conduct an analysis of thermal processes in the heat flux sensor when they function. This analysis makes it possible to determine the characteristics of the sensors.

#### 2 Model

The schematic of using the heat flux sensor for measurement of the heat flux density in the object under study is presented on Fig. 1a.The object is the thermally conductive wall with the certain thickness and the length and width much larger than that of the sensor. The sensor is placed on the object and the measured heat flux flows through it. In fact, the measured heat flux is not equal to the actual heat flux flowing through the object due to the influence of the sensor. To estimate this influence and to determine the measuring error it is necessary to have data about the temperature distribution and the heat flux densities in the structure of the sensor and the object under investigation.



Figure 1: Schematic of using the heat flux sensor in a measurement and the equivalent structure for modelling: 1 - the heat flux sensor; 2 - the object under study

For finding the temperature distribution in the structure with the sensor and the object under study and heat flux densities on their surfaces, the analytical method was used which has been presented in [7]. In the structure of the sensor and the object one should mark out the domain of the modelling. This domain consists of the sensor and the section of the object the length of which is equal to ten length of the sensor. Taken into account the mirror symmetry of this structure the domain of modelling is reduced to its half, for example, to right part (Fig 1b). In modelling this domain should be divided into three rectangular regions depending on the boundary conditions and the thermal parameters of the components: region of the sensor and two regions of the wall.The equivalent structure of the domain of modelling is shown on Fig. 1c.

In accordance with [7] the stationary heat deferential equation for each region can be presented in the following form

$$\frac{\partial^2 T_j}{\partial x_j^2} + \frac{\partial^2 T_j}{\partial y_j^2} = 0, \qquad (1)$$

where  $T_j$  is the temperature of the region j;  $x_j$  and  $y_j$  are the coordinates of the region j. Using the Neumann boundary conditions on the boundaries of each regions one can obtain the temperature distribution in them. In general the temperature distribution in each region can be written as follows [7]

$$T_{j} = D_{0,0}^{(j)} + 2\sum_{k=1}^{\infty} D_{k,0}^{(j)} \cos(k\pi x_{j}/l_{j}) + 2\sum_{m=1}^{\infty} D_{0,m}^{(j)} \cos(m\pi y_{j}/b_{j}) + (2) + \frac{4}{l_{j}b_{j}\lambda_{j}} \sum_{k=1}^{\infty} \sum_{m=1}^{\infty} D_{k,m}^{(j)} \cos(k\pi x_{j}/l_{j}) \cos(m\pi y_{j}/b_{j}),$$

where

$$D_{k,m}^{(j)} = \frac{-(-1)^k \delta_m^{(j,s)} - (-1)^m \delta_k^{(j,t)} + \delta_m^{(j,u)} + \delta_k^{(j,v)}}{l_j b_j \lambda_j [(k\pi/l_j)^2 + (m\pi/b_j)^2]}; \quad (3)$$

 $l_j$ ,  $b_j$  are the length and width of the region j;  $\lambda_j$  is the thermal conductivity of the region j;  $\delta_m^{(j,s)}$ ,  $\delta_k^{(j,t)}$ ,  $\delta_m^{(j,u)}$ ,  $\delta_k^{(j,v)}$  are the weighting coefficients determining the heat flux densities on the boundaries between region j and regions s, t, u, and v respectively; k, m are the summation indices on x and y coordinates, respectively. The regions s, t, u, and v are located, respectively, right, above, left and below the region j.

The expressions for the temperature distribution in the regions contain the unknown weighting coefficients,  $\delta_m^{(j,s)}$ ,  $\delta_k^{(j,t)}$ ,  $\delta_m^{(j,u)}$ , and  $\delta_k^{(j,v)}$ , which characterize the heat flux densities on the boundaries of the regions. The values of

these coefficients can be determined with using the following boundary conditions

$$q^{(0,e1)} = h(T_0\big|_{x_0 = l_0} - T_e); \qquad (4)$$

$$q^{(0,e_2)} = h(T_0\big|_{y_0 = b_0} - T);$$
<sup>(5)</sup>

$$T_0\big|_{y_0=0} = T_1\big|_{y_1=b_1};$$
(6)

$$T_1\Big|_{x_1=l_1} = T_2\Big|_{x_2=0};$$
(7)

$$q^{(2,e3)} = h(T_2|_{y_2 = b_2} - T_e); \qquad (8)$$

$$T_1\Big|_{x_1=0} = T_w; (9)$$

$$T_2\Big|_{x_2=0} = T_{\rm w}\,,\tag{10}$$

where *h* is the convective heat transfer coefficient;  $T_{\rm w}$  is the temperature of the lower surface wall;  $T_{\rm e}$  is the environment temperature near the upper surface wall.

Using the boundary conditions (4)-(10) one can obtain the generalized system of linear equations for the unknown weighting coefficients in a matrix representation

$$\boldsymbol{M}\boldsymbol{\Delta} = \boldsymbol{\Phi} \;, \tag{11}$$

where M is the matrix of the coefficients;  $\Delta$  is the vector of the unknown weighting coefficients;  $\boldsymbol{\Phi}$  is the vector of the right parts. The designation of the matrix and the vectors in (11) is given in [7]. Solving the system (11) allows one to find the values of the all weighting coefficients.

#### **3** Results

The method was used to analyze the thermal processes in the structure consisting of the heat flux sensor and the object through which the measured heat flux flows. The object was the thermally conductive wall with the following parameters: thickness – 60 mm; thermal conductivity – 0.81 W/(m·K). The shape of the heat flux sensor was chosen to be square. The parameters of the heat flux sensor had the following values: the length of the square side – 50 mm; thickness – 2.5 mm; thermal conductivity – 5 W/(m·K). The other parameters were assumed to be: the temperature of the lower surface wall – 25  $^{\circ}$ C; the environment temperature – 15  $^{\circ}$ C; convective heat transfer coefficient – 50 W/(m<sup>2</sup>·K).

Fig. 2 shows the temperature distribution in the structure under consideration. The non-uniform temperature distribution occurs in the heat flux sensor. This is due to taking into account in the model the convective heat transfer through the lateral surface of the sensor. Fig 3 presents the temperature distribution along the upper surfaces of the heat flux sensor and the wall. Fig. 4 shows heat flux density along

the upper surfaces of the heat flux sensor and the wall. This dependences allows one to see the difference between the temperatures of the upper surfaces of the sensor and the wall and between the heat flux densities on these surfaces.

At using a heat flux sensor based on a thermopile and using spatial temperature difference method, the important factor is the difference between temperatures on the lower and upper surfaces of the sensor [1]. An output signal of the sensor is proportional to this temperature difference

$$\Delta E = \alpha N \left( T_{\rm l} - T_{\rm u} \right), \tag{12}$$

where  $\Delta E$  is the output signal of the sensor;  $\alpha$  is the Seebeck coefficient of thermocouples constituting the thermopile; N is the number of thermocouple pairs in the thermopile;  $T_1$  and  $T_u$  are the temperature of the lower and upper surfaces of the sensor, respectively. Using the measured output signal of the sensor and knowing its thickness (d) and thermal conductivity ( $\lambda$ ) one can determine the heat flux density ( $q_s$ ) in the system of the sensor and the wall.

$$q_{\rm s} = \lambda \left( T_{\rm l} - T_{\rm u} \right) / d = \lambda \Delta E / d\alpha N , \qquad (13)$$

According (12) and (13), in designing a heat flux sensor, it is important to locate the thermocouples in the regions where the difference between temperatures on the lower and upper surfaces is identical. For the variant considered in this paper, the difference between temperatures on the lower and upper surfaces of the sensor along the sensor is shown in Fig. 5. This presented data allows one to determine the section of the sensor where the above-mentioned difference is constant and where one should locate the thermocouples of the sensor.

It is worthwile to compare the heat flux densities in the sensor obtained by two ways: 1) the direct modelling with using the presented method; 2) the calculation with using (13) where the values of the temperatures are found also with the help of the presented method. The changes of said heat flux densities along the sensor are presented in Fig. 6. As can be seen from the presented data the proximity between the two heat flux densities is observed in the inner area of the sensor.



Figure 2: Temperature distribution in the structure of the heat flux sensor and the wall

### 4 Conclusion

The presented method allows one to analytically analyze thermal processes in the structure consisting of the heat flux sensor and the object with the investigated heat flux providing the sensor is located on the object surface. Heat transfer through object surfaces can be convective and/or conductive. This method can be used in designing heat flux sensors to determine their parameters and to choose the optimum design variant. It is also promising to use this method in operating heat flux sensors to determine a measurement error and its dependence on parameters of the object under study and measurement conditions.

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*Figure 3: Temperature distribution along the upper surfaces of the heat flux sensor and the wall* 



Figure 4: Heat flux density along the upper surfaces of the heat flux sensor and the wall



Figure 5: Difference between the temperatures on the lower and upper surfaces of the heat flux sensor



Figure 6: 1 – heat flux density on the upper surface of the sensor determined by modelling; 2 – heat flux density calculated through the difference between the temperatures on the lower and upper surfaces of the sensor

# Fabrication, Performance and Reliability of a Thermally Enhanced Wafer Level Fan Out Demonstrator with Integrated Heatsink

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#### Abstract

The leading Fan-Out Wafer-Level Packaging technology, WLFO by NANIUM, stemmed from Infineon's embedded Wafer-Level BGA (eWLB) technology, has limited heat dissipation capability, as the materials used in, namely the epoxy mold compound (EMC), originally aimed process ability and mechanical stability, but not heat conduction. As WLFO technology expands to WLSiP (Wafer-Level System-in-Package) for very high-density system integration, the thermal performance becomes a critical factor. In a broader scope, improving heat dissipation capabilities opens WLFO technology platform to power applications.

The main challenge for power dissipation on WLSiP packaging is that the EMC must be electrical insulator, placing challenges on both heat conduction and bonding to metallic heat spreader. Whereas mold compounds are typically organic resins filled with inorganic fillers, high performance thermal interface material (TIM) are designed for metal-metal interfaces, not for organic-metal interface as required for chip backside overmolded WLFO package. Another challenge is the assembly of an integrated heatsink, over and larger than the package, on a volume manufacturing capable process, to yield both good thermal conduction and reliable thermomechanical bonding.

The work done is part of the collaborative European FP7-ICT project NANOTHERM (Innovative Nano and Micro Technologies for Advanced Thermo and Mechanical Interfaces), together with a consortium of leading IDM, OEM, OSAT, material suppliers and academic/institutes.

#### **1** Introduction and Background

Wafer Level Fan-Out Packaging (WLFO) at Nanium stems from Infineon's eWLB technology [1][2]. While eWLB, in its genesis, was focused on single die, low power applications, WLFO rapidly expanded into a multi-chip, multi-component WLP technology, enabling Wafer Level System-in-Package (WLSiP), where the increase on power density placed a concern on thermal performance, due to the poor heat conductivity of the mold compound (MC).

In some special single-chip, high power products, the package backside is grinded to exposed the chip and a metallic heatsink (HS) is attached to the package back side with an appropriate Si-to-Metal Thermal Interface Material (TIM) adhesive. This method has the advantage of providing a direct heat path from chip to heatsink, therefore an optimal heat dissipation, while using the existing WLFO processes and materials. The limitation is that chip and HS are connected electrically because good heat conductive adhesives are generally also electrical conductors. Such chip-HS electrical connection is sometimes allowed, but often forbidden. Moreover, for two or more chips, this method implies all chips at the same electrical potential. In a generic SiP, with relevant heat dissipation needs, the above solution of exposing inner components by grinding becomes prohibitive or, at least, very restrictive, even defeating the purpose of having an electrically isolated system in a single package. Therefore, it is necessary to close the gap between high power density packages and WLSiP solutions on WLFO technology.

The aim of this work, show in Figure 1, is a **Power-FanOut** demonstrator, combining SiP and Power, with improved thermal performance and proven thermomechanical reliability.

In a previous work by the authors [3], the thermal performance characterization of typical Fan Out packages and the gains achieved with a thermally improved mold compound (MC) were presented. Figure 2 summarizes this data, as well as the impact of over-mold gap (OM). In the same work, a solution for the thermal and mechanical bonding of the heatsink was shown. The mold compound surface metallization with a standard Ti-Cu sputtering successfully solved the organic-to-metal bonding barrier and allowed the use of highly conductive Sintered Silver Adhesives (SSA) to integrate a Cu heatsink (HS) on the Fan Out package. The present work proceeds on the implementation of those solution and demonstrates the thermal performance gains and reliability results.

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Figure 1 - Power-FO goal, combining Power and WLSiP.



Figure 2 – Thermal characterization and improvement of Fan-Out package, summarized from [3]

#### 2 Demonstrator

The demonstrator's stack-up, from RDL to HS is shown in Figure 3. The MC metallization and TIM/SSA, for the bonding of the HS to the Fan-Out package, are indicated. Two SiP constructions were done: "A/B", with 48 independent diodes, occupying ~45% of package area, for multi pattern heating; and "C", with a series of 11 Ni Resistors and one diode per package quarter, occupying ~25% of package area, for independent quadrant heating.



**Figure 3** – Power-FO demonstrator stack up (top) and the two embedded component variants, A/B and C.

#### 2.1 Build-Up and Test Matrix

In addition to the two embedding component versions, other variants were introduced. These variants are described in Figure 4, as well the different thermal performance and reliability tests.

- MC1 (std) introduced as reference for MC2 gains and to assess HS-MC1 as intermediate solution;
- MC metallization: Ti (in fact TiO2) and TiCu-Ni; Ti as "Low Cost" variant; TiCuNi to use known TIM-Ni good adhesion quality and to match HS plating;
- TIMx and TIMz two types of SSA for selection;
- SiP construction A, B and C to rows A), B) and C) of test board (A and B: different board routing; C to exercise independent quadrant heating);
- Columns with and without heatsink, to assess contribution of MC and HS to thermal performance.

For Thermal performance test, only two configuration were selected: i) standard MC1 for baseline comparison; and ii) MC2-TIMx-Ni, as it is not expected any significant difference in the thermal resistance of TIMs and metallization. Also, boards included units with and without heatsink, in order to evaluate the isolated effect of MC.

For the Thermo-Mechanical Reliability tests, all 5 configurations were carried on, all units with heatsink. Soaking/MSL1, Drop Test (30x) and Thermal Cycling (1000x) [-25/100°C] (1 cycle/h, TC2, IPC9701) were performed to assess the HS bonding reliability. [-25/100°C] span was chosen in consistency with heatsink applications, i.e., to narrow the device's temperature operation range.



Boards for Thermo-Mech Reliability – All units with heatsink

Figure 4– Board assembly of Demonstrator and test matrix

#### 2.2 Demonstrator Construction Flow

One of the challenges of the demonstrator was the assembly of an integrated heatsink, *over and larger* than the package, on a volume manufacturing capable process.

For the case of a heatsink smaller than package, the assembly flow would be "*HS-on-Pkg*", easily done at wafer level. After RDL, the wafer is metallized on the backside via sputtering, then SSA adhesive is printed over the metallized wafer backside (e.g., via stencil printing) and the heatsinks placed with standard Pick&Place equipment. The adhesive curing is done at wafer level, followed by package singulation, with no mechanical conflict with the heatsink. However, heatsink smaller than package, arguably, does not make the best use of the ability to extend the dissipation area beyond the package, so it is not the target in this work.

**Heatsink larger than package** is a more challenging case, thus envisioned to the Demonstrator. Figure 5 shows the devised "*HS-on-Pkg*" process, capable for volume production and using existing equipment at Nanium. The build-up of the WLFO is shown at the top, with the new wafer backside metallization, after RDL process. The HS assembly process uses a thermal release tape, standard on compress molding process, which holds a matrix of heatsinks until TIM curing, whose temperature causes the tape to loose adhesion and releases the Power FO units to the next steps.



**Figure 5** – Assembly flow overview from FOWLP to test board, with focus on the Pkg-on-Heatsink integration process

The automated processes for adhesive dispensing, with volumetric control, and for P&P of WLFO SiP units over the adhesive, with controlled force and time, are crucial to guarantee a uniform Bond Line Thickness (BLT) across the package area, above a min limit 40um, which are important factors for HS bonding reliability, as demonstrated in [3].

#### **3** Thermal Performance

#### 3.1 Surface Temperature Measurement Method

For the thermal performance measurements of the different variants, the surface temperature profile along the diagonals of the excited unit was measured by IR thermography, on a FLIR P65 camera, Figure 6. The chamber environment is controlled at  $\sim$ 25°C, and the reflections inside the chamber are minimized by the tilted camera view and by the anti-reflective coating.



Figure 6 – Surface temperature measurement with IR.

#### 3.2 Temperature Resistance Measurements

Table 1 shows the Case-to-Ambient thermal resistance values calculated on configuration "C" units, for MC1 and MC2, with and without heatsink, and for both diagonal (2-quadrant) and homogeneous (4-quadrant) excitation cases. The temperature profiles along the diagonals were measured at steady-state conditions and the maximum  $\Delta T$  from the surface (either MC or HS) to the ambient was read.

<b>TADIE I</b> – Summary of results from the merinal measurements	Table 1 –	Summarv	of results	from IR	thermal	measurements
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		М	C1	MC2	
		2-quad	4-quad	2-quad	4-quad
No heatsink	Pwr [W]	1.25	2.88	1.40	2.58
	∆ <sub>T</sub> [ºC]	43.1	69.1	43.2	62.8
	$\Theta_{CA}[K/W]$	34.5	24.0	30.8	24.3
W/ Heatsink	Pwr [W]	1.21	3.65	1.40	3.65
	∆ <sub>T</sub> [ºC]	25.0	74.7	28.9	75.7
	Θ <sub>CA</sub> [K/W]	20.7	20.5	20.6	20.7

The Case-to-Ambient thermal resistance on the table,  $\Theta_{CA}$ , is calculated as the ratio of  $\Delta T$  to the Power excitation value. As explained in the next section,  $\Theta_{CA}$  encompasses both thermal paths to air and thru PCB.

The Junction-to-Case resistance,  $\theta_{J-C}$ , is not measured in this work, as it has been characterized in [3] and can be inferred from Figure 2. Nevertheless,  $\theta_{J-C}$  is much smaller than  $\Theta_{CA}$ , especially for the case of MC2 (<1K/W, for a typical ~50% Si occupation ratio), so the error introduced in the calculations by any inaccuracy on  $\theta_{J-C}$  is negligible. Also, for the temperature measurements over HS, the thermal resistance between package surface (MC) and the HS can be ignored: for a <50um BLT,  $\lambda$ >30W/m.K, over 64mm<sup>2</sup> of package area, the TIM adds only <0.03K/W to  $\theta_{J-C}$ .

#### 3.3 Simplified Thermal Model

Figure 7 shows the thermal model of the Demonstrator and its simplification to the two-series of *Junction-to-Case* and *Case-to-Ambient* thermal resistance.



Figure 7 - Simplification of Demonstrator's thermal model

The model starts by describing  $\theta_{J-C}+\theta_{C-Air}$  for the heat dissipation path to air  $(Q_A)$  and  $\theta_{J-Base}$  (= $\theta_{J-Pcb}+\theta_{Pcb-Base}$ ) for the heat dissipation path to PCB and cold plate base  $(Q_B)$ . Air and Base are at the same temperature (Figure 6), set as *Ambient Temperature*.  $\theta_{J-Amb}$  is calculated as:

$$\theta_{J-Amb} = \frac{(\theta_{J-C} + \theta_{C-Air}) \cdot \theta_{J-B}}{\theta_{J-C} + \theta_{C-Air} + \theta_{J-B}}$$
(1)

While the dissipated heat Q is the total *Power* fed to the set of dies and diodes, represented globally as *Junction*, the temperature is measured not at the *Junction*, but rather at the "*Case*", i.e., either at MC body or heatsink. Therefore, the  $\Delta T_C/Q$  ratio in Table 1 must be equated and interpreted:

$$Q = Q_A + Q_B = \frac{\Delta T_C}{\theta_{C-Air}} + \frac{\Delta T_C}{\theta_{J-B}} \cdot \frac{\theta_{J-C} + \theta_{C-Air}}{\theta_{C-Air}}$$
(2)

with 
$$\Delta T_C \cdot \frac{\theta_{J-C} + \theta_{C-Air}}{\theta_{C-Air}} = \Delta T_J$$
 (3)

$$Q = \frac{\Delta T_C}{\theta_{C-Air}} \cdot \left(\frac{\theta_{J-B} + \theta_{J-C} + \theta_{C-Air}}{\theta_{J-B}}\right)$$
(4)

Considering that  $\theta_{J-C} \ll (\theta_{C-Air} + \theta_{J-Base})$ , about two orders of magnitude smaller,  $\Delta T_C/Q$  represents the thermal resistance of parallel paths to ambient (to air and thru PCB), i.e.,  $\Theta_{CA}$ :

$$\frac{\Delta T_C}{Q} = \frac{\theta_{C-Air} \cdot \theta_{J-B}}{\theta_{J-C} + \theta_{C-Air} + \theta_{J-B}} \cong \frac{\theta_{C-Air} \cdot \theta_{J-B}}{\theta_{C-Air} + \theta_{J-B}}$$
(5)

$$\frac{\Delta T_C}{Q} \cong \theta_{C-Air} / / \theta_{J-B} = \theta_{C-Amb} \text{ or } \Box_{CA}$$
(6)

Equation (1) can be decomposed in a sum of equation (5), to evidence  $\Delta T_C/Q$ , and a weighted term of  $\theta_{J-C}$  (8):

$$\theta_{J-Amb} = \theta_{J-C} \cdot \frac{\theta_{J-B}}{\theta_{J-C} + \theta_{C-Air} + \theta_{J-B}} + \frac{\Delta T_C}{Q}$$
(7)

$$0 < \frac{\theta_{J-B}}{\theta_{J-C} + \theta_{C-Air} + \theta_{J-B}} < 1 \tag{8}$$

$$\theta_{J-Amb} < \theta_{J-C} + \frac{\Delta T_C}{Q} \tag{9}$$

Conservative model:  $\square_{JA} = \theta_{J-C} + \square_{CA}$  (10)

Assuming the weighting term (8) as 1 (max),  $\theta_{J-Amb}$  (9) can be substituted by the upper bounded value  $\Theta_{JA}$  (10), resulting in the conservative, simplified model shown in Figure 7. This simplified model for  $\Theta_{JA}$  is used throughout this paper.

#### 3.4 Thermal Performance with No Heatsink

In order to assess the contribution of mold compound to  $\Theta_{CA}$  and, in parallel, to get a baseline for the heatsink contribution, units of configuration C on MC1 and MC2, without heatsink, were excited asymmetrically, by applying power to opposite package quarters, Figure 8.



Figure 8 – Comparison of MC1-MC2 performance, on units without heatsink and asymmetric (diagonal) heating.

The MC2 unit reduces  $\Theta_{CA}$  by ~11% relative to MC1 unit, as result from the improved in-package heat spreading. The XY-plane heat spreading is clearly seen on the normalized temperature difference at the surface  $(\theta_{\text{Surf}})$  and along the "hot" diagonal ( $\theta_{Diag}$ ). The better thermal conductivity of MC2 ( $\lambda$ =3.1 W/m.K vs 1.0W/m.K of MC1) improves the inpackage heat spreading, which increases the effective heat dissipation area and reduces heat resistance to both the air and PCB. This mechanism is sketched in Figure 9. The fact that  $\Delta T$  to ambient is the same for both cases (~43°C), in spite of the higher power dissipated on MC2 (1.4W versus 1.25W on MC1 unit), also means that the "hot spots" are smoothed out, i.e., the two maxima on the hot diagonal are spread laterally, instead of being amplified, which would be expected if power increases for the same material and geometry conditions.



Figure 9 – Improved in-package heat spreading of MC2 results in lower  $\theta_{J-C}$  (values referring to the 8x8 WLFO SiP demonstrator)

The better thermal conductivity of MC2 directly influences the main heat path to the package surface,  $\theta_{J-C}$ , as seen in

Figure 2. Taking into account both conduction and spreading effects of  $\lambda_{MC2}$ ,  $\Theta_{JA}$  reduces from >37K/W (MC1) down to ~32K/W (-14%). Note that  $\Theta_{JA}$  on MC1 case represents the performance of a standard WLFO package on a generic scenario of asymmetric heating, with hot spots, thus being the baseline comparison for the demonstrator.

A lower  $\Theta_{CA}$  is observed for the 4-quadrant excitation and is similar for MC1 and MC2,  $\Theta_{CA} \approx 24 \text{K/W}$ . The  $\Theta_{CA}$ dependence on the heated area results from its calculation method, which takes the temperature at the hottest spot, now at the package center. This is explained in Figure 10, where the 4-quadrant excitation is simulated as a sum of two diagonal excitation. The profile for each quadrant is thus the algebraic sum of the profiles measured as a "cold" quadrant and as a "hot" quadrant. If we consider, for simulation purposes, the second diagonal excitation as the mirror of the first diagonal (measured values from MC2) and add the effects, the simulated profile for the 4-quadrant heating indicates the hotter point at the package center (no longer over each hot quadrant) and  $\Theta_{\text{CA}}{=}24\text{K/W},$  which is in excellent agreement with the real values. An identical analysis with MC1 values has shown identical results.



**Figure 10** – Simulation of 4-quadrant heating by the sum of hot and cold diagonals, in excellent agreement to experimental values

The  $\theta_{C-A}$  dependence on the heated area is another way to translate that  $\Theta_{CA}$  relies on the *effective* area exchanging heat to the ambient, either to the air or to PCB. The 4-quadrant heating case exhibits lower  $\Theta_{CA}$  because it exploits better, or more uniformly, almost all package area. The same  $\Theta_{CA}$  value was observed for MC1 and MC2, because the inpackage heat spreading becomes not relevant when the package is symmetrically and more uniformly heated (4-quadrant).

#### 3.5 Thermal Performance With Heatsink

As expected, the heat-spreading effect of heatsink eliminates hot-spots, maximizes the heat dissipation area thus minimizes  $\Theta_{CA}$  and, consequently,  $\Theta_{JA}$ . Referring to Table 1, the heatsink reduces  $\Theta_{CA}$  to ~20K/W, either for MC1 or MC2, and regardless if diagonal heating or full heating was applied. That is, the heatsink provides a "flat" temperature  $(\Delta T < 1^{\circ}C)$ , regardless of the heat distribution underneath and MC type, as shown in Figure 11. It should be noted that the heatsink, being larger than the package  $(10 \times 10 \text{ mm}^2 \text{ vs})$  $8 \times 8 \text{mm}^2$  of the SiP), definitely contributes to lower  $\Theta_{CA}$ , but the simple increment of dissipation area to air of ~1.5x does not fully accounts for the  $\Theta_{CA}$  reduction from 34.5K/W to 20.7K/W on the MC1, 2-quadrant heating scenario. Clearly, this reduction relies on the heat spreading effect to enhance heat exchange area both to air and, thru the package itself, to the PCB.

The combined effects of the higher thermal conductivity of MC2 – which lower  $\theta_{J-C}$  and promotes in-package heat spreading; and the inclusion of a heatsink – responsible for the heat spreading and dissipation area increasing, contribute to the heat dissipation improvement of the demonstrator. The mechanism of heat transfer  $\rightarrow$  spreading  $\rightarrow$  dissipation is depicted in Figure 12, as well as the summary of overall gains achieved throughout the work.

The application of high conductivity SSA as TIM for the MC-HS bonding introduces a negligible  $\theta_{TIM}$  in the heat path (<0.03K/W, BLT <50µm). This is a key achievement on this work, because it results directly from the devised solution for organic-to metal bonding, which enables the application of a heatsink on over-molded SiP package.



Figure 11 - Heat-spreading effect of HS.



Figure 12 – Improved heat dissipation by lower  $\theta_{J-C}$  (heat transfer) and heatsink effect (heat spreading and dissipation).

#### 3.6 Estimation of Thermal Resistance to Air and PCB

Considering the cases of 4-quadrant heating on Table 1, in which the full SiP body is heated homogeneously, and considering the thermal model of Figure 7, the following assumptions can be made:

- The heatsink increases the dissipation area to air by the ratio of HS-to-Pkg area, i.e, 100/64, and  $\theta_{C-Air}$  is reduced proportionally;
- The heatsink does not affect the thermal path to PCB because all package area is already dissipating to PCB, so  $\theta_{J-B}$  is same with or without HS.

Given that an increase of ~56% of dissipation area to air only resulted in a reduction of ~15% of  $\Theta_{CA}$ , one can estimate values for  $\theta_{C-Air}$  and  $\theta_{J-B}$ . Figure 13 summarizes the calculations for MC2 case, estimating a reduction of  $\theta_{C-Air}$ from ~78K/W to ~50K/W by the introduction of the heatsink. An analysis with the values from MC1, 4-quadrant heating case would yield similar results.



Figure 13 – Estimation of  $\theta_{J-B}$  and  $\theta_{C-Air}$  with and without HS

The estimations for  $\theta_{C-Air}$  and  $\theta_{J-B}$  support the approximation done in equation (5),  $\theta_{J-C} \ll (\theta_{C-Air} + \theta_{J-Base})$ , thus supporting the simplified thermal model used. In addition, given that less than half the power is dissipated thru air, the temperature drop from junction to case is ~1°C, further validating the conservative model of equation (10).

#### 4 Thermo-Mechanical Reliability Performance

A very important and critical factor for the thermal performance of the demonstrator is the reliable bonding of the heatsink to the SiP package. The solution devised for the MC-heatsink bonding, i.e., the MC surface metallization and the application of highly conductive SSA, proved its good thermal performance. It must now provide the required reliability standards for electronic industry. Therefore, the reliability tests focused on the robustness of the MCheatsink bonding, rather than on the SiP package itself or its solder connection to the PCB, as this is related to a standard WLFO.

The selected tests were:

- TCoB 1000x [-25/100°C], 1 cycle/h, TC2, IPC9701
- Drop Test 30x
- Soaking/MSL1 (168h @ 85°C/ 85% RH + Reflow)

The Reliability tests were conducted at board-level (std JEDEC test board) to simulate a final application, on the 5 configurations in Figure 4. All units were submitted to a reflow cycle prior to the above tests (SAC profile reflow, to solder the units to the JEDEC PCB). Drop Test and Soaking/MSL1 were done on the same boards, in that sequence. The [-25/100°C] span in TCoB is in consistency with heatsink application, which has the purpose of narrowing the device's temperature operation range.

#### 4.1 Reliability Results of successful combination

Table 2 summarizes the reliability results achieved. Units with <u>Ni-metallized MC2</u> and using <u>TIMx</u> SSA for the heatsink bonding passed all tests, as shown in Figure 14 (TCoBx1000) and in the 7 respective units of Figure 15 (Drop Test and Soaking/MSL1, mixed configuration board).

Table 2 – Reliability test matrix and summary of results

Assy Materials			Reliability results summary			
MC	TIM	Met	Reflow	DT30	Soaking	TC1000
MC1	TIM	T: / NI:	Low SOR	Low SOR -SOR n.a.	n.a.	Low SOR
(ref)	TIVIX		>SOR			>SOR
MC2	TIMx	Ti		n.a.	n.a.	0
		Ni	$\checkmark$	$\checkmark$	$\checkmark$	<ul> <li>Image: A start of the start of</li></ul>
	TIMz	Ti	v -	./		٢
		Ni	~	•	n.a.	~

Figure 14 shows SAM results after reflow and after TCoBx1000, for the successful configuration, with almost all units showing good and unchanged MC-HS bonding. Only unit #14 (top row,  $2^{nd}$  unit from the right) showed relevant degradation, note however, from an already large delaminated status (~40%). Compared to the other units, with "clean" SAM after Reflow, this points out to a problem during assembly, likely on the cleanliness of the surfaces causing poor adhesive wetting (no plasma surface activation was used). That is, no delamination is caused by the thermal cycle on units with no delamination at start, so it is critical to have a good surface cleanliness and adhesive wetting during P&P and adhesive lamination.



Figure 14 - TIMx over Ni-metallized MC2 passed TC1000.



**Figure 15** – On a mixed configuration board, the units with MC2/Ni/TIMx showed no change after Dropt Test and Soaking/MSL1 test, from initial SAM (after reflow, not shown)

Figure 15 shows SAM results of Drop Test and [subsequent] Soaking/ MSL1, on a mixed-built board, with MC2/Ni/TIMx and TIMz, and *Dummy* units. (*Dummies refer* to units used for setup procedures, without SMD components, on *Ti-metallized MC and bonded with either TIMx or TIMx.*) On the Drop Test, no evolution was observed in any of the units (initial SAM after reflow not shown, but identical to that of Drop Test). On the Soaking test, only unit#1 (lower left corner, MC2/Ni/TIMz) showed negative evolution, from an already delaminated status. The seven MC2/Ni/TIMx units showed full laminated areas at the start, with exception of unit #4 with <20% delaminated area and assessed as acceptable. No evolution is observed on both tests, even on unit #4, thus passing the tests.

#### 4.2 Reliability Results of TIMz

In contrast to the good results on MC2/Ni/TIMx units in Figure 15, is it clear the very different and worse behavior of the other units, either with TIMz or on dummy units. The poor bonding results of TIMz are better seen in Figure 16, present already at initial SAM, before TC. These bad results are possibly due to a poorer wettability and/or flow-ability of TIMz during Pick&Place of the SiP over the heatsink (refer to Figure 5), as the "cross" dispensing shape is clearly visible. The TC test stopped at the TC300 (first check point), with no evolution at TC.

A slightly better MC-HS adhesion is observed on the Timetallized units, however this does not mean better adhesion of TIM to Ti, because the delamination occurs at TIM-HS interface, not MC-TIM. In fact, on the Ni-metallized units almost all TIM remained at the MC. This is better seen on the heatsink pull-off on unit #15, after Drop Test, shown at the top of Figure 15. The delaminated area (white area on SAM) corresponds to TIM over MC and HS is clean at that area, while laminated area (darker corner at SAM) showed very good adhesion, even causing the corner of the MC to be ripped-off from the package and remaining of the TIM. (Note: This also demonstrates the very strong bonding of sputtered metal to MC.) It remains unexplored the reason why the better MC-HS adhesion on Ti-metallized units.



Figure 16 – TIMz showed poor adhesion results overall. Test stopped at TC300  $(1^{st}$  check point) with no evolution.

#### 4.3 Reliability Results of MC1

Figure 17 shows the TC1000 results performed on MC1/Ti/TIMx units. This test is relevant to assess the MC-metallization solution on a "Low Cost" construction version, i.e., using the standard MC1 and simplifying the metallization to Ti sputtering (in fact, TiO2, as Ti oxidizes

immediately when in contact to air). The top row, with Construction C, showed good result after both reflow and TC, comparable to those achieved on MC2/Ni/TIMx, with only very small and not relevant delamination at the TIM edges.



Figure 17 - TC1000 results on "low cost" Ti-metallized MC1

Construction C has lower occupation ratio (~25%) than A/B (~45%), so this results suggests the reliability of the proposed "Low Cost" solution is, to some extension, sensitive to the Si Occupation Ratio (SOR) and, consequently, to the CTE of the package. As Si has much lower CTE than MC, the lower the Si content, the higher the overall package's CTE and closer to that of MC. This results, i.e., good reliability of MC1 for low SOR construction, is also consistent to the good results of MC2, regardless of package's SOR, because of the higher CTE of MC2 (alumina fillers) relative to MC1 (silica fillers). Moreover, MC2's CTE is much closer to that of heatsink (Cu), which reduces the stress on TIM due to the slight CTE mismatch between HS and package. In this sense, the use of MC2 is further justified, not only because of better thermal performances, but also for the ability to reduce stress on TIM.

#### 5 Conclusions

A Power Fan Out demonstrator, combining SiP and Power applications, has been successfully manufactured and its thermal performance and thermomechanical reliability has been shown. The key element on this work was the organic-to-metal bonding method, by means of sputtering metallization on the package backside Mold Compound (MC), which allowed the application of high conductivity Sintered Silver Adhesives (SSA) for the MC-Heatsink bonding. This way, the SSA TIM introduced a negligible  $\theta_{\rm TIM}$  in the heat path and the application of a heatsink on over-molded SiP became almost as trivial as in metallic packages.

On the reliability, the SiP-HS bonding on the demonstrator passed TC1000 cycles, Drop Test and Soaking/MSL1 test:

- TiCuNi metallization over thermally improved MC (MC2), along with SSA TIMx for the bonding of a Niplated Cu heatsink, proved to be a reliable solution;
- MC2, with CTE closer to that of Cu HS, reduced the stress on TIM and contributed to the reliability of the solution;
- A simplified, low cost solution of Ti sputtering over standard MC and using TIMx for HS bonding, showed equally suitable for packages with low occupation ratio.
- On the thermal performance, the mechanism of heat transfer → spreading → dissipation was implemented and verified:
- The demonstrator with no heatsink has shown  $\Theta_{CA}$  of ~35K/W and ~31K/W, for MC1 and MC2 respectively, on a diagonal heating pattern; MC2 reduced  $\Theta_{CA}$  by ~11% on the account of better in-package heat spreading, which increased the effective dissipation area to air and PCB;
- The application of heatsink reduced  $\Theta_{CA}$  to ~20K/W, for both MC types and regardless of the heating pattern inside the SiP (hot spots); a  $\Delta T < 1^{\circ}$ C at the heatsink surface showed the maximization of heat dissipation area;
- For applications where a large and system level heatsink is applied over the package,  $\theta_{J-C}$  becomes the dominant thermal resistance in the heat dissipation path. In such cases, MC2 brings the advantage of  $\theta_{J-C} < 1$ K/W.

On the manufacturing side, a process for "*HS-on-Pkg*", addressing the more challenging case of *heatsink larger than package*, was devised and successfully tested on the manufacturing of the demonstrator units. The process is capable for volume production and uses the standard equipment at Nanium's 300mm FOWLP process line.

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# **Authors Index**

Aasmundtveit, Knut E. Abo Ras, Mohamad Aladov, Andrey Alberto, Diego Aliyu, Attahir Murtala Ansari, Zaid A J Aranda, Sandra Azadmehr, Mehdi **Bailey**, Chris Bándy, EnikĐ Barros, Hugo Bein, Márton C. Besold, Sebastian Biber, Catharina R **Bissuel**, Valentin Bluet, Jean-Marie Bognár, György **Boianceanu**, Cristian Bornoff, Robin Cardoso, André Gil Casano, Giovanni Casper, Thorben Castellazzi, Alberto Cattin, Viviane Chapuis, Pierre-Olivier Cheramy, Severine Chernyakov, Anton Chevrier, Norbert Chou, Wibawa Codecasa, Lorenzo Colonna, Jean-Philippe consortium, QuantiHeat Coudrain, Perceval d'Alessandro, Vincenzo Daniel, Olivier Defregger, Stefan Elger, Gordon Ender, Ferenc Enright, Ryan Fang, Yake Farcy, Alexis Farkas, Gábor Fernández, Manuel Fukunaga, Shuhei Funaki, Tsuyoshi Gaál, Lajos García Fernández, Javier Gomes, Séverine Górecki, Krzysztof Guen, Eloïse Hammer, René Hamon, Benoit Hantos, Gusztáv Hattel, Jesper Henri Hegedüs, János

Session 1 Session 6, Session 12 Session 10 Poster 2 Session 7 Poster 2 Session 7 Session 1 Session 4 Poster 1 Poster 2 Session 9 Session 2 Session 8 Session 4 Session 6 Poster 1 Session 3 Session 8, Session 9 Poster 2 Poster 1 Session 2 Session 7 Poster 2 Session 6 Session 1 Session 10 Session 1 Session 3 Session 4, Session 4 Session 1 Session 6 Session 1 Session 4, Session 4 Session 4 Session 9 Session 2 Session 1 Session 12 Session 8 Session 1 Session 9 Session 7 Session 7 Session 7 Session 9 Session 1 Session 6, Session 6, Poster 2 Session 10 Session 6 Session 9 Session 9 Poster 1, Poster 2, Session 10, Session 11 Poster 2 Session 10, Session 11

Heilmann. Jens Hildenbrand, Volker Ito, Hiroaki Jabbari, Mirmasoud Jani, Lázár Janicki, Marcin Janicki, Marcin Joerg, Bauer Joly, Julien Jordà, Xavier Juergen, Keller Kalashnikov, Ivan Karvinen, Reijo Keller, Jürgen Kempitiya, Asantha Kendig, Dustin Kharitonov, Igor A. Kim, Chang Wan Klapetek, Petr Kocsis, György Kotelon, Marie-Cécile Kovács, Boldizsár Kozlov, Alexander Kraker, Elke Kristóf, Gergely Lampio, Kaj Laraqi, Najib Lebedev, Sergey V. Lee, Kun Hyung Lee. Kwanhun Lefebvre, Charles-Alexis Lefèvre, Stéphane Lei, Shenghui Liu, E Llorente, Sergio Lugten, Sangye Lui, Tung Ching Luiten, Wendy Ma, Byungjin Magnani, Alessandro Magnien, Julien Maj, Cezary Maquet, Jérôme Marcus, Schulz Márkus, Ferenc Markus, Woehrmann Martin, Genevieve Martinek. Jan Marty, Christophe Massoud, Mouhannad Matsuyama, Shinichiro Maurya, Ram Subhash May, Daniel Mitterhuber, Lisa Mizerov, Michael Mizsei, János Mohamad, Abo Ras Mohn, Melanie Monier-Vinard, Eric

Poster 1 Session 9 Session 3 Poster 2 Poster 2 Session 12 Session 6 Session 11 Session 9 Session 7 Session 11 Session 10 Poster 2 Poster 1 Session 3 Session 6 Session 12 Poster 1 Poster 2 Poster 1 Session 4 Session 11 Poster 2 Session 9 Session 11 Poster 2 Session 4 Session 12 Poster 1 Poster 1 Poster 1 Poster 2 Session 12 Session 2 Session 7 Session 9 Poster 1 Session 2 Poster 1 Session 4, Session 4 Session 9 Session 5 Session 8 Session 11 Poster 1 Session 11 Session 9 Poster 2 Session 9 Session 6 Session 3 Poster 2 Session 11, Session 12 Session 9 Session 10 Poster 1, Poster 1 Session 11 Session 1 Session 4

Poster 1 Montero, Jose Luis Poster 1 Mroßko, Raul Poster 1 Muthuraman, Balaji Nandhivarm Poster 2 Na, Zhigang Session 5, Session 6 Napieralski, Andrzej Session 3 Neag, Marius Session 3 Negoita, Andrei Session 1 Nielsch, Kornelius Niittymäki, Lauri Petteri Session 8 Noijen, Sander Poster 1 Session 3 Ohbu, Toshiharu Ordonez-Miranda, Jose Session 6 Session 8 Parry, John Pérez Rodriguez, Nicolás Session 1 Perpiñà, Xavier Session 7 Péter, Norbert Session 11 Petrosyants, Konstantin O. Session 12 Piret, Hélène Poster 2 Piva. Stefano Poster 1 Plesa, Cosmin-Sorin Session 3 Plesz, Balázs Poster 1 Pohl, László Poster 1 Session 11 Poppe, Andras Poppe, András Poster 2, Session 9, Session 10 Prieto, Rafael Session 1 Session 10 Ptak, Przemysław Ranieri. Marco Poster 2 Raszkowski, Tomasz Session 6 Session 1 Reith, Heiko Renahy. David Session 6 Renaudin, Theo Session 9 Rencz, Marta Session 9, Session 11 Rinaldi. Niccolò Session 4, Session 4 **Rogie**, Brice Session 4 Session 2 Römer, Ulrich Rosenfeld, Moshe Session 8 Roy, Avisek Session 1 Rózsás, Gábor Poster 1 Rubio. Leire Poster 1 Session 12 Sambursky, Lev M. Samson, Agnieszka Session 6 Schierning, Gabi Session 1 Schilders, Wil Session 9 Schlörb, Heike Session 1 Schöps, Sebastian Session 2 Session 11 Sergey, Sheva Shakouri, Ali Session 6 Session 12 Shen. Alexandre Poster 1 Sheva, Sergey Sieger, Tom Session 1 Skadron, Kevin Session 5 Šlesinger, Radek Poster 2 Session 12 Stakhin, Veniamin G. Poster 2 Staliulionis, Zygimantas Session 5 Stan, Mircea Suh, Won-Bae Poster 1 Szabó, Péter Gábor Poster 1 Takács, Gábor Poster 1 Tay, Andrew Session 6

Tony, Catherine	Session 4
Tóth, Péter	Session 11
Tothe, Benoit	Session 9
Ur, Soma	Poster 1
Valtr, Miroslav	Poster 2
van Veen, Co	Session 2
Vass-Varnai, Andras	Session 8
Vellvehi, Miquel	Session 7
Volz, Sebastian	Session 6
Wang, Gang	Session 8
Wang, Ke	Session 5
Wilson, John	Session 8
Wong Voon, Hon	Session 8
Wunderle, Bernhard	Poster 1
Wunderle, Bernhard	Session 6, Session 11, Session 12
Xiaodan, Chen	Session 8
Xing, Fu	Session 8
Yamanari, Naoki	Session 3
Yu, Joan	Session 9
Yuksel-Gungor, Aylin	Poster 2
Zahner, Thomas	Session 2
Zajac, Piotr	Session 5
Zakgeim, Aleksander	Session 10
Zemach, Efi	Session 8
Zubert, Mariusz	Session 6

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